

ESP32-S2-MINI-1 & ESP32-S2-MINI-1U

Datasheet

2.4 GHz Wi-Fi (802.11 b/g/n) module

Built around ESP32-S2 series of SoC, Xtensa® single-core 32-bit LX7 microprocessor

4 MB flash and optional 2 MB PSRAM in chip package

37 GPIOs, rich set of peripherals

On-board PCB antenna or external antenna connector



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About This Document

This document provides the specifications for ESP32-S2-MINI-1 and ESP32-S2-MINI-1U modules.

Document Updates

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Revision History

For revision history of this document, please refer to the [last page](#).

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1 Module Overview

1.1 Features

CPU and On-Chip Memory

- ESP32-S2FH4 or ESP32-S2FN4R2 chip embedded, Xtensa® single-core 32-bit LX7 microprocessor, up to 240 MHz
- 128 KB ROM
- 320 KB SRAM
- 16 KB SRAM in RTC
- 4 MB embedded flash
- 2 MB embedded PSRAM (ESP32-S2FN4R2 only)

Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μ s guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Peripherals

- GPIO, SPI, LCD, UART, I2C, I2S, Camera interface, IR, pulse counter, LED PWM, TWAI®

(compatible with ISO 11898-1), USB OTG 1.1, ADC, DAC, touch sensor, temperature sensor

Integrated Components on Module

- 40 MHz crystal oscillator

Antenna Options

- On-board PCB antenna (ESP32-S2-MINI-1)
- External antenna via a connector (ESP32-S2-MINI-1U)

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature: -40 ~ 85 °C

Certification

- Green certification: RoHS/REACH
- RF certification: FCC/CE-RED/SRRC/IC

Test

- HTOL/HTSL/uHAST/TCT/ESD

1.2 Description

ESP32-S2-MINI-1 and ESP32-S2-MINI-1U are two powerful, generic Wi-Fi MCU modules that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), wearable electronics and smart home.

The ordering information of the two modules is listed as follows:

Table 1: Ordering Information

| Module | Ordering code | Chip embedded | Module dimensions (mm) |
|---|-----------------------|---------------|------------------------|
| ESP32-S2-MINI-1 (ANT) | ESP32-S2-MINI-1-N4 | ESP32-S2FH4 | 15.4 × 20.0 × 2.4 |
| | ESP32-S2-MINI-1-N4R2 | ESP32-S2FN4R2 | |
| ESP32-S2-MINI-1U (CONN) | ESP32-S2-MINI-1U-N4 | ESP32-S2FH4 | 15.4 × 15.4 × 2.4 |
| | ESP32-S2-MINI-1U-N4R2 | ESP32-S2FN4R2 | |
| Notes: | | | |
| For dimensions of the external antenna connector, please see Section 7.3. | | | |

ESP32-S2-MINI-1 comes with a on-board PCB antenna, and ESP32-S2-MINI-1U with an U.FL connector for external antenna. Both ESP32-S2-MINI-1 and ESP32-S2-MINI-1U have two variants:

- integrating the ESP32-S2FH4 chip (which is embedded with a 4 MB high-temperature flash), or
- integrating the ESP32-S2FN4R2 chip (which is embedded with a 4 MB flash and 2 MB PSRAM)

The two variants only differ in the chip integrated. In this datasheet unless otherwise stated, ESP32-S2-MINI-1 refers to both ESP32-S2-MINI-1-N4 and ESP32-S2-MINI-1-N4R2, whereas ESP32-S2-MINI-1U refers to both ESP32-S2-MINI-1U-N4 and ESP32-S2-MINI-1U-N4R2.

The ESP32-S2FH4 chip and the ESP32-S2FN4R2 chip falls into the same category, namely ESP32-S2 chip series. ESP32-S2 series of chips has an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. It has a low-power co-processor that can be used instead of the CPU to save power while performing tasks that do not require much computing power, such as monitoring of peripherals.

ESP32-S2 series integrates a rich set of peripherals, ranging from SPI, I2S, UART, I2C, LED PWM, TWAI®, LCD, Camera interface, ADC, DAC, touch sensor, temperature sensor, as well as up to 43 GPIOs. It also includes a full-speed USB On-The-Go (OTG) interface to enable USB communication.

The ESP32-S2FH4 chip and the ESP32-S2FN4R2 chip vary in:

- temperature of embedded flash
- whether a PSRAM is embedded

For details, please refer to Section *Family Member Comparison* in [ESP32-S2 Series Datasheet](#).

1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Home Control Panel
- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications
- Smart POS Machines

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2 Block Diagram

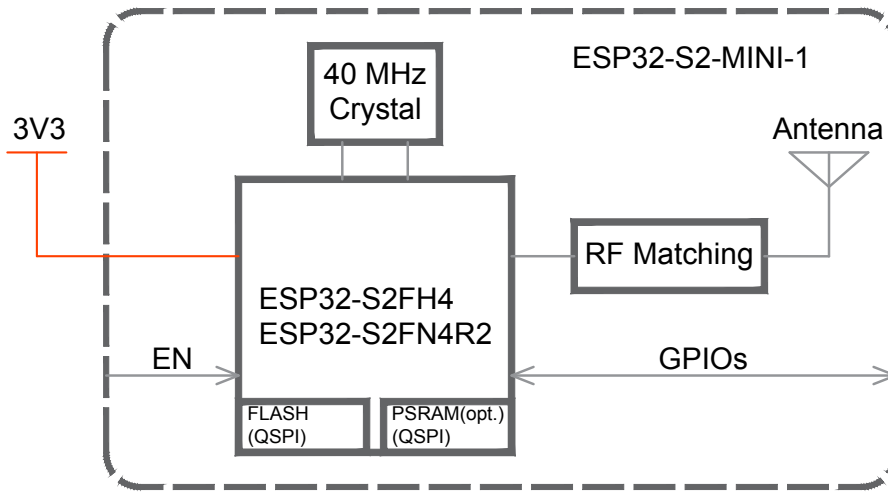


Figure 1: ESP32-S2-MINI-1 Block Diagram

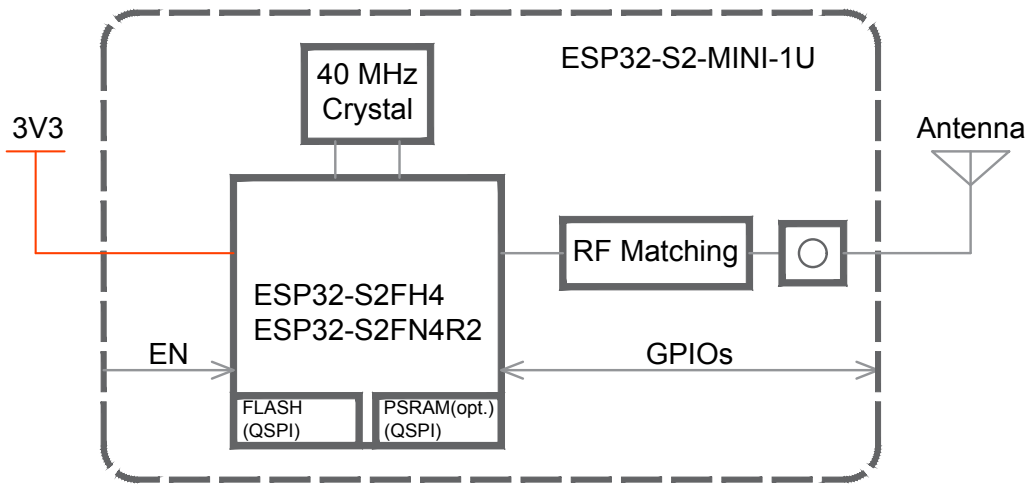


Figure 2: ESP32-S2-MINI-1U Block Diagram

3 Pin Definitions

3.1 Pin Layout

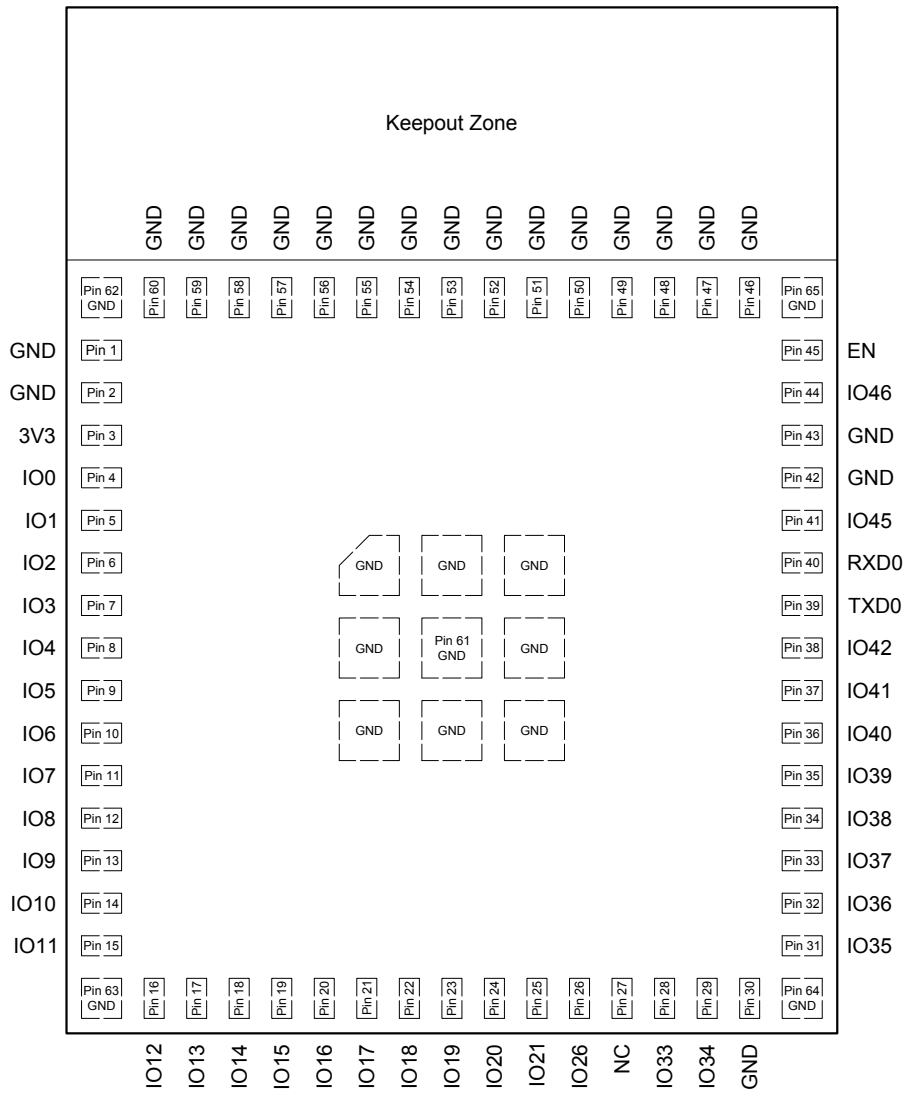


Figure 3: ESP32-S2-MINI-1 Pin Layout (Top View)

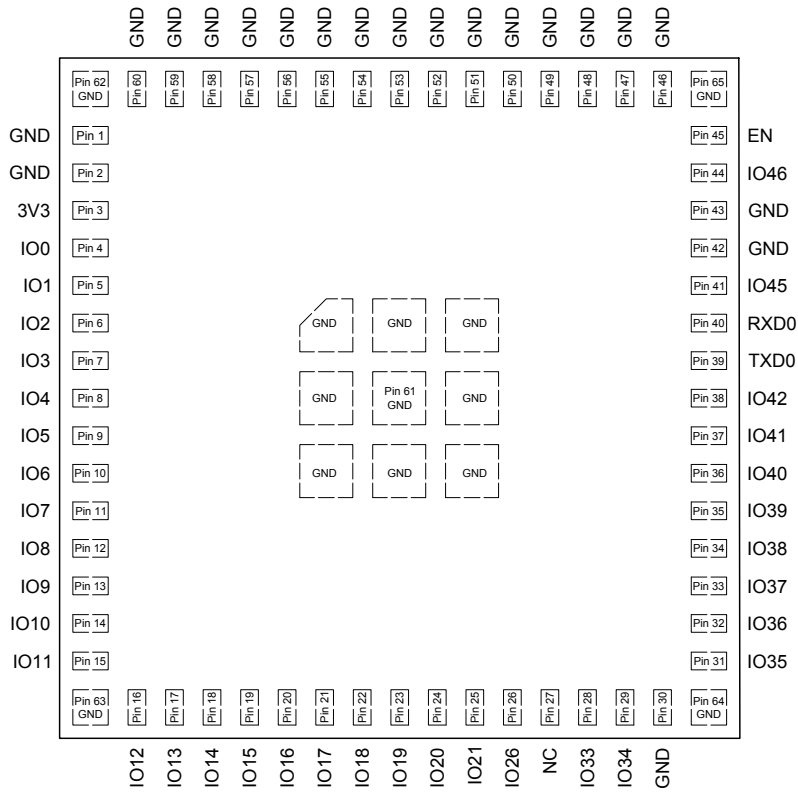


Figure 4: ESP32-S2-MINI-1U Pin Layout (Top View)

Note:
 The pin diagram shows the approximate location of pins on the module. For the actual mechanical diagram, please refer to Figure 7.1 Physical Dimensions.

3.2 Pin Description

The module has 65 pins. See pin definitions in Table 2.

Table 2: Pin Definitions

| Name | No. | Type | Function |
|------|-------------------------|-------|------------------------------------|
| GND | 1, 2, 30, 42, 43, 46-65 | P | Ground |
| 3V3 | 3 | P | Power supply |
| IO0 | 4 | I/O/T | RTC_GPIO0, GPIO0 |
| IO1 | 5 | I/O/T | RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0 |
| IO2 | 6 | I/O/T | RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1 |
| IO3 | 7 | I/O/T | RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2 |
| IO4 | 8 | I/O/T | RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3 |
| IO5 | 9 | I/O/T | RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4 |
| IO6 | 10 | I/O/T | RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5 |
| IO7 | 11 | I/O/T | RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6 |
| IO8 | 12 | I/O/T | RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7 |

| Name | No. | Type | Function |
|------|-----|-------|--|
| IO9 | 13 | I/O/T | RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPiHD |
| IO10 | 14 | I/O/T | RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPiCS0, FSPiIO4 |
| IO11 | 15 | I/O/T | RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPiD, FSPiIO5 |
| IO12 | 16 | I/O/T | RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPiCLK, FSPiIO6 |
| IO13 | 17 | I/O/T | RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPiQ, FSPiIO7 |
| IO14 | 18 | I/O/T | RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPiWP, FSPiDQS |
| IO15 | 19 | I/O/T | RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P |
| IO16 | 20 | I/O/T | RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N |
| IO17 | 21 | I/O/T | RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1 |
| IO18 | 22 | I/O/T | RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3 |
| IO19 | 23 | I/O/T | RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D- |
| IO20 | 24 | I/O/T | RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+ |
| IO21 | 25 | I/O/T | RTC_GPIO21, GPIO21 |
| IO26 | 26 | I/O/T | SPiCS1, GPIO26 |
| NC | 27 | — | NC |
| IO33 | 28 | I/O/T | SPiIO4, GPIO33, FSPiHD |
| IO34 | 29 | I/O/T | SPiIO5, GPIO34, FSPiCS0 |
| IO35 | 31 | I/O/T | SPiIO6, GPIO35, FSPiD |
| IO36 | 32 | I/O/T | SPiIO7, GPIO36, FSPiCLK |
| IO37 | 33 | I/O/T | SPiDQS, GPIO37, FSPiQ |
| IO38 | 34 | I/O/T | GPIO38, FSPiWP |
| IO39 | 35 | I/O/T | MTCK, GPIO39, CLK_OUT3 |
| IO40 | 36 | I/O/T | MTDO, GPIO40, CLK_OUT2 |
| IO41 | 37 | I/O/T | MTDI, GPIO41, CLK_OUT1 |
| IO42 | 38 | I/O/T | MTMS, GPIO42 |
| TXD0 | 39 | I/O/T | U0TXD, GPIO43, CLK_OUT1 |
| RXD0 | 40 | I/O/T | U0RXD, GPIO44, CLK_OUT2 |
| IO45 | 41 | I/O/T | GPIO45 |
| IO46 | 44 | I | GPIO46 |
| EN | 45 | I | High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating. |

Notice:

- IO18 on the module is pulled up to VDD33 through a 10 k Ω resistor. For details, please refer to Figure 5 and Figure 6.
- IO26 is used by the embedded PSRAM on the ESP32-S2-MINI-1-N4R2 and ESP32-S2-MINI-1U-N4R2 modules, and cannot be used for other purposes.
- For peripheral pin configurations, please refer to [ESP32-S2 Series Datasheet](#).

3.3 Strapping Pins

ESP32-S2 series of chips has three strapping pins: GPIO0, GPIO45, GPIO46. The pin-pin mapping between ESP32-S2 series of chips and the module is as follows, which can be seen in Chapter 5 *Schematics*:

- GPIO0 = IO0
- GPIO45 = IO45
- GPIO46 = IO46

Software can read the values of corresponding bits from register "GPIO_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

IO0, IO45 and IO46 are connected to the internal pull-up/pull-down. If they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S2 series of chips.

After reset, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration of the strapping pins.

Table 3: Strapping Pins

| VDD_SPI Voltage ¹ | | | |
|--|-----------|--------------------|--------------------|
| Pin | Default | 3.3 V | 1.8 V |
| IO45 ³ | Pull-down | 0 | 1 |
| Bootling Mode ² | | | |
| Pin | Default | SPI Boot | Download Boot |
| IO0 | Pull-up | 1 | 0 |
| IO46 | Pull-down | Don't-care | 0 |
| Enabling/Disabling ROM Code Print During Bootling ^{4 5} | | | |
| Pin | Default | Enabled | Disabled |
| IO46 | Pull-down | See the fifth note | See the fifth note |

Note:

1. Firmware can configure register bits to change the settings of "VDD_SPI Voltage".
2. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
3. Internal pull-up resistor (R1) for IO45 is not populated in the module, as the flash in the module works at 3.3 V by default (output by VDD_SPI). Please make sure IO45 will not be pulled high when the module is powered up by external circuit.
4. ROM code can be printed over TXD0 (by default) or DAC_1 (IO17), depending on the eFuse bit.
5. When eFuse UART_PRINT_CONTROL value is:
 - 0, print is normal during boot and not controlled by IO46.
 - 1 and IO46 is 0, print is normal during boot; but if IO46 is 1, print is disabled.

2 and IO46 is 0, print is disabled; but if IO46 is 1, print is normal.
3, print is disabled and not controlled by IO46.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|--------------------|----------------------|------|-----|------|
| VDD33 | Power supply voltage | -0.3 | 3.6 | V |
| T _{STORE} | Storage temperature | -40 | 105 | °C |

4.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|--|-----|-----|-----|------|
| VDD33 | Power supply voltage | 3.0 | 3.3 | 3.6 | V |
| I _{VDD} | Current delivered by external power supply | 0.5 | — | — | A |
| T _A | Operating ambient temperature | -40 | — | 85 | °C |
| Humidity | Humidity condition | — | — | 85 | %RH |

4.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------------|--|-------------------------|-----|-------------------------|------|
| C _{IN} | Pin capacitance | — | 2 | — | pF |
| V _{IH} | High-level input voltage | 0.75 × VDD ¹ | — | VDD ¹ + 0.3 | V |
| V _{IL} | Low-level input voltage | -0.3 | — | 0.25 × VDD ¹ | V |
| I _{IH} | High-level input current | — | — | 50 | nA |
| I _{IL} | Low-level input current | — | — | 50 | nA |
| V _{OH} ² | High-level output voltage | 0.8 × VDD ¹ | — | — | V |
| V _{OL} ² | Low-level output voltage | — | — | 0.1 × VDD | V |
| I _{OH} | High-level source current (VDD ¹ = 3.3 V, V _{OH} ≥ 2.64 V, PAD_DRIVER = 3) | — | 40 | — | mA |
| I _{OL} | Low-level sink current (VDD ¹ = 3.3 V, V _{OL} = 0.495 V, PAD_DRIVER = 3) | — | 28 | — | mA |
| R _{PU} | Pull-up resistor | — | 45 | — | kΩ |
| R _{PD} | Pull-down resistor | — | 45 | — | kΩ |
| V _{IH_nRST} | Chip reset release voltage | 0.75 × VDD ¹ | — | VDD ¹ + 0.3 | V |
| V _{IL_nRST} | Chip reset voltage | -0.3 | — | 0.25 × VDD ¹ | V |

Note:

1. VDD is the I/O voltage for a particular power domain of pins.
2. V_{OH} and V_{OL} are measured using high-impedance load.

4.4 Current Consumption Characteristics

With the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *RTC and Low-Power Management* in [ESP32-S2 Series Datasheet](#).

Table 7: Current Consumption Depending on RF Modes

| Work mode | Description | | Peak (mA) |
|---------------------|-------------|------------------------------------|-----------|
| Active (RF working) | TX | 802.11b, 20 MHz, 1 Mbps, @19.5 dBm | 310 |
| | | 802.11g, 20 MHz, 54 Mbps, @15 dBm | 220 |
| | | 802.11n, 20 MHz, MCS7, @13 dBm | 200 |
| | | 802.11n, 40 MHz, MCS7, @13 dBm | 160 |
| | RX | 802.11b/g/n, 20 MHz | 63 |
| | | 802.11n, 40 MHz | 68 |

Note:

- The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 100% duty cycle.
- The current consumption figures for in RX mode are for cases when the peripherals are disabled and the CPU idle.

Table 8: Current Consumption Depending on Work Modes

| Work mode | Description | | Current consumption (Typ) |
|-------------|---|----------------------|---------------------------|
| Modem-sleep | The CPU is powered on | 240 MHz | 22 mA |
| | | 160 MHz | 17 mA |
| | | Normal speed: 80 MHz | 14 mA |
| Light-sleep | — | | 550 μ A |
| Deep-sleep | The ULP co-processor is powered on. | | 235 μ A |
| | ULP sensor-monitored pattern | | 22 μ A @1% duty |
| | RTC timer + RTC memory | | 25 μ A |
| | RTC timer only | | 20 μ A |
| Power off | CHIP_PU is set to low level, the chip is powered off. | | 1 μ A |

Note:

- The current consumption figures in Modem-sleep mode are for cases where the CPU is powered on and the cache idle.
- When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consumption changes accordingly.

- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.
- During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I2C are able to operate.
- The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When touch sensors work with a duty cycle of 1%, the typical current consumption is 22 μ A.

4.5 Wi-Fi RF Characteristics

4.5.1 Wi-Fi RF Standards

Table 9: Wi-Fi RF Standards

| Name | | Description |
|--|--------|--|
| Center frequency range of operating channel <i>note1</i> | | 2412 ~ 2484 MHz |
| Wi-Fi wireless standard | | IEEE 802.11b/g/n |
| Data rate | 20 MHz | 11b: 1, 2, 5.5 and 11 Mbps 11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 11n: MCS0-7, 72.2 Mbps (Max) |
| | 40 MHz | 11n: MCS0-7, 150 Mbps (Max) |
| Antenna type | | PCB antenna, IPEX antenna |

1. Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.
2. For the modules that use IPEX antennas, the output impedance is 50 Ω . For other modules without IPEX antennas, users do not need to concern about the output impedance.

4.5.2 Transmitter Characteristics

Table 10: Transmitter Characteristics

| Parameter | Rate | Typ | Unit |
|-----------------------|-----------------|------|------|
| TX Power <i>note1</i> | 11b, 1 Mbps | 19.5 | dBm |
| | 11b, 11 Mbps | 19.5 | |
| | 11g, 6 Mbps | 18 | |
| | 11g, 54 Mbps | 15 | |
| | 11n, HT20, MCS0 | 18 | |
| | 11n, HT20, MCS7 | 13.5 | |
| | 11n, HT40, MCS0 | 18 | |
| | 11n, HT40, MCS7 | 13.5 | |

1. Target TX power is configurable based on device or certification requirements.

4.5.3 Receiver Characteristics

Table 11: Receiver Characteristics

| Parameter | Rate | Typ | Unit |
|----------------------------|-----------------|-----|------|
| RX Sensitivity | 1 Mbps | -97 | dBm |
| | 2 Mbps | -95 | |
| | 5.5 Mbps | -93 | |
| | 11 Mbps | -88 | |
| | 6 Mbps | -92 | |
| | 9 Mbps | -91 | |
| | 12 Mbps | -89 | |
| | 18 Mbps | -86 | |
| | 24 Mbps | -83 | |
| | 36 Mbps | -80 | |
| | 48 Mbps | -76 | |
| | 54 Mbps | -74 | |
| | 11n, HT20, MCS0 | -92 | |
| | 11n, HT20, MCS1 | -88 | |
| | 11n, HT20, MCS2 | -85 | |
| | 11n, HT20, MCS3 | -82 | |
| | 11n, HT20, MCS4 | -79 | |
| | 11n, HT20, MCS5 | -75 | |
| | 11n, HT20, MCS6 | -73 | |
| | 11n, HT20, MCS7 | -72 | |
| | 11n, HT40, MCS0 | -89 | |
| | 11n, HT40, MCS1 | -85 | |
| | 11n, HT40, MCS2 | -83 | |
| | 11n, HT40, MCS3 | -79 | |
| | 11n, HT40, MCS4 | -76 | |
| | 11n, HT40, MCS5 | -72 | |
| 11n, HT40, MCS6 | -70 | | |
| 11n, HT40, MCS7 | -68 | | |
| RX Maximum Input Level | 11b, 1 Mbps | 5 | dBm |
| | 11b, 11 Mbps | 5 | |
| | 11g, 6 Mbps | 5 | |
| | 11g, 54 Mbps | 0 | |
| | 11n, HT20, MCS0 | 5 | |
| | 11n, HT20, MCS7 | 0 | |
| | 11n, HT40, MCS0 | 5 | |
| | 11n, HT40, MCS7 | 0 | |
| Adjacent Channel Rejection | 11b, 11 Mbps | 35 | dB |
| | 11g, 6 Mbps | 31 | |
| | 11g, 54 Mbps | 14 | |
| | 11n, HT20, MCS0 | 31 | |
| | 11n, HT20, MCS7 | 13 | |
| | 11n, HT40, MCS0 | 19 | |
| | 11n, HT40, MCS7 | 8 | |

5 Schematics

This is the reference design of the module.

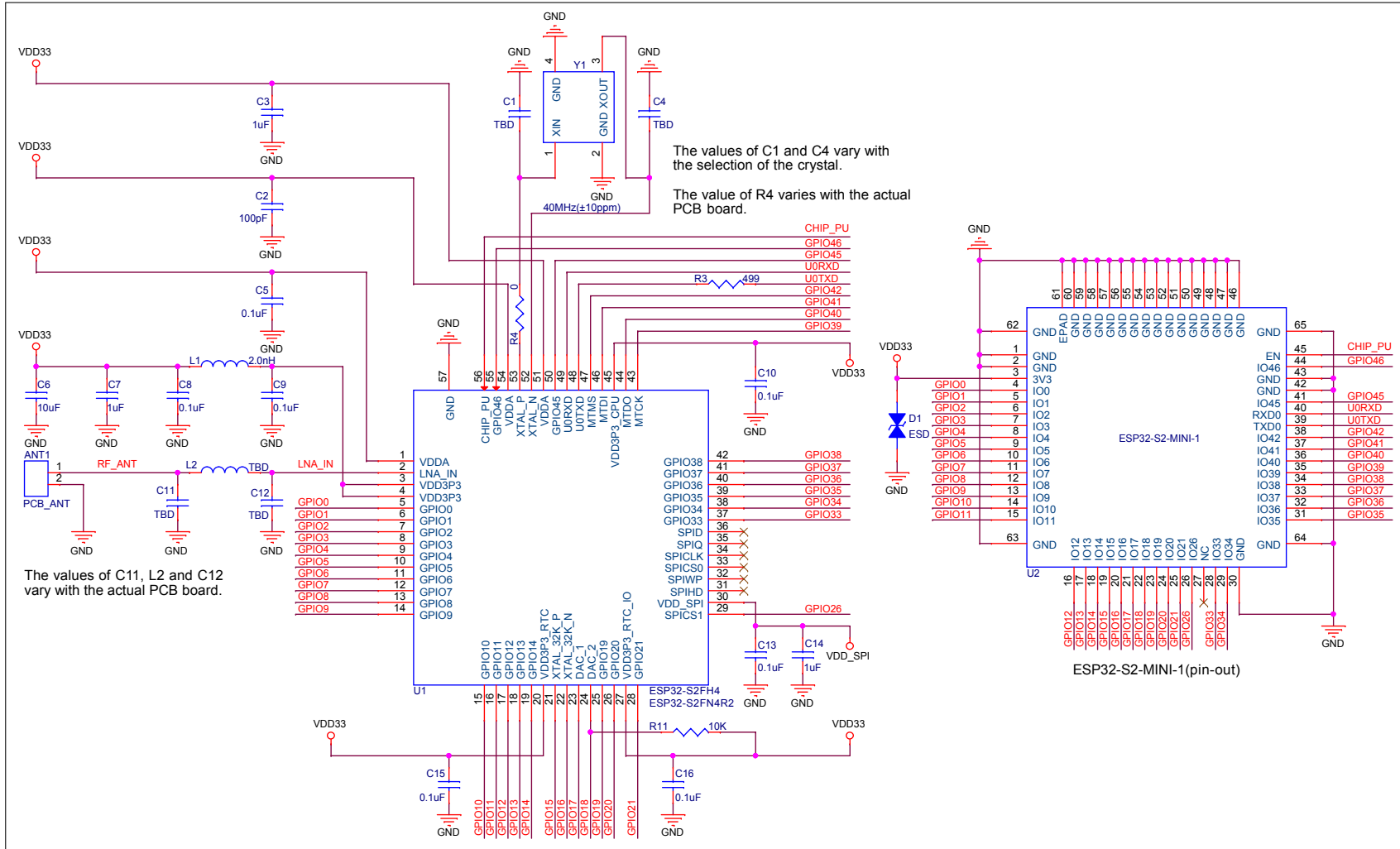


Figure 5: ESP32-S2-MINI-1 Schematics

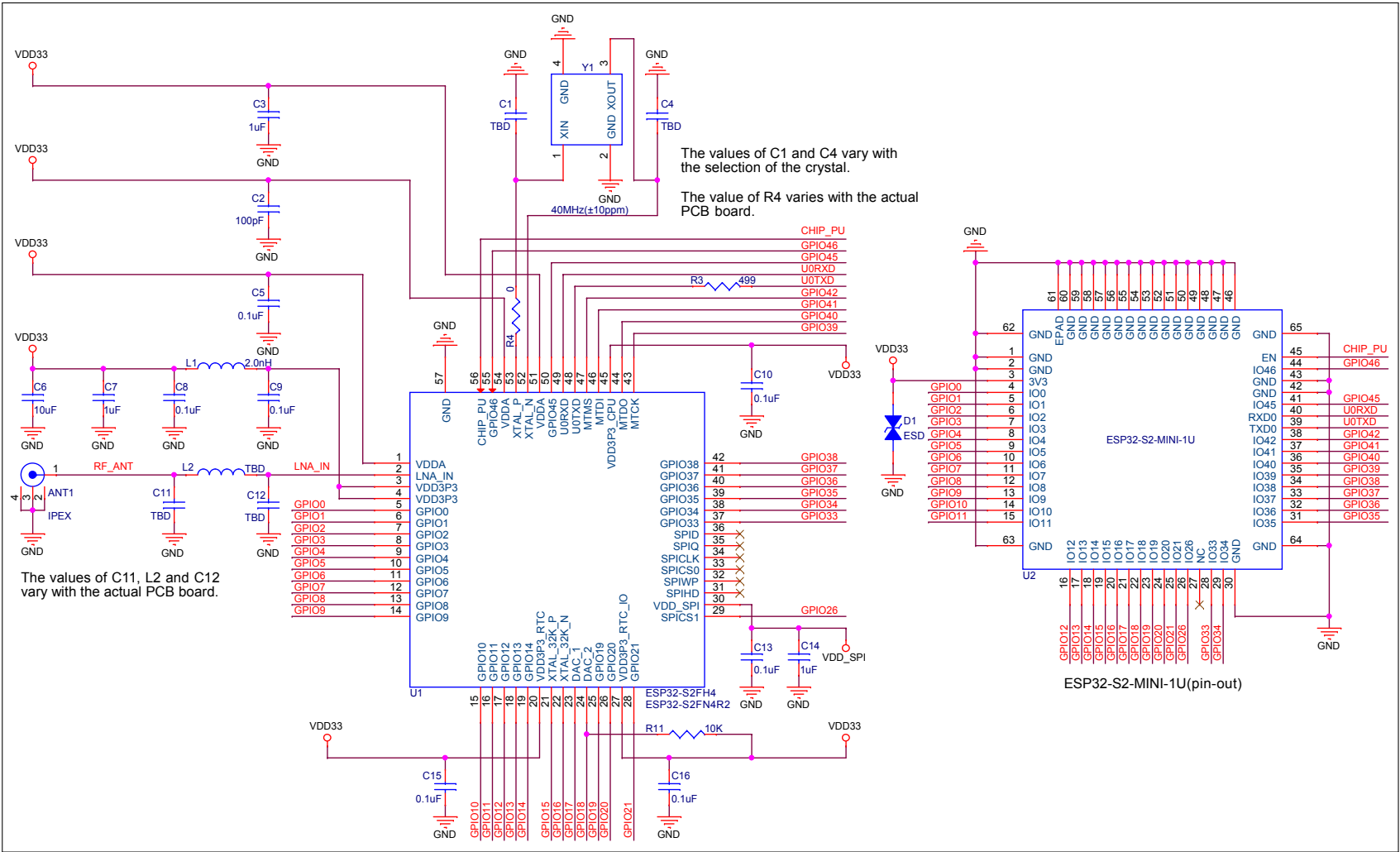


Figure 6: ESP32-S2-MINI-1U Schematics

6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

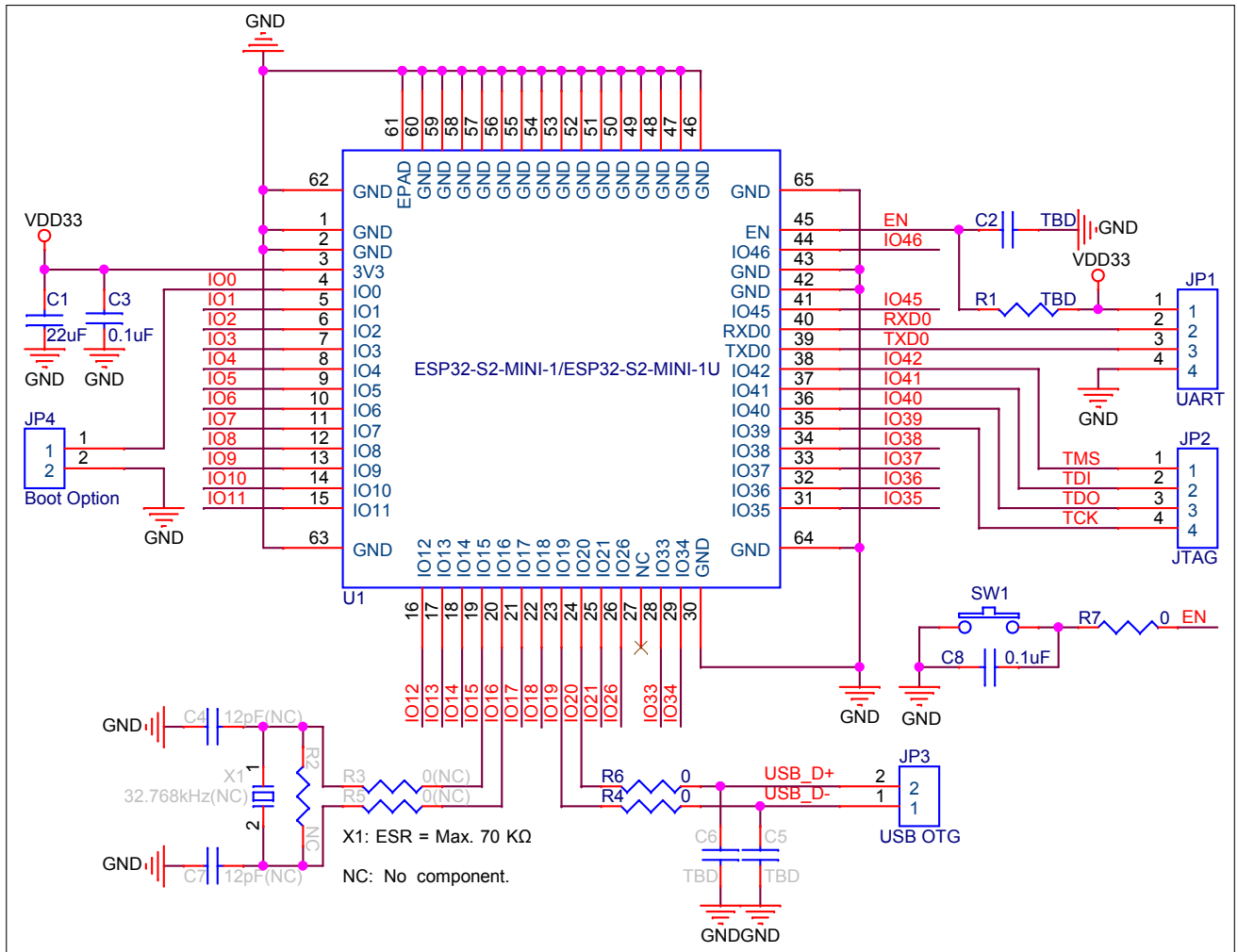


Figure 7: Peripheral Schematics

Note:

- Soldering the EPAD to the ground of the base board is not a must, though doing so can get optimized thermal performance. If users do want to solder it, they need to ensure that the correct quantity of soldering paste is applied.
- To ensure the power supply to the ESP32-S2 series of chips during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually $R = 10\text{ k}\Omega$ and $C = 1\ \mu\text{F}$. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S2's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in [ESP32-S2 Series Datasheet](#).

7 Physical Dimensions and PCB Land Pattern

7.1 Physical Dimensions

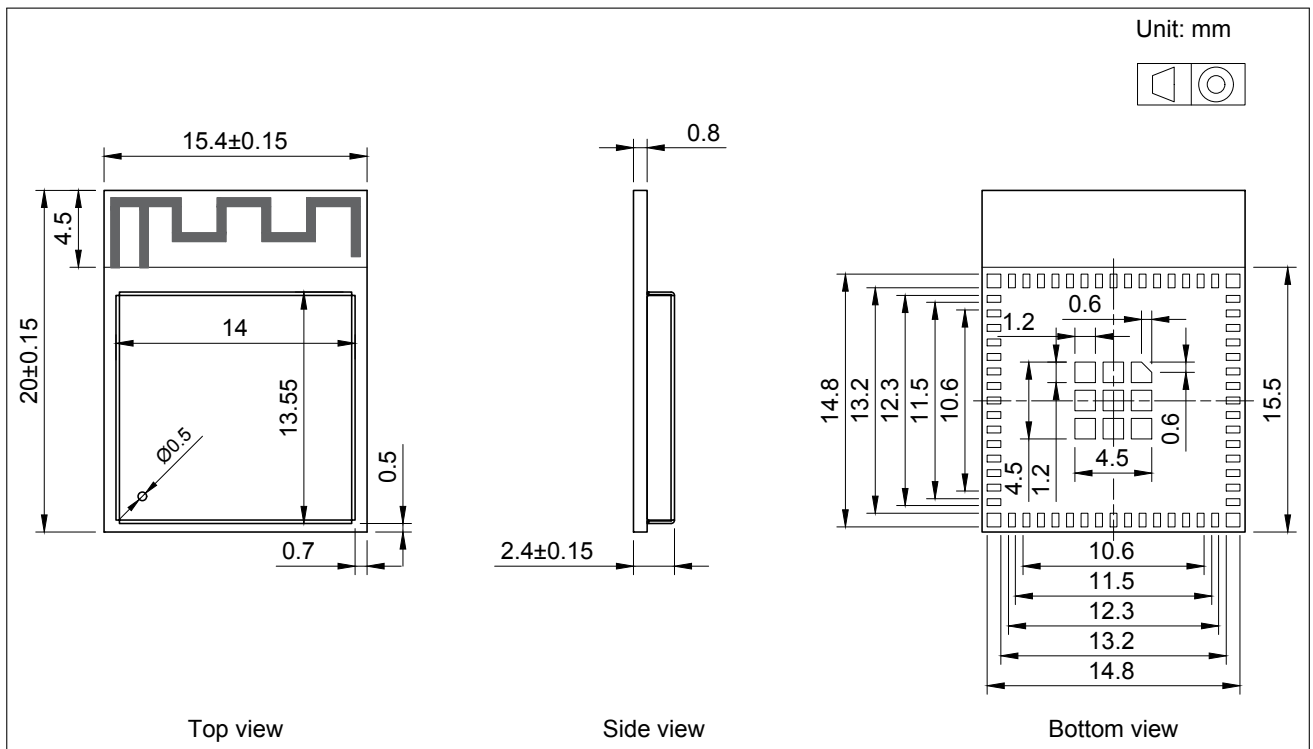


Figure 8: ESP32-S2-MINI-1 Physical Dimensions

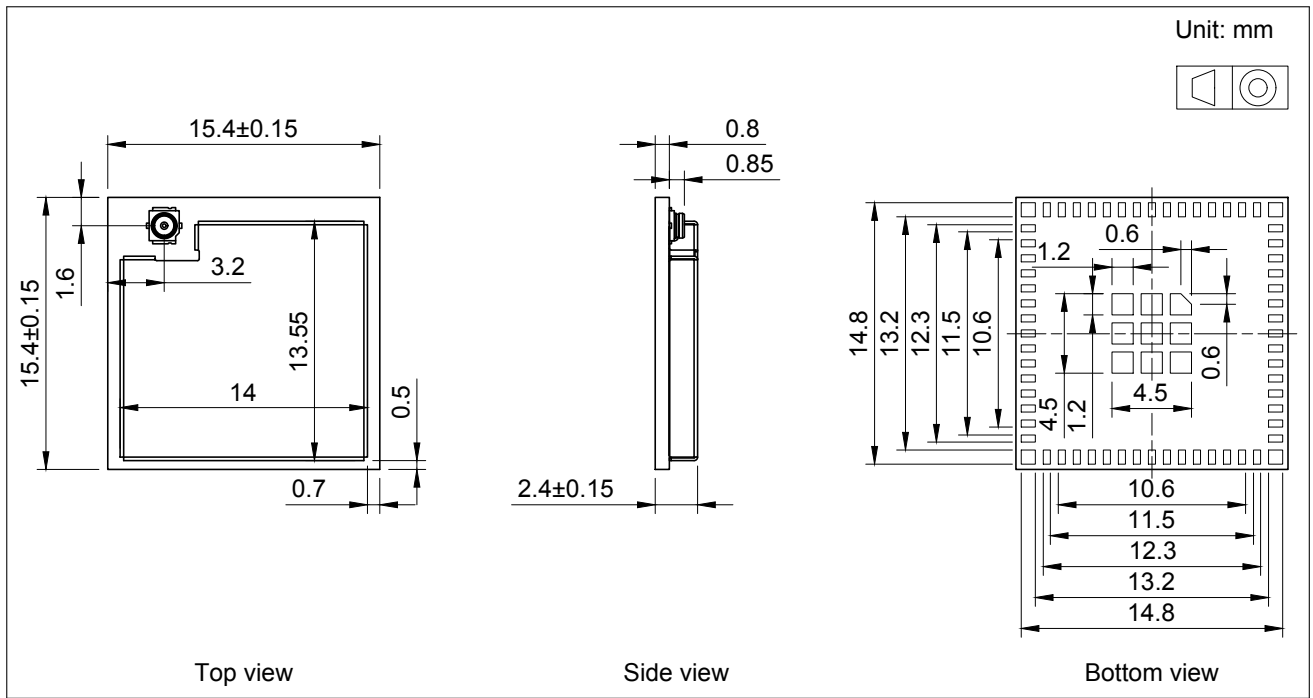


Figure 9: ESP32-S2-MINI-1U Physical Dimensions

Note:

For information about tape, reel, and product marking, please refer to [Espressif Module Package Information](#).

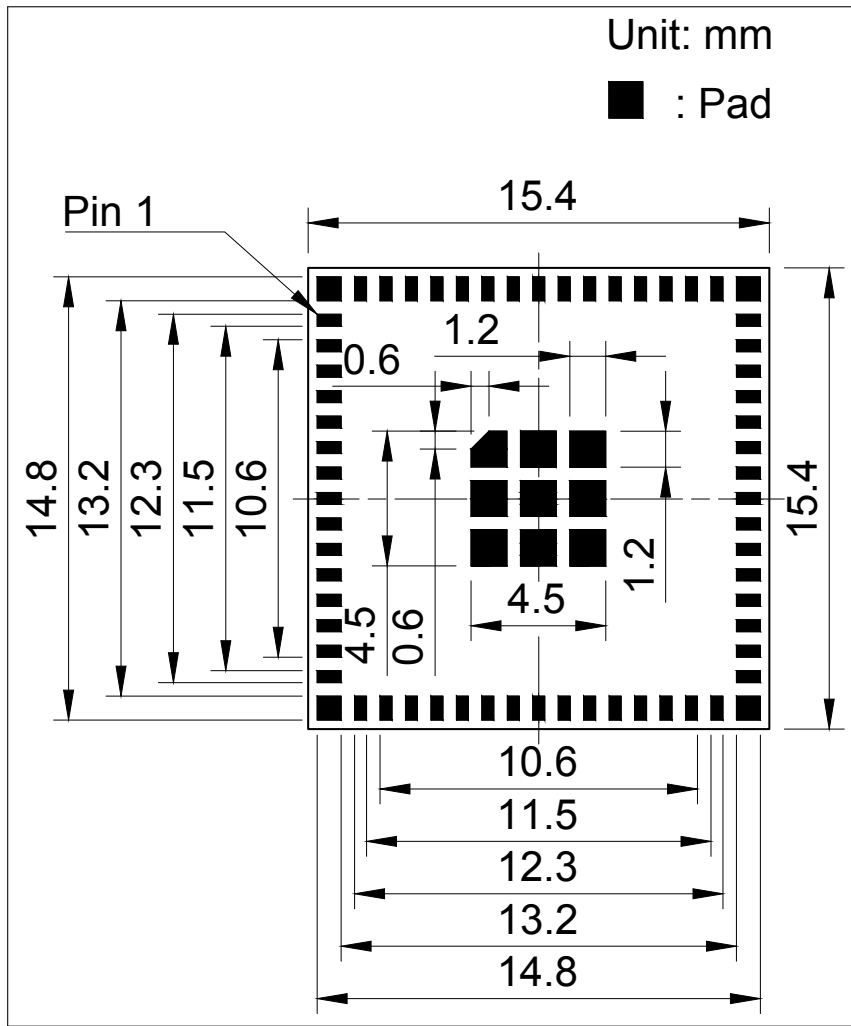


Figure 11: ESP32-S2-MINI-1U Recommended PCB Land Pattern

7.3 Dimensions of External Antenna Connector

ESP32-S2-MINI-1U uses the third generation external antenna connector as shown in Figure 12. This connector is compatible with the following connectors:

- W.FL Series connector from Hirose
- MHF III connector from I-PEX
- AMMC connector from Amphenol

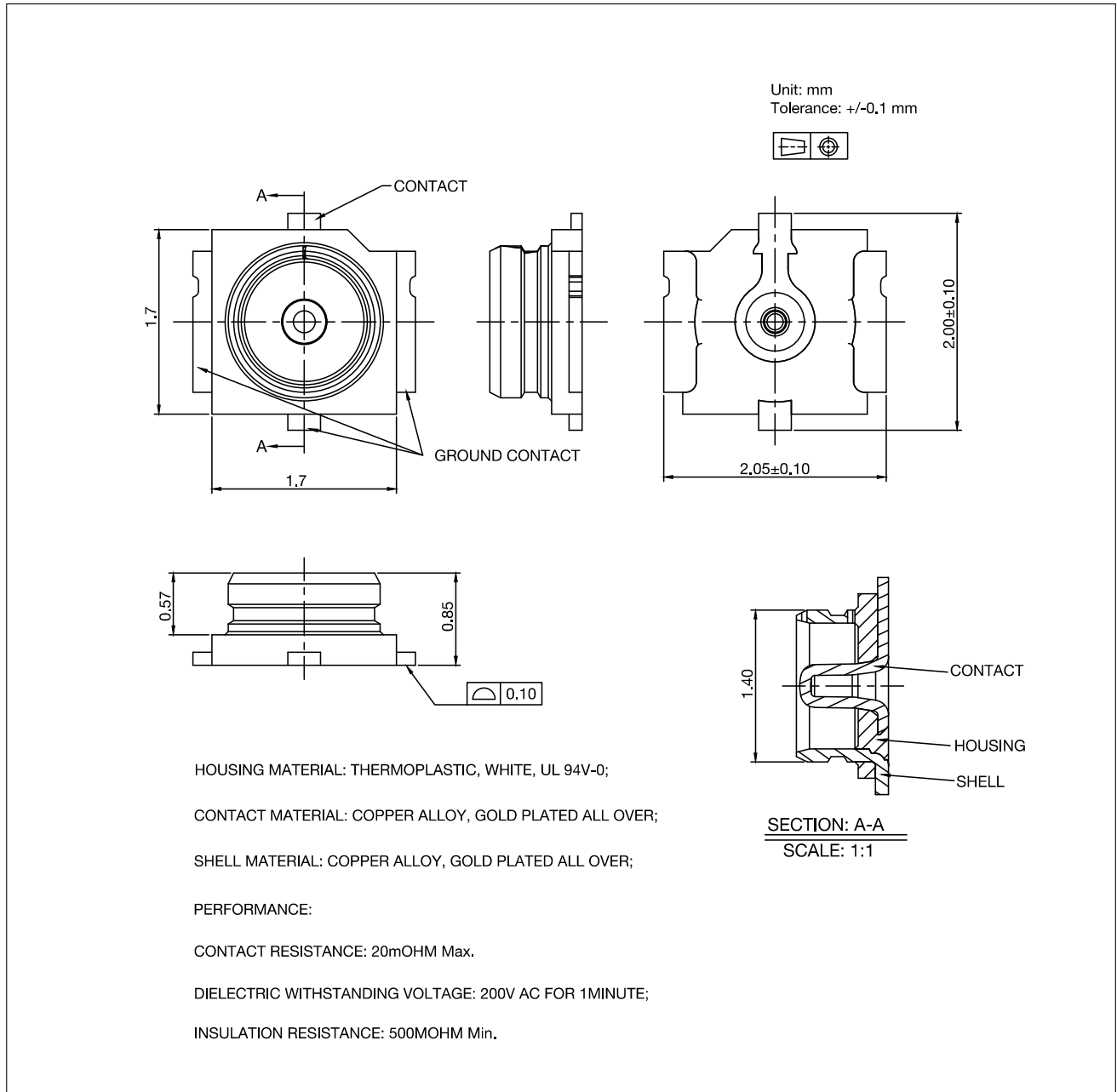


Figure 12: Dimensions of External Antenna Connector

8 Product Handling

8.1 Storage Condition

The products sealed in Moisture Barrier Bag (MBB) should be stored in a noncondensing atmospheric environment of $< 40\text{ }^{\circ}\text{C}/90\%\text{RH}$.

The module is rated at moisture sensitivity level (MSL) 3.

After unpacking, the module must be soldered within 168 hours with factory conditions $25\pm 5\text{ }^{\circ}\text{C}$ and $/60\%\text{RH}$. The module needs to be baked if the above conditions are not met.

8.2 ESD

- Human body model (HBM): 2000 V
- Charged-device model (CDM): 500 V
- Air discharge: 6000 V
- Contact discharge: 4000 V

8.3 Reflow Profile

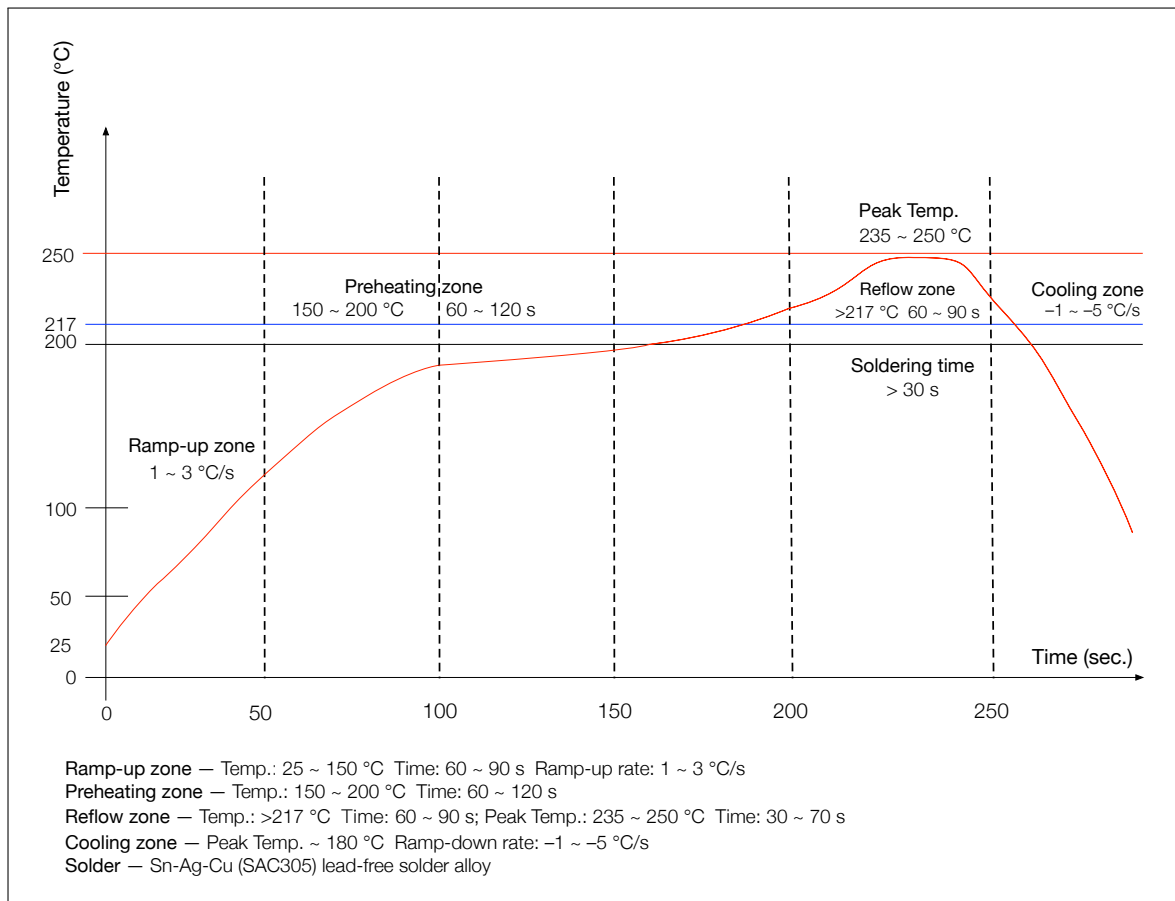


Figure 13: Reflow Profile

Note:

Solder the module in a single reflow.

9 MAC Addresses and eFuse

The eFuse in ESP32-S2 family of chips has been burnt into 48-bit `mac_address`. The actual addresses the chip uses in station or AP modes correspond to `mac_address` in the following way:

- Station mode: `mac_address`
- AP mode: `mac_address + 1`

There are seven blocks in eFuse for users to use. Each block is 256 bits in size and has independent write/read disable controller. Six of them can be used to store encrypted key or user data, and the remaining one is only used to store user data.

10 Learning Resources

10.1 Must-Read Documents

The following link provides documents related to ESP32-S2.

- [ESP32-S2 Datasheet](#)
This document provides an introduction to the specifications of the ESP32-S2 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.
- [ESP-IDF Programming Guide](#)
It hosts extensive documentation for ESP-IDF ranging from hardware guides to API reference.
- [ESP32-S2 Technical Reference Manual](#)
The manual provides detailed information on how to use the ESP32-S2 memory and peripherals.
- [Espressif Products Ordering Information](#)

10.2 Must-Have Resources

Here are the ESP32-S2-related must-have resources.

- [ESP32-S2 BBS](#)
This is an Engineer-to-Engineer (E2E) Community for ESP32-S2 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

Revision History

| Date | Version | Release notes |
|------------|---------|--|
| 2021-06-25 | V1.0 | <ul style="list-style-type: none">• Added module variants embedded with the ESP32-S2FN4R2 chip• Added module description to the title page• Updated Chapter 1 Module Overview• Added description in Section 7.3 Dimensions of External Antenna Connector• Replaced "chip family" with "chip series" following Espressif's taxonomy |
| 2020-12-17 | V0.6 | <ul style="list-style-type: none">• Added TWAI to Chapter 1 Module Overview• Updated Table 7 Current Consumption Characteristics• Updated the capacitance value of RC delay circuit to 1 μF in Chapter 6 Peripheral Schematics• Updated note in Section 8.3 Reflow Profile |
| 2020-09-23 | V0.5 | Preliminary release. |



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