AK4112B

High Feature 96kHz 24bit DIR

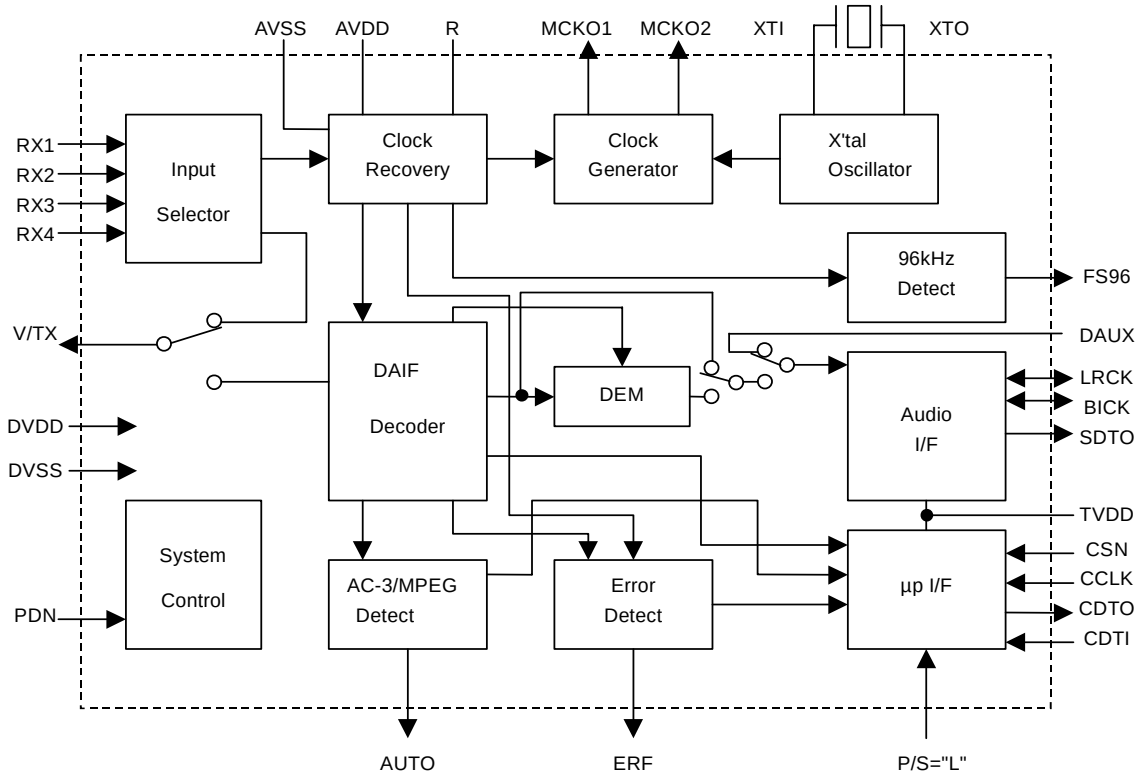
GENERAL DESCRIPTION

The AK4112B is a digital audio receiver (DIR) compatible with 96kHz, 24bits. The channel status decoding supports both consumer and professional modes. The AK4112B can automatically detect a Non-PCM bit stream. When combined with an AK4527B multi channel codec, the two chips provide a system solution for AC-3 applications. The dedicated pins or a serial µP I/F can control the mode setting. The small package, 28pin VSOP saves the board space.

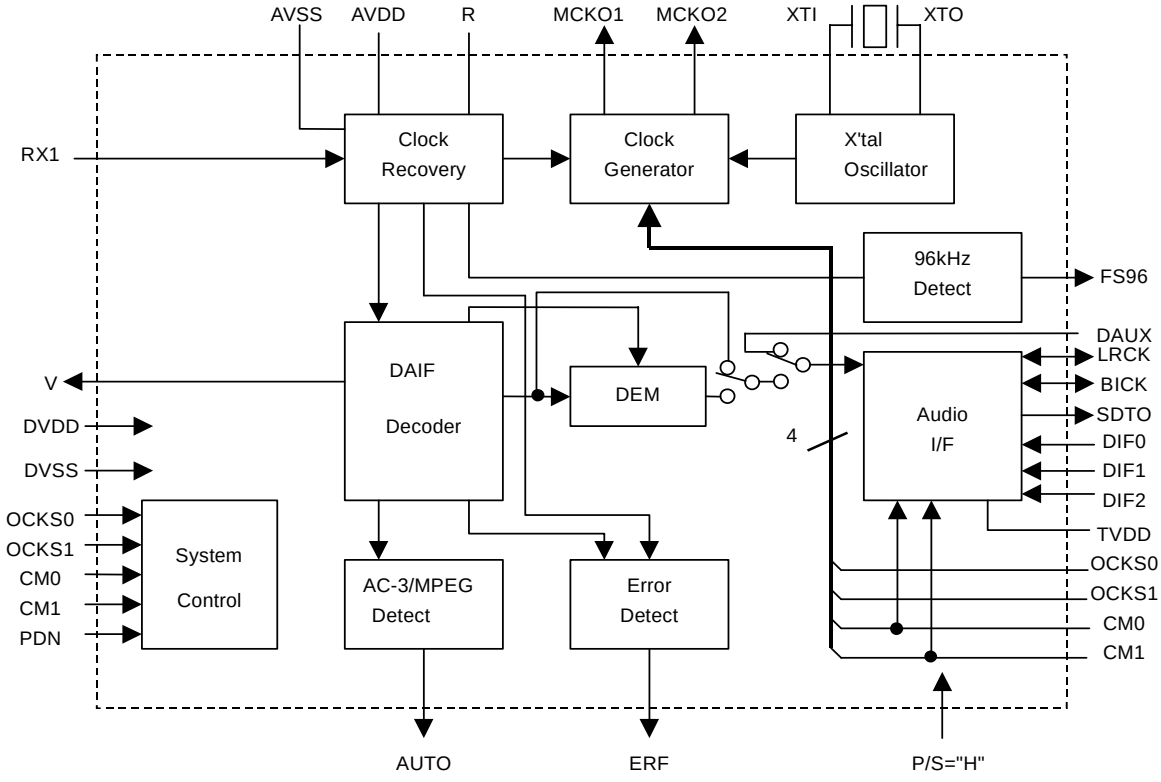
*AC-3 is a trademark of Dolby Laboratories.

FEATURES

- ☐ **Supports AES/EBU, IEC958, S/PDIF, EIAJ CP1201**
- ☐ **Low jitter Analog PLL**
- ☐ **PLL Lock Range: 22k~108kHz**
- ☐ **Clock Source: PLL or X'tal**
- ☐ **4 channel Receivers input and 1 through transmission output**
- ☐ **Auxiliary digital input**
- ☐ **De-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz**
- ☐ **Dedicated Detect Pins**
  - **- Non-PCM Bit Stream Detect Pin**
  - **- Validity Flag Detect Pin**
  - **- 96kHz Sampling Detect Pin**
  - **- Unlock & Parity Error Detect Pin**
- ☐ **Supports up to 24bit Audio Data Format**
- ☐ **Audio I/F: Master or Slave Mode**
- ☐ **32bits Channel Status Buffer**
- ☐ **Burst Preamble bit Pc, Pd Buffer for Non-PCM bit stream**
- ☐ **Serial µP I/F**
- ☐ **Two Master Clock Outputs: 128fs/256fs/512fs**
- ☐ **Operating Voltage: 2.7 to 3.6V with 5V tolerance**
- ☐ **Small Package: 28pin VSOP**
- ☐ **Ta: -40~85°C**



Serial Control Mode

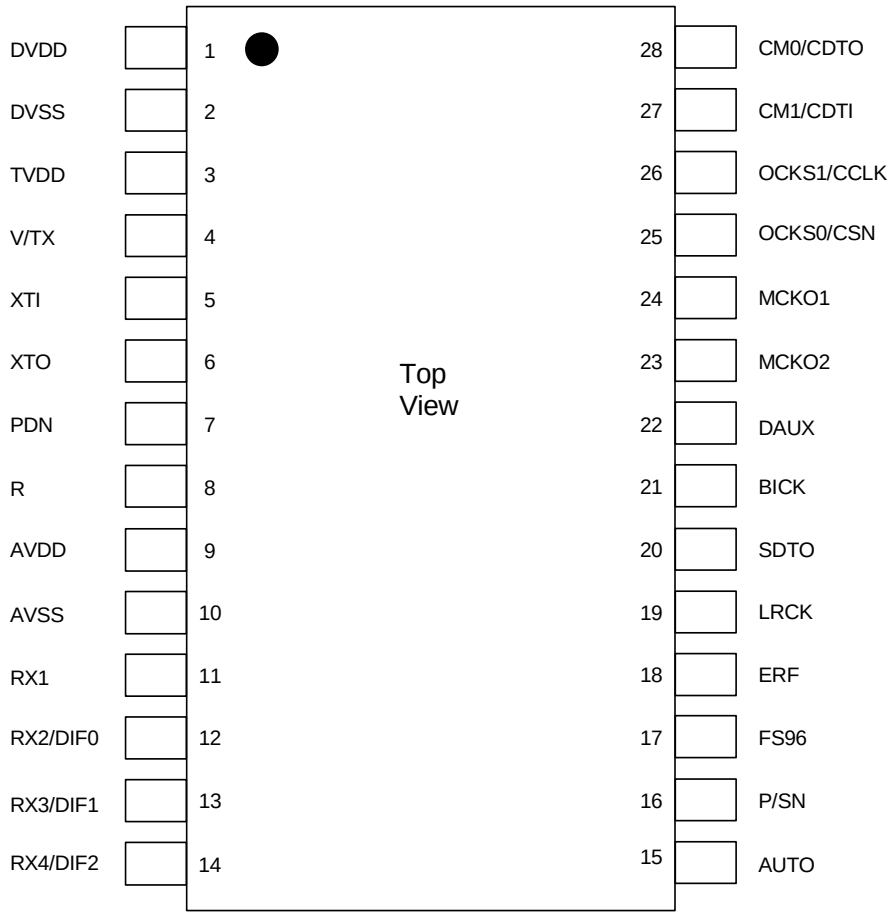


Parallel Control Mode

■ Ordering Guide

AK4112BVF	-40 ~ +85 °C	28pin VSOP (0.65mm pitch)

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVDD	-	Digital Power Supply Pin, 3.3V
2	DVSS	-	Digital Ground Pin
3	TVDD	-	Input Buffer Power Supply Pin, 3.3V or 5V
4	V	O	Validity Flag Output Pin in Parallel Mode
	TX	O	Transmit channel (through data) Output Pin in Serial Mode
5	XTI	I	X'tal Input Pin
6	XTO	O	X'tal Output Pin
7	PDN	I	Power-Down Mode Pin When "L", the AK4112B is powered-down and reset.
8	R	-	External Resistor Pin 18kΩ +/-1% resistor to AVSS externally.
9	AVDD	-	Analog Power Supply Pin
10	AVSS	-	Analog Ground Pin
11	RX1	I	Receiver Channel 1 This channel is selected in Parallel Mode or default of Serial Mode.
12	DIF0	I	Audio Data Interface Format 0 Pin in Parallel Mode
	RX2	I	Receiver Channel 2 in Serial Mode
13	DIF1	I	Audio Data Interface Format 1 Pin in Parallel Mode
	RX3	I	Receiver Channel 3 in Serial Mode
14	DIF2	I	Audio Data Interface Format 2 Pin in Parallel Mode
	RX4	I	Receiver Channel 4 in Serial Mode
15	AUTO	O	Non-PCM Detect Pin "L": No detect, "H": Detect
16	P/S	I	Parallel/Serial Select Pin "L": Serial Mode, "H": Parallel Mode
17	FS96	O	96kHz Sampling Detect Pin (RX Mode) "H": fs=88.2kHz or more, "L": fs=54kHz or less. (X'tal Mode) "H": XFS96=1, "L": XFS96=0.
18	ERF	O	Unlock & Parity Error Output Pin "L": No Error, "H": Error
19	LRCK	I/O	Output Channel Clock Pin
20	SDTO	O	Audio Serial Data Output Pin
21	BICK	I/O	Audio Serial Data Clock Pin
22	DAUX	I	Auxiliary Audio Data Input Pin
23	MCK02	O	Master Clock #2 Output Pin
24	MCK01	O	Master Clock #1 Output Pin
25	OCKS0	I	Output Clock Select 0 Pin in Parallel Mode
	CSN	I	Chip Select Pin in Serial Mode
26	OCKS1	I	Output Clock Select 1 Pin in Parallel Mode
	CCLK	I	Control Data Clock Pin in Serial Mode
27	CM1	I	Master Clock Operation Mode Pin0 in Parallel Mode
	CDTI	I	Control Data Input Pin in Serial Mode
28	CM0	I	Master Clock Operation Mode Pin1 in Parallel Mode
	CDTO	O	Control Data Output Pin in Serial Mode

Note 1: All input pins except internal pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
	Input Buffer	TVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 3)	Δ GND		0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Input Voltage (Except XTI pin)		VIN	-0.3	TVDD+0.3	V
Input Voltage (XTI pin)		VINX	-0.3	DVDD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 2: All voltages with respect to ground.
Note 3: AVSS and DVSS must be connected to the same ground.
WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V;Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	AVDD	2.7	3.3	3.6	V
	Digital	DVDD	2.7	3.3	AVDD	V
	Input Buffer	TVDD	DVDD	3.3	5.5	V

Note 2: All voltages with respect to ground.

S/PDIF RECEIVER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V;TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin		10		kΩ
Input Voltage	VTH	350			mVpp
Input Hysteresis	VHY	-	130		mV
Input Sample Frequency	fs	22	-	108	kHz

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=2.7~3.6V;TVDD=2.7~5.5V; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Power Supply Current					
Normal operation : PDN = "H" (Note 4)			20	40	mA
Power down: PDN = "L" (Note 5)			10	100	μA
High-Level Input Voltage (Except XTI pin)	VIH	70%DVDD	-	TVDD	V
High-Level Input Voltage (XTI pin)	VIH	70%DVDD	-	DVDD	V
Low-Level Input Voltage	VIL	DVSS-0.3	-	30%DVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	± 10	μA

Note 4: AVDD, DVDD=3.3V, TVDD=5.0V, C_L=20pF, fs=96kHz, X'tal=12.288MHz,
Clock Operation Mode 2, OCKS1=1, OCKS0=0.
AVDD=8mA(typ), DVDD=12mA(typ), TVDD=10μA(typ)
Note 5: RX inputs are open and all digital input pins are held DVDD or DVSS.

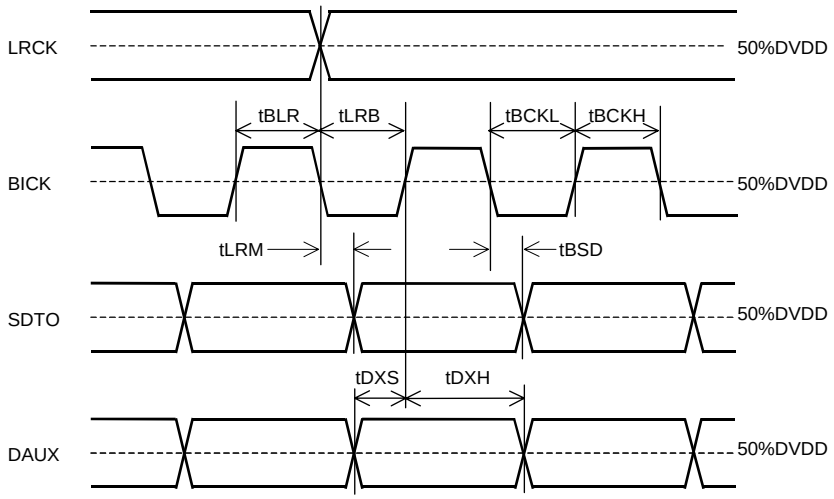
SWITCHING CHARACTERISTICS

(Ta=25°C; DVDD, AVDD2.7~3.6V, TVDD=2.7~5.5V; C_L=20pF)

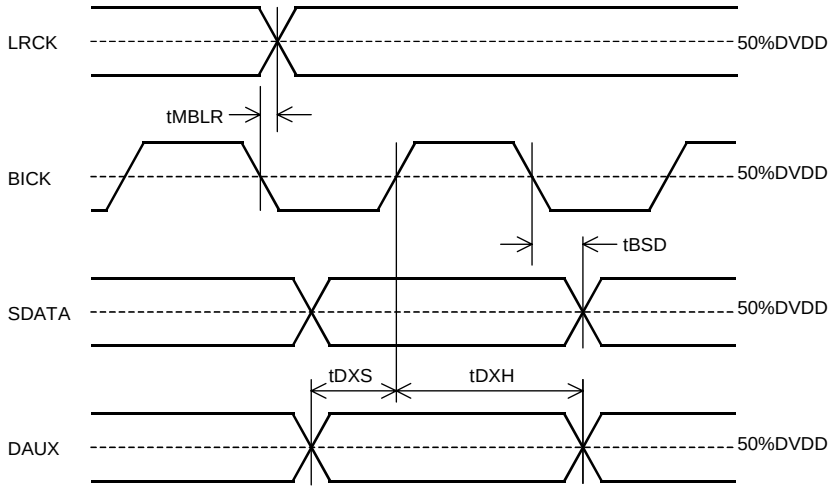
Parameter			Symbol	min	typ	max	Units
Master Clock Timing							
	Crystal Resonator	Frequency	fXTAL	11.2896		24.576	MHz
	External Clock	Frequency	fECLK	11.2896		24.576	MHz
		Duty	dECLK	40	50	60	%
	MCKO1 Output	Frequency	fMCK1	5.632		27.648	MHz
		Duty	dMCK1	40	50	60	%
	MCKO2 output	Frequency	fMCK2	2.816		27.648	MHz
		Duty	dMCK2	40	50	60	%
PLL Clock Recover Frequency (RX1-4)			fpll	22	-	108	kHz
LRCK Frequency			fs	22	48	108	kHz
Duty Cycle			dLCK	45		55	%
Audio Interface Timing							
Slave Mode							
BICK Period			tBCK	140			ns
BICK Pulse Width Low			tBCKL	60			ns
Pulse Width High			tBCKH	60			ns
LRCK Edge to BICK "↑"		(Note 6)	tLRB	30			ns
BICK "↑" to LRCK Edge		(Note 6)	tBLR	30			ns
LRCK to SDTO (MSB)			tLRM			35	ns
BICK "↓" to SDTO			tBSD			35	ns
DAUX Hold Time			tDXH	20			ns
DAUX Setup Time			tDXS	20			ns
Master Mode							
BICK Frequency			fBCK		64fs		Hz
BICK Duty			dBCK		50		%
BICK "↓" to LRCK			tMBLR	-20		20	ns
BICK "↓" to SDTO			tBSD			40	ns
DAUX Hold Time			tDXH	20			ns
DAUX Setup Time			tDXS	20			ns
Control Interface Timing							
CCLK Period			tCCK	200			ns
CCLK Pulse Width Low			tCCKL	80			ns
Pulse Width High			tCCKH	80			ns
CDTI Setup Time			tCDS	50			ns
CDTI Hold Time			tCDH	50			ns
CSN "H" Time			tCSW	150			ns
CSN "↓" to CCLK "↑"			tCSS	50			ns
CCLK "↑" to CSN "↑"			tCSH	50			ns
CDTO Delay			tDCD			45	ns
CSN "↑" to CDTO Hi-Z			tCCZ			70	ns
Reset Timing							
PDN Pulse Width			tPW	150			ns

Note 6: BICK rising edge must not occur at the same time as LRCK edge.

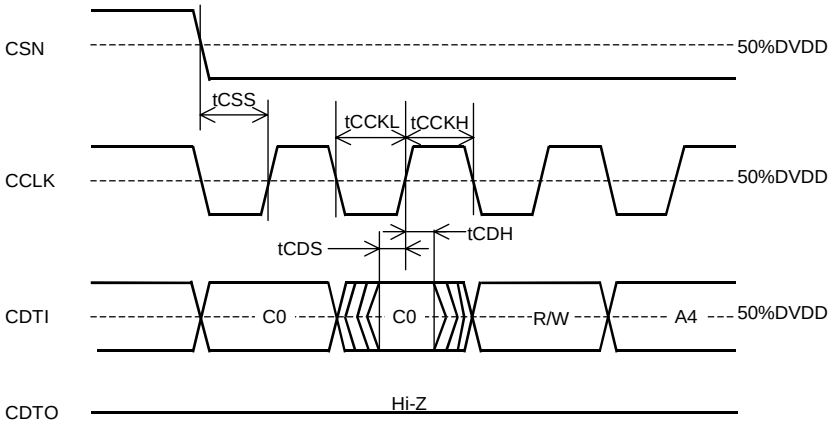
■ Timing Diagram



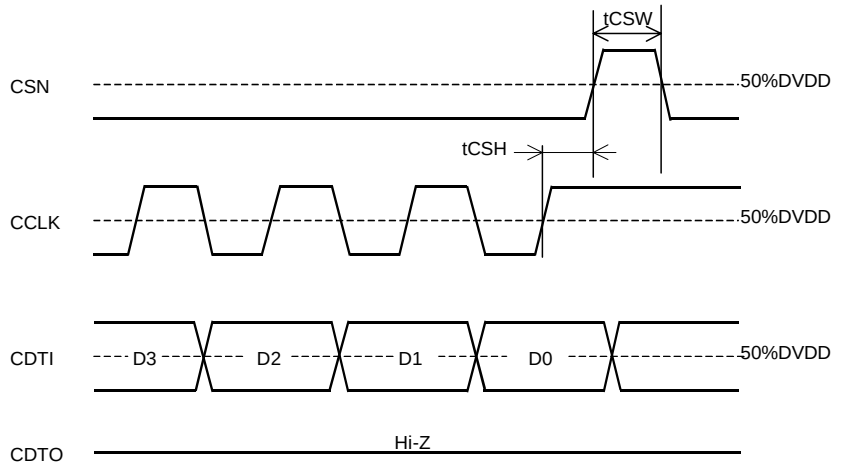
Serial Interface Timing (Slave Mode)



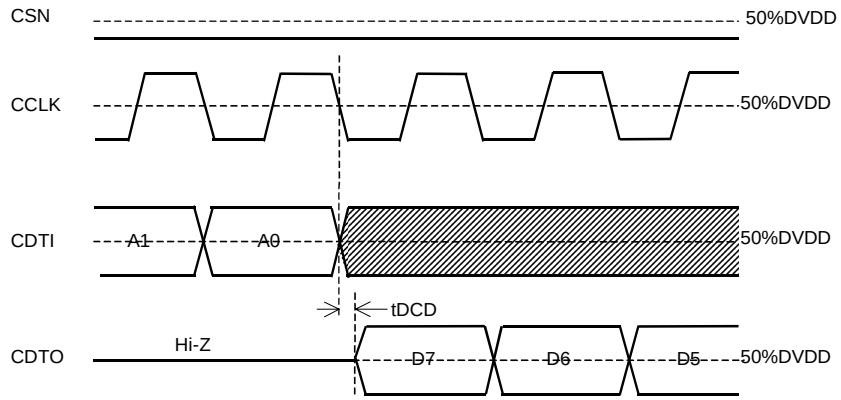
Serial Interface Timing (Master Mode)



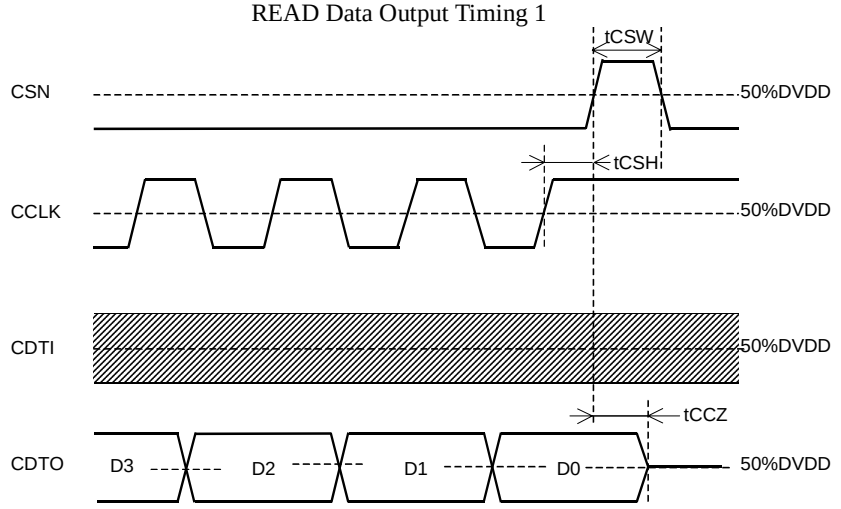
WRITE/READ Command Input Timing



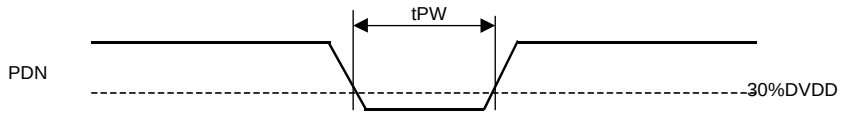
WRITE Data Input Timing



READ Data Output Timing 1



READ Data Input Timing 2



Power Down & Reset Timing

OPERATION OVERVIEW

■ Non-PCM (AC-3, MPEG, etc.) Stream Detect

The AK4112B has a Non-PCM steam auto detect function. When the 32bit mode Non-PCM preamble based on Dolby "AC-3 Data Stream in IEC958 Interface" is detected, the AUTO goes "H". The 96bit sync code consists of 0x0000, 0x0000, 0x0000, 0x0000, 0xF872 and 0x4E1F. Detection of this pattern will set the AUTO "H". Once the AUTO is set "H", it will remain "H" until 4096 frames pass through the chip without additional sync pattern being detected. When those preambles are detected, the burst preambles Pc and Pd that follow those sync codes are stored to registers 0DH-10H.

■ Clock Recovery and 96kHz Detect

On chip low jitter PLL has a wide lock range with 22kHz to 108kHz and the lock time is less than 20ms. The 96kHz detect output pin FS96 goes "H" when the sampling rate is 88.2kHz or more and "L" at 54kHz or less. In X'tal Mode, the FS96 pin outputs the value which is set by XFS96. PLL loses lock when the received sync interval is incorrect.

■ Master Clock

The AK4112B has two clock outputs, MCKO1 and MCKO2. These clocks are derived from either the recovered clock or from the X'tal oscillator. The frequencies of the master clock outputs (MCKO1 & MCKO2) are set by OCKS0 and OCKS1 as shown in Table 1. 96kHz sampling is not supported at No.2.

No.	OCKS1	OCKS0	MCKO1	MCKO2	X'tal	fs (kHz)	
0	0	0	256fs	256fs	256fs	32, 44.1, 48, 96	Default
1	0	1	256fs	128fs	256fs	32, 44.1, 48, 96	
2	1	0	512fs	256fs	512fs	32, 44.1, 48	
3	1	1	Test Mode				

Table 1. Master clock frequencies select

■ Clock Operation Mode

The CM0 and CM1 select the clock source of MCKO1/2 and the data source of SDTO via the dedicated pins or the control register. In Mode 2, the clock source is switched from PLL to X'tal when PLL goes unlock state. In Mode3, the clock source is fixed to X'tal, but PLL is also operating and the recovered data such as C bits can be monitored.

Mode	CM1	CM0	UNLOCK	PLL	X'tal	Clock source	FS96	SDTO	
0	0	0	-	ON	OFF	PLL	RFS96	RX	Default
1	0	1	-	OFF	ON	X'tal	XFS96	DAUX	
2	1	0	0	ON	ON	PLL	RFS96	RX	
			1	ON	ON	X'tal	XFS96	DAUX	
3	1	1	-	ON	ON	X'tal	XFS96	DAUX	

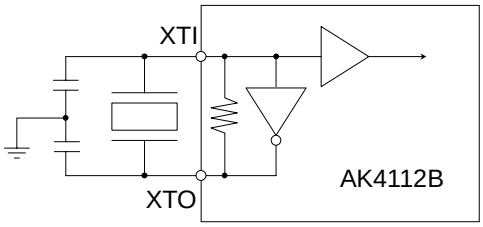
ON: Oscillation (Power-up), OFF: STOP (Power-down)

Table 2. Clock Operation Mode select

■ Clock Source

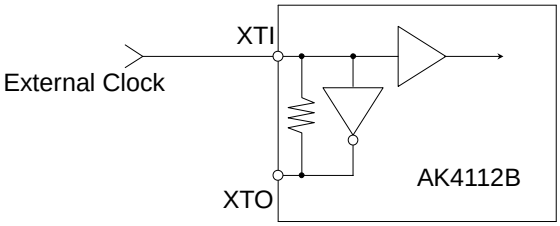
The following circuits are available to feed the clock to XTI pin (#5 pin) of AK4112B.

1) X'tal



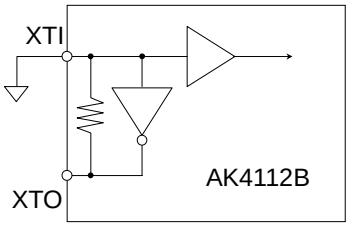
Note: External capacitance depends on the crystal oscillator (Typ. 10-40pF)

2) External clock



Note: Input clock must not exceed DVDD.

3) Fixed to the Clock Operation Mode 0



■ Sampling Frequency and Pre-emphasis Detect

The AK4112B outputs the encoded information of sampling frequency and pre-emphasis in channel status to FS0, FS1 and PEM bits in control register. These information are output from channel 1 at default. It can be switched to channel 2 by CS12 bit in control register.

FS1	FS0	fs	Byte 3 Bits 0-3
0	0	44.1kHz	0000
0	1	Reserved	all others
1	0	48kHz	0100
1	1	32kHz	1100

Table 3. fs information in Consumer Mode

FS1	FS0	fs	Byte 0 Bits 6-7
0	0	44.1kHz	10
0	1	Reserved	00
1	0	48kHz	01
1	1	32kHz	11

Table 4. fs information in Profession Mode

PEM	Pre-emphasis	Byte 0 Bits 3-5
0	OFF	≠ 0X100
1	ON	0X100

Table 5. PEM in Consumer Mode

PEM	Pre-emphasis	Byte 0 Bits 2-4
0	OFF	≠110
1	ON	110

Table 6. PEM in professional Mode

■ De-emphasis Filter Control

The AK4112B includes the digital de-emphasis filter (tc=50/15μs) by IIR filter corresponding to four sampling frequencies (32kHz, 44.1kHz, 48kHz and 96kHz). When DEAU bit="1", the de-emphasis filter is enabled automatically by sampling frequency and pre-emphasis information in the channel status. The AK4112B goes this mode at default. Therefore, in Parallel Mode, the AK4112B is always placed in this mode and the de-emphasis filter is controlled by the status bits in channel 1. In Serial Mode, DEM0/1 and DFS bits can control the de-emphasis filter when DEAU is "0". When the "0" data is input to the de-emphasis filter, the output data will be "0" or "-1". The internal de-empahsis filter is bypassed and the recovered data is output without any change if either pre-emphasis or de-emphasis Mode is OFF.

FS96	FS1	FS0	Mode
0	0	0	44.1kHz
0	0	1	OFF
0	1	0	48kHz
0	1	1	32kHz
1	0	0	OFF
1	0	1	OFF
1	1	0	96kHz
1	1	1	OFF

Table 7. De-emphasis Auto Control at DEAU="1" and PEM="1"

DFS	DEM1	DEM0	Mode	
0	0	0	44.1kHz	
0	0	1	OFF	Default
0	1	0	48kHz	
0	1	1	32kHz	
1	0	0	OFF	
1	0	1	OFF	
1	1	0	96kHz	
1	1	1	OFF	

Table 8. De-emphasis Manual Control at DEAU="0" and PEM="1"

■ System Reset and Power-Down

The AK4112B has a power-down mode for all circuits by PDN pin can be partially powerd-down by PWN bit. The RSTN bit initializes the register and resets the internal timing. In Parallel Mode, only the control by PDN pin is enabled. The AK4112B should be reset once by bringing PDN pin = "L" upon power-up.

PDN Pin (Pin #7):

All analog and digital circuit are placed in the power-down and reset mode by bringing PDN= "L". All the registers are initialized, and clocks are stopped. Reading/Witting to the register are disabled.

RSTN Bit (Address 00H; D0):

All the registers except PWN and RSTN are initialized by bringing RSTN bit = "0". The internal timings are also initialized. Witting to the register is not available except PWN and RSTN. Reading to the register is disabled.

PWN Bit (Address 00H; D1):

The clock recovery part is initialized by bringing PWN bit = "0". In this case, clocks are stopped. The registers are not initialized and the mode settings are kept. Writing and Reading to the registers are enabled.

■ Biphase Input and Through Output

Four receiver inputs (RX1-4) are available in Serial Control Mode. Each input includes amplifier corresponding to unbalance mode and can accept the signal of 350mV or more. IPS0-1 selects the receiver channel, and OPS0-1 selects the source of the bit stream driving the transmit channel (TX). The TX output can be stopped by setting TXE bit "0".

IPS1	IPS0	INPUT Data	
0	0	RX1	Default
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 9. Recovery data select

OPS1	OPS0	INPUT Data	
0	0	RX1	Default
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 10. Output data select

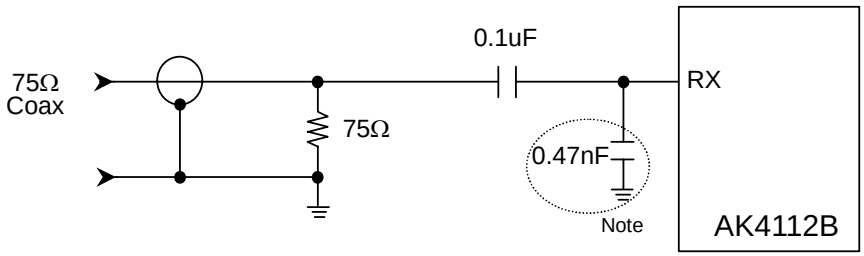


Figure 1. Consumer Input Circuit (Coaxial Input)

Note: In case of coaxial input, if a coupling level to this input from the next RX input line pattern exceeds 50mV, there is a possibility to occur an incorrect operation. In this case, it is possible to lower the coupling level by adding this decoupling capacitor.

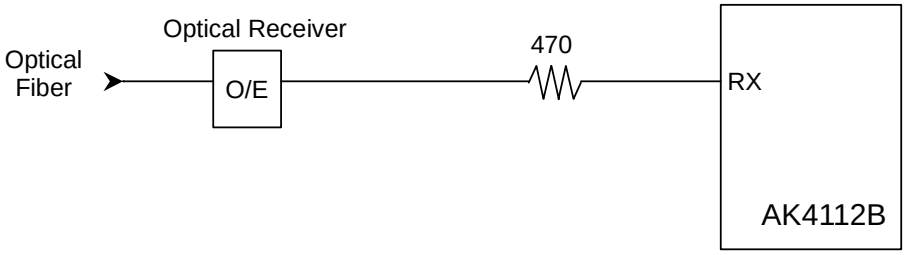
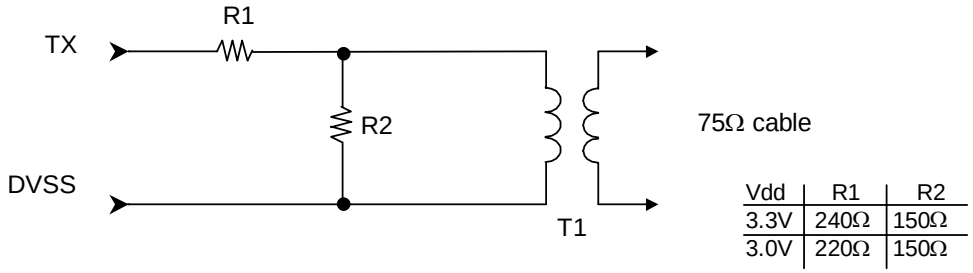


Figure 2. Consumer Input Circuit (Optical Input)

In case of coaxial input, as the input level of RX line is small, in Serial Mode, be careful not to crosstalk among RX input lines. For example, by inserting the shield pattern among them. In Parallel Mode, only one channel input (RX1) is available and RX2-4 change to other pins for audio format control. Those pins must be fixed to “H” or “L”.

The AK4112B includes the TX output buffer. The output level meets combination 0.5V+/-20% using the external resistor network. The T1 in Figure 3 is a transformer of 1:1.



Vdd	R1	R2
3.3V	240Ω	150Ω
3.0V	220Ω	150Ω

Figure 3. TX External Resistor Network

■ Error Handling

There are the following five factors which ERF pin goes “H”. ERF pin shows the status of the internal PLL operation and it is “L” when the PLL is OFF (Clock Operation Mode 1).

1. Unlock Error : “H” when the PLL goes UNLOCK state.
2. Parity Error : Updated every sub-frame cycle.
3. Biphase Error : Updated every sub-frame cycle
4. Frame length Error : Updated every sub-frame cycle
5. STC (Status Change) flag=“1” : Holds “1” until reading 03H.

In Parallel Mode, ERF pin outputs the ORed signal including the factors of 1,2,3 and 4. Once ERF pin goes ”H”, it maintains “H” for 1024/fs cycles after the all error factors are removed. Table 11 shows the state of each output pins when the ERF pin is “H”. The Frame length Error is occurred when the interval of preamble in biphase signal is incorrect. When unlock state, the channel status bits are not updated and the previous data is maintained.

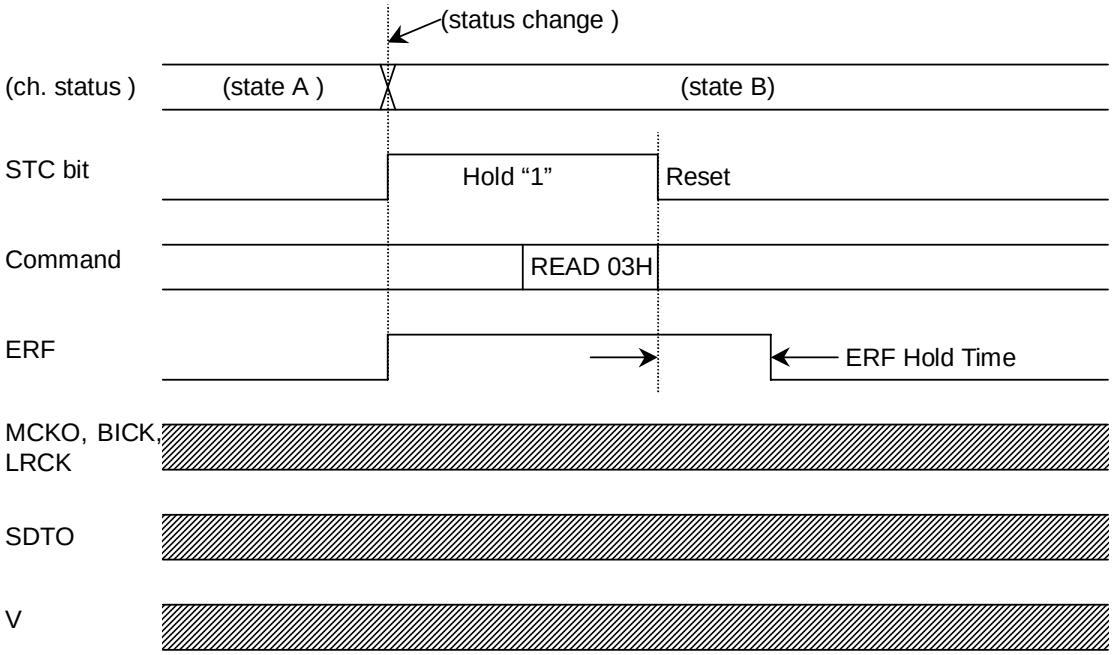
Error	AUTO	SDTO	V
Unlock Error	“L”	“L”	“L”
Parity Error	Output	Previous Data	Output
Biphase Error	Output	Previous Data	Output
Frame Length Error	Output	Previous Data	Output

Table 11. Error handling (Parallel Mode)

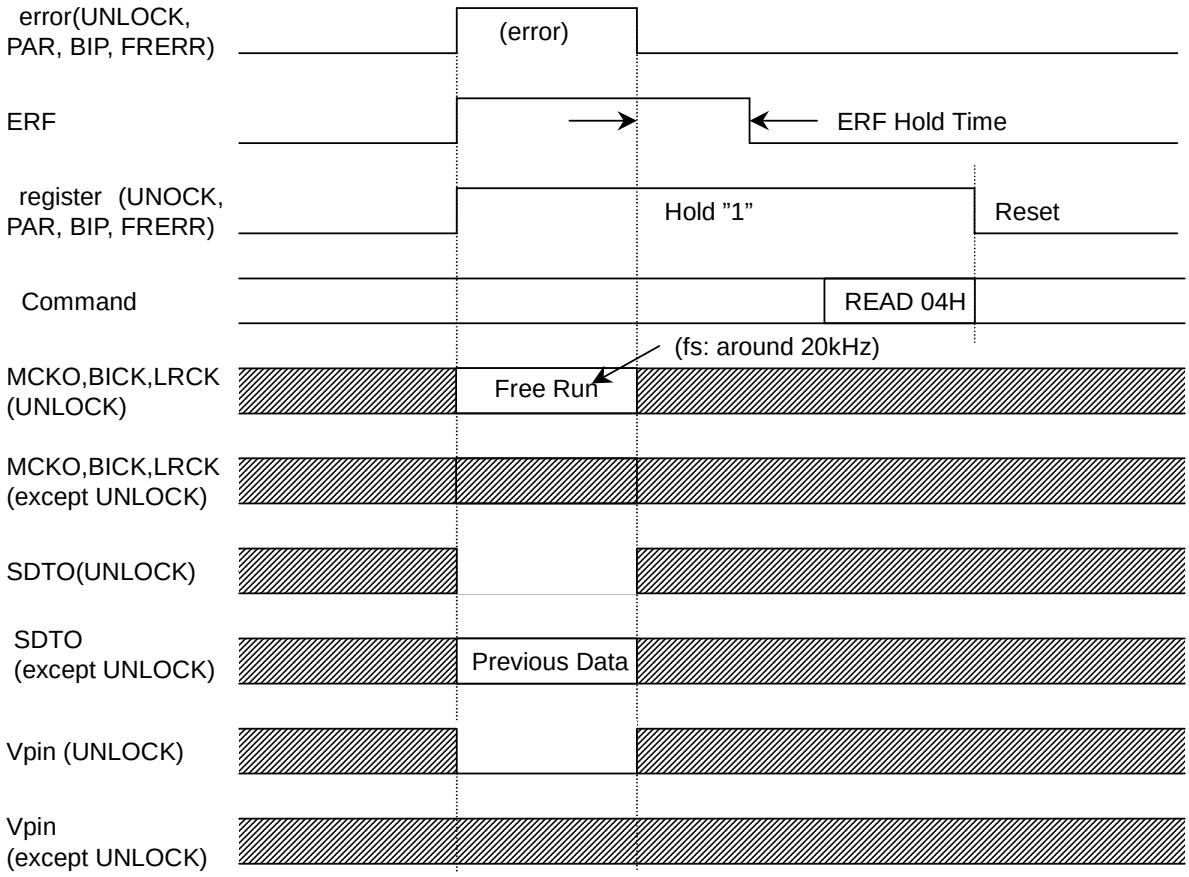
In Serial Mode, ERF pin outputs the ORed signal including the factors of 1,2,3,4 and 5. However, Parity, Biphase and Frame Length Error can be masked by MPAR bit, and the STC flag can be masked by MSTC bit. When those are masked by each bit, the error factor does not affect ERF pin operation. The STC flag is set whenever a comparison between the last sample of bits D5-0 of the receiver status 1 register (03H) and the new sample are different This comparison is made every fs cycle. The STC flag is reset by reading the register 03H. This flag is also disabled during the first block after reset.
Once ERF pin goes ”H”, it maintains “H” for 1024/fs cycles (can be changed by ERFH0-1 bits) after the all error factors (In case of STC, from STC flag “1” to reading 03H) are removed. Once PAR, BIP, FRERR, V or UNLOCK bit goes “1”, it returns “0” by reading Receiver Status 2 (04H). When unlock state, the channel status bits are not updated and the previous data is maintained.

Error & Status	Register					Pin			
	UNLOCK	PAR	BIP	FRERR	STC	AUTO	SDTO	V	TX
Unlock Error	1	0	0	0	0	“L”	“L”	“L”	Output
Parity Error	0	1	0	0	0	Output	Previous Data	Output	Output
Biphase Error	0	0	1	0	0	Output	Previous Data	Output	Output
Frame Length Error	0	0	0	1	0	Output	Previous Data	Output	Output
Status change	0	0	0	0	1	Output	Output	Output	Output

Table 12. Error handling (Serial Mode; MPAR=1, MSTC=1)



ERF pin timing at Status Change



ERF pin timing at UNLOCK, PAR, BIP, FRERR error

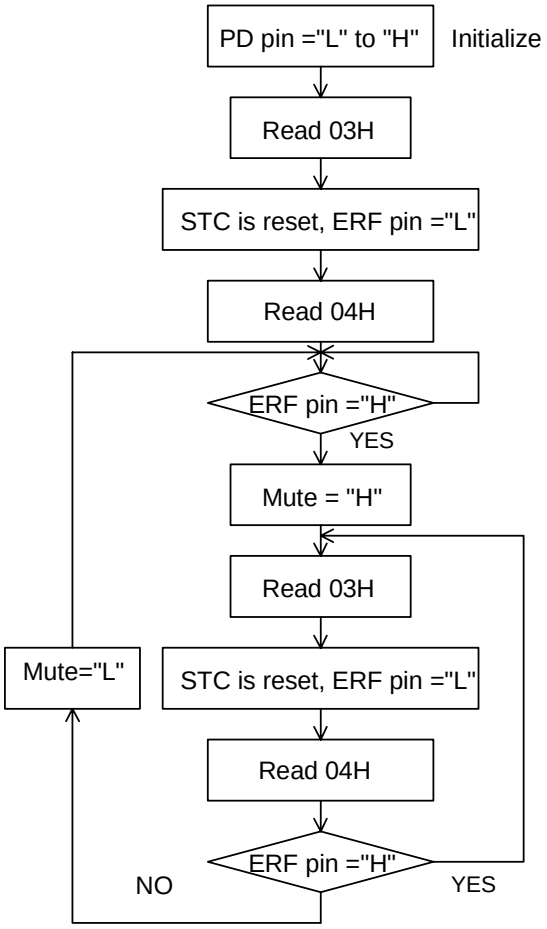


Figure 4. Error handling sequence Example

■ Audio Serial Interface Format

The DIF0, DIF1 and DIF2 pins as shown in Table 13 can select eight serial data formats. In all formats the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the DAUX is latched on the rising edge of BICK. BICK outputs 64fs clock in Mode 0-5. Mode 6-7 are Slave Modes, and BICK is available up to 128fs at fs=48kHz. In the format equal or less than 20bit (Mode0-2), LSBs in sub-frame are truncated. In Mode 3-7, the last 4LSBs are auxiliary data (see Figure 5).

When the Parity Error, Biphase Error or Frame Length Error occurs in a sub-frame, AK4112B continues to output the last normal sub-frame data from SDTO repeatedly until the error is removed. When the Unlock Error occurs, AK4112B output "0" from SDTO. In case of using DAUX pin, the data is transformed and output from SDTO. DAUX pin is used in Clock Operation Mode 1, 3 and unlock state of Mode 2.

The input data format to DAUX should be left justified except in Mode5 and 7(Table 13). In Mode5 or 7, both the input data format of DAUX and output data format of SDTO are I^2S. Mode6 and 7 are Slave Mode that is corresponding to the Master Mode of Mode4 and 5. In salve Mode, LRCK and BICK should be fed with synchronizing to MCKO1/2.

The initial state of the audio format is the Master Mode upon the power-up. Therefore, if the audio format is changed to the Slave Mode after power-up, the setting of the external clocks should be careful until completing to set the control registers.

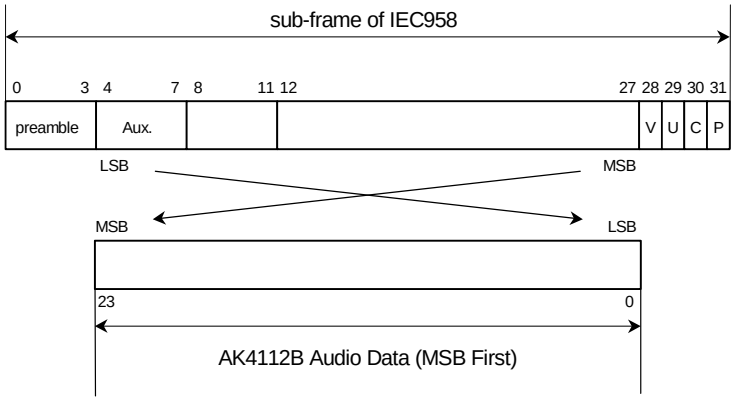


Figure 5. Bit configuration

Mode	DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
							I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 13. Audio data format

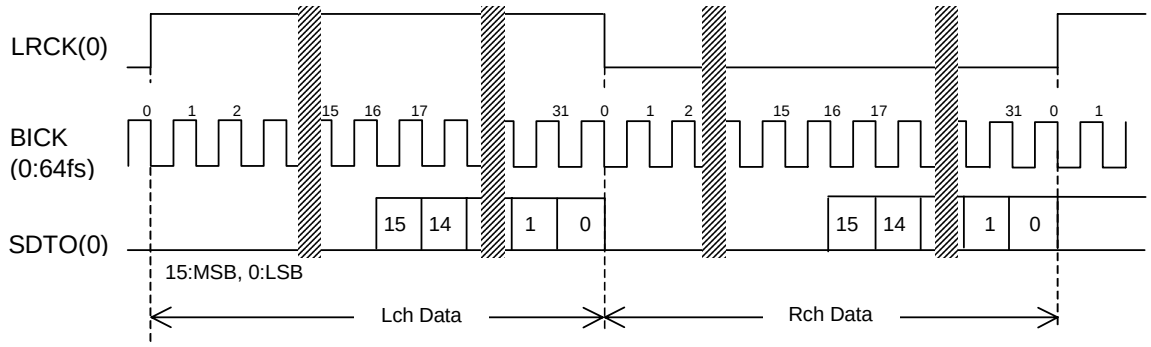


Figure 5. Mode 0 Timing

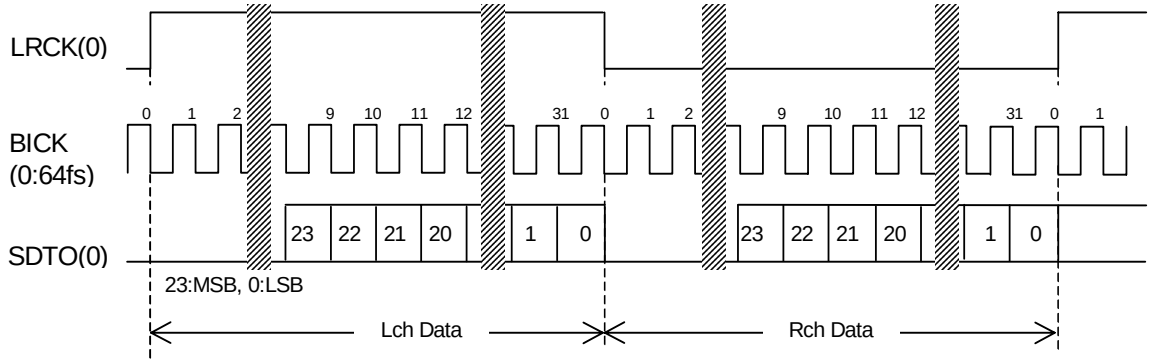


Figure 6. Mode 3 Timing

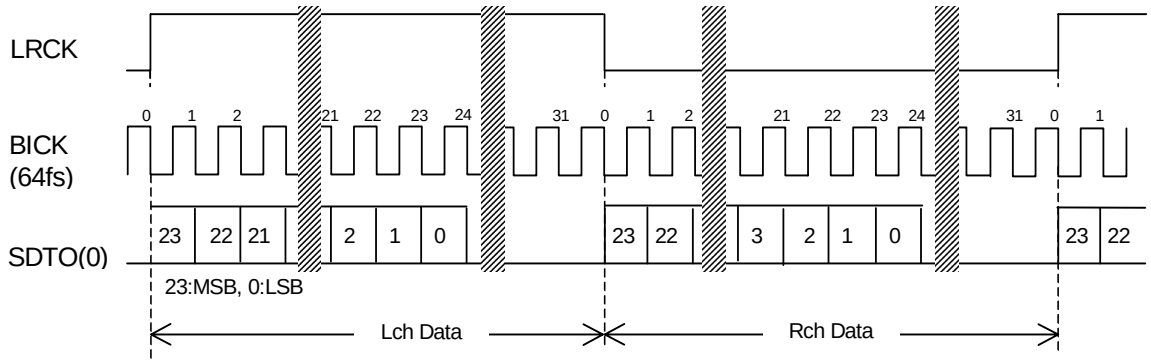


Figure 7. Mode 4, 6 Timing

Mode 4: LRCK, BICK: Output
Mode 6: LRCK, BICK: Input

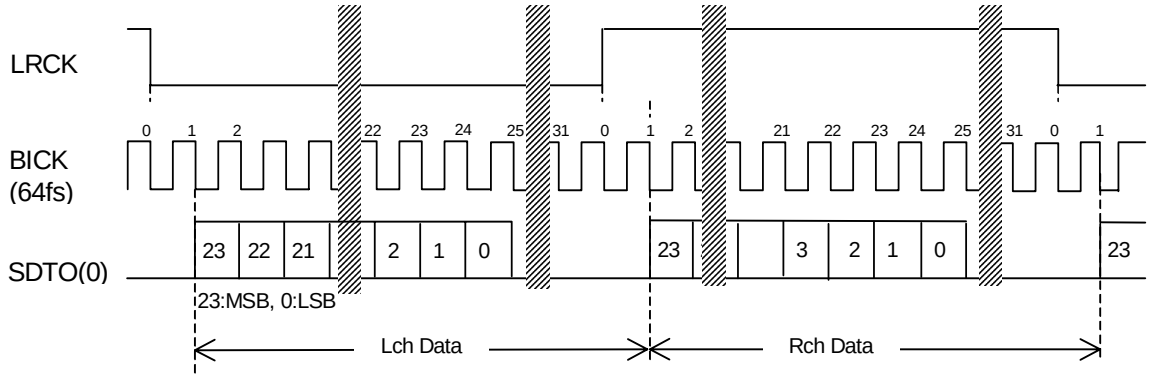
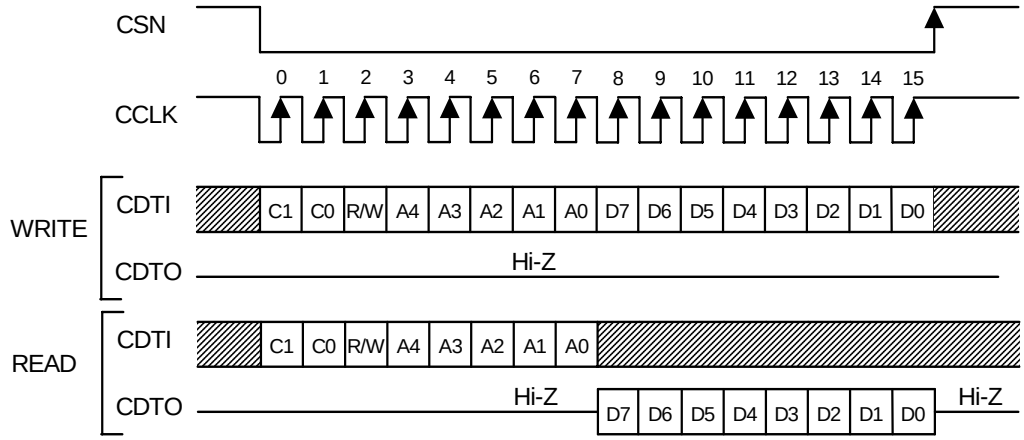


Figure 8. Mode 5, 7 Timing

Mode 5: LRCK, BICK: Output
Mode 7: LRCK, BICK: Input

■ Serial Control Interface

The internal registers may be either written or read by the 4-wire µP interface pins: CSN, CCLK, CDTI & CDTO. The data on this interface consists of Chip address (2bits, C0/1 are fixed to "00"), Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CSN. For read operations, the CDTO output goes high impedance after a low-to-high transition of CSN. The maximum speed of CCLK is 5MHz. PDN= "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4112B should be reset by PDN= "L".



C1-C0: Chip Address (Fixed to "00")
R/W: READ/WRITE (0:READ, 1:WRITE)
A4-A0: Register Address
D7-D0: Control Data

Figure 10. Control I/F Timing

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Clock & Power down Control	0	BCU	CM1	CM0	OCKS1	OCKS0	PWN	RSTN
01H	Input/Output Control	MPAR	MSTC	CS12	TXE	IPS1	IPS0	OPS1	OPS0
02H	Format & De-emphasis Control	V/TX	DIF2	DIF1	DIF0	DEAU	DEM1	DEM0	DFS
03H	Receiver status 1	ERF	0	AUDION	AUTO	PEM	FS1	FS0	RFS96
04H	Receiver status 2	CV	STC	CRC	UNLOCK	V	FRERR	BIP	PAR
05H	Channel A Status Byte 0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
06H	Channel A Status Byte 1	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
07H	Channel A Status Byte 2	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
08H	Channel A Status Byte 3	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24
09H	Channel B Status Byte 0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
0AH	Channel B Status Byte 1	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8
0BH	Channel B Status Byte 2	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
0CH	Channel B Status Byte 3	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24
0DH	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0EH	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
0FH	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
10H	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
11H	Count Control	0	0	0	0	0	EFH1	EFH0	XFS96

Notes:

For addresses from 12H to 1FH, data must not be written.
When PDN pin goes “L”, the registers are initialized to their default values.
When RSTN bit goes “0”, the internal timing is reset and the registers are initialized to their default values.
All data can be written to the register even if PWN bit is “0”.

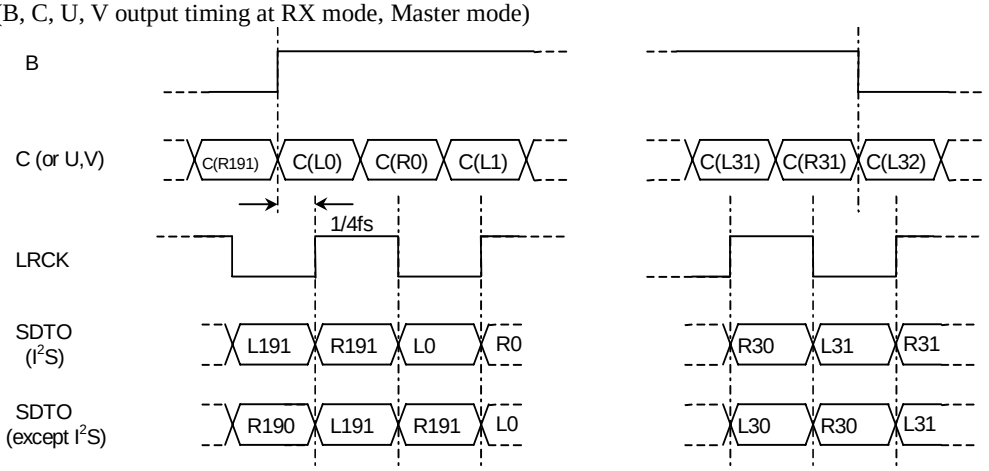
■ Register Definitions

Reset & Initialize

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Clock & Power down Control	0	BCU	CM1	CM0	OCKS1	OCKS0	PWN	RSTN
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
default		0	0	0	0	0	0	1	1

RSTN: Timing Reset & Register Initialize
0: Reset & Initialize
1: Normal Operation
PWN: Power Down
0: Power down
1: Normal Operation
OCKS1-0: Master Clock frequency Select
CM1-0: Master Clock Operation Mode Select
BCU: Block start & C/U output Mode
When BCU=1, the 3 output pins change another function.
MCKO2 pin→ B; block start signal
AUTO pin→ C bit
FS96 pin→ U bit
The block signal goes high at the start of frame 0 and remains high until the end of frame 31.

(B, C, U, V output timing at RX mode, Master mode)



Input/Output Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Input/Output Control	MPAR	MSTC	CS12	TXE	IPS1	IPS0	OPS1	OPS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
default		1	0	0	1	0	0	0	0

OPS1-0: Output Through Data Select
IPS1-0: Input Recovery Data Select
TXE: TX Output Enable
0: Disable. TX output pin is placed in a high impedance state.
1: Enable
CS12: Channel Status Select
0: Channel 1
1: Channel 2
Selects which channel status is used to derive AUDION, PEM, FS1 and FS0.
The de-emphasis filter, however, is always controlled by channel 1 in the Parallel Mode.
MSTC: Status change flag mask bit
This bit is low to mask status change from being reported by ERF.
MPAR: Parity mask bit
This bit is low to mask Parity Error, Biphase Error and Frame Length Error from being reported by ERF.

Format & De-emphasis Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Format & De-emphasis Control	V/TX	DIF2	DIF1	DIF0	DEAU	DEM1	DEM0	DFS
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
default		0	1	0	0	1	0	1	0

V/TX: V/TX Output Select
0: Validity Flag Output. This output is updated every fs cycle.
1: TX
DFS: 96kHz De-emphasis Control
DEM1-0: 32, 44.1, 48kHz De-emphasis Control
DEAU: De-emphasis Auto Detect Enable
0: Disable
1: Enable
DIF2-0: Audio Data Format Control

Receiver Status 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Receiver status 1	ERF	0	AUDION	AUTO	PEM	FS1	FS0	RFS96
R/W		RD	RD	RD	RD	RD	RD	RD	RD
default		0	0	0	0	0	0	0	0

RFS96: 96kHz Sampling Detect at Recovery Mode.
0: fs=54kHz or less.
1: fs=88.2kHz or more

FS1-0: Sampling Frequency Output

PEM: Pre-emphasis Output
0: OFF
1: ON
This bit is made by encoding channel status bits.

AUTO: Non-PCM Auto Detect
0: No detect
1: Detect
This function is the same as AUTO pin.

AUDION: Audio bit Output
0: Audio
1: Non Audio

ERF: Unlock or Parity Error or Status change
0: No Error or No change
1: Error or Change
This function is the same as ERF pin. This bit goes "1" when Unlock Error, Parity Error, Biphase Error, Frame Length Error or Status Change occurs. If MPAR=0 & MSTC=0, only an unlock error is reported.

Receiver Status 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Receiver status 2	CV	STC	CRC	UNLOCK	V	FRERR	BIP	PAR
R/W		RD	RD	RD	RD	RD	RD	RD	RD
default		0	0	0	0	0	0	0	0

PAR: Parity Status (0:No Error, 1:Error)
It is high if Parity Error is detected in the sub-frame. PAR is unaffected by the state of MPAR.

BIP: Biphase Status (0:No Error, 1:Error)

FRERR: Frame Error Status (0:No Error, 1:Error)

V: Validity bit (0:No Error, 1:Error)

UNLOCK: PLL Lock status (0:Lock, 1:Unlock)

CRC: Cyclic Redundancy Check (0:No Error, 1:Error on either channel)

STC: Status change flag of Receiver status 1 (0:No change, 1:change)
This flag goes "H" when the latest value of D5-0 in Receiver Status 1(03H) is different from the previous value. This comparison is made at every fs cycle. This bit returns to "L" by reading Receiver Status 1(03H). The flag is disabled during the first block after Reset.

CV: Channel Status Validity (0:Valid, 1:Not Valid, data is updating)
This signal goes "H" at the start of frame 0 and maintains "H" until the end of frame 31.

Channel Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Channel A Status Byte 0	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
06H	Channel A Status Byte 1	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8
07H	Channel A Status Byte 2	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
08H	Channel A Status Byte 3	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24
09H	Channel B Status Byte 0	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
0AH	Channel B Status Byte 1	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8
0BH	Channel B Status Byte 2	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
0CH	Channel B Status Byte 3	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24
R/W		RD							
default		Not initialized							

CA31-0: Channel A Status Byte 4-1
CB31-0: Channel B Status Byte 4-1
Bit definition changes depending upon PRO bit setting. When CV=1, these bits are updating and may be invalid.

Burst Preamble Pc/Pd in non-PCM encoded Audio bitstreams

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Burst Preamble Pc Byte 0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0EH	Burst Preamble Pc Byte 1	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
0FH	Burst Preamble Pd Byte 0	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
10H	Burst Preamble Pd Byte 1	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
R/W		RD							
default		Not initialized							

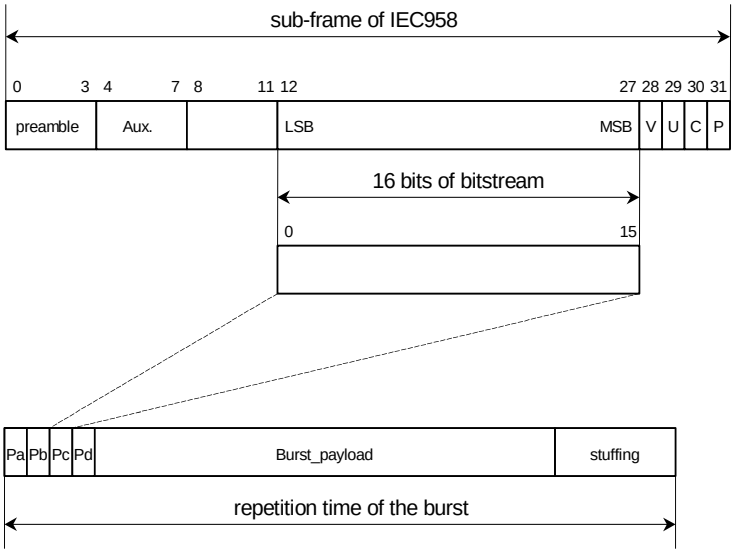
PC15-0: Burst Preamble Pc Byte 1, 0
PD15-0: Burst Preamble Pd Byte 1, 0

Count Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Count Control	0	0	0	0	0	EFH1	EFH0	XFS96
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
default		0	0	0	0	0	0	1	0

XFS96: FS96 output select at X'tal Mode (clock Operation Mode1, Mode3 and Unlock state of Mode2)
1: FS96pin="H"
0: FS96pin="L"
EFH1-0: Error Flag Hold Count Select
00: 512 LRCK
01: 1024 LRCK
10: 2048 LRCK
11: 4096 LRCK

■ Burst preambles in non-PCM bitstreams



Preamble word	Length of field	Contents	value
Pa	16 bits	sync word 1	0xF872
Pb	16 bits	sync word 2	0x4E1F
Pc	16 bits	Burst info	see Table 15.
Pd	16 bits	Length code	numbers of bits

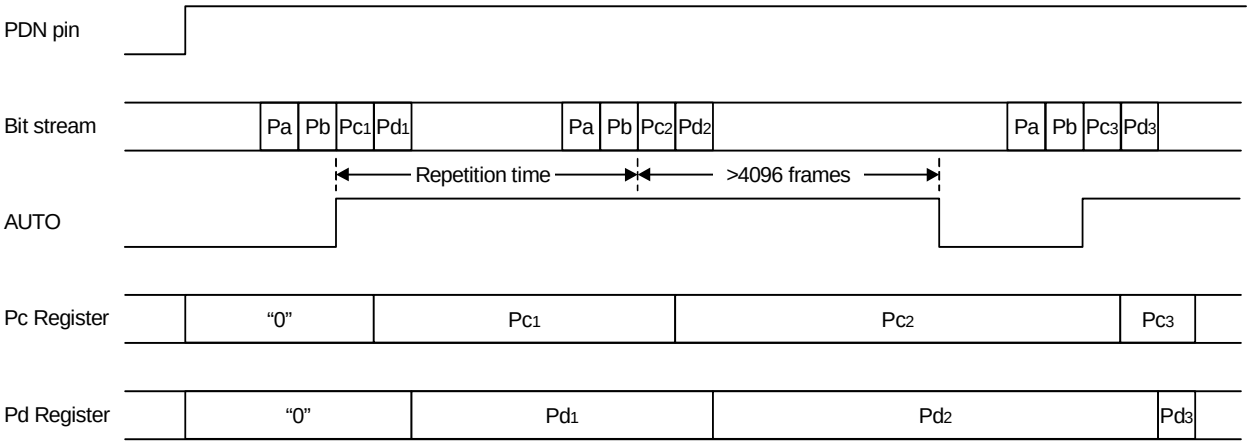
Table 14. Burst preamble words

Bits of Pc	value	contents	repetition time of burst in IEC958 frames
0-4		data type	
	0	NULL data	≤4096
	1	Dolby AC-3 data	1536
	2	reserved	
	3	PAUSE	
	4	MPEG-1 Layer1 data	384
	5	MPEG-1 Layer2 or 3 data or MPEG-2 without extension	1152
	6	MPEG-2 data with extension	1152
	7	MPEG-2 AAC ADTS	1024
	8	MPEG-2, Layer1 Low sample rate	384
	9	MPEG-2, Layer2 or 3 Low sample rate	1152
	10	reserved	
	11	DTS type I	512
	12	DTS type II	1024
	13	DTS type III	2048
	14	ATRAC	512
	15	ATRAC2/3	1024
	16-31	reserved	
5, 6	0	reserved, shall be set to “0”	
7	0	error-flag indicating a valid burst_payload	
	1	error-flag indicating that the burst_payload may contain errors	
8-12		data type dependent info	
13-15	0	bit stream number, shall be set to “0”	

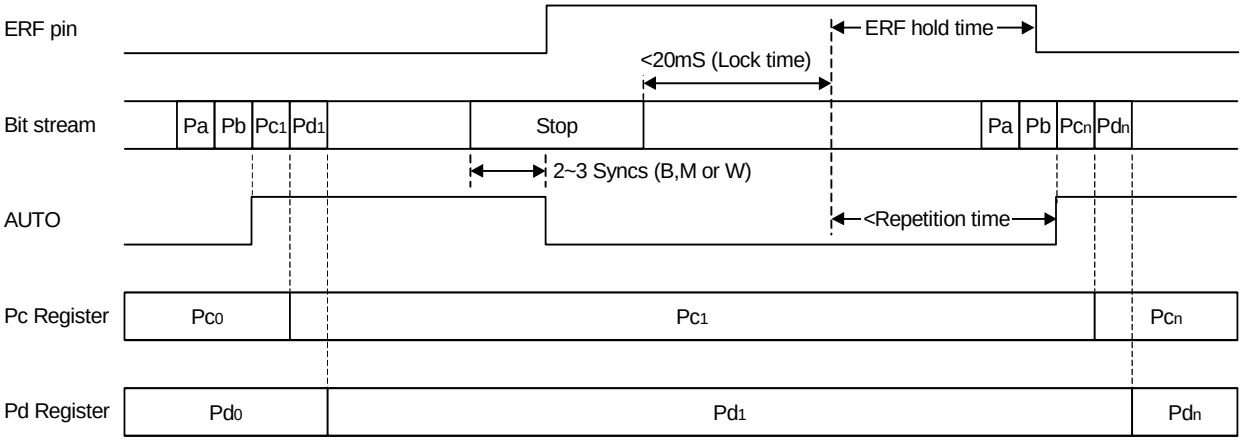
Table 15. Fields of burst info Pc

■ Non-PCM Bitstream timing

1) When Non-PCM preamble is not coming within 4096 frames,



2) When Non-PCM bitstream stops



SYSTEM DESIGN

Figure 11 shows the example of system connection diagram for Serial Mode.

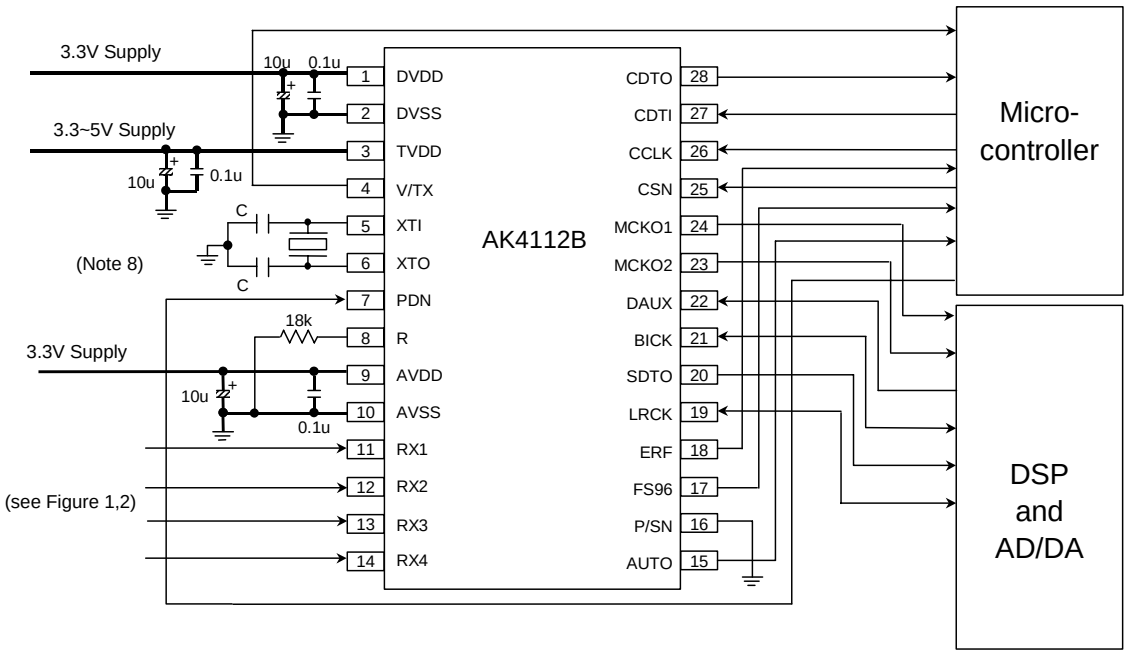


Figure 11. Typical Connection Diagram (Serial Mode)

Notes:

- "C" depends on the crystal oscillator (Typ. 10-40pF)
- AVSS and DVSS must be connected the same ground plane
- Digital signals, especially clocks, should be kept away from the R pin in order to avoid an effect to the clock jitter performance.

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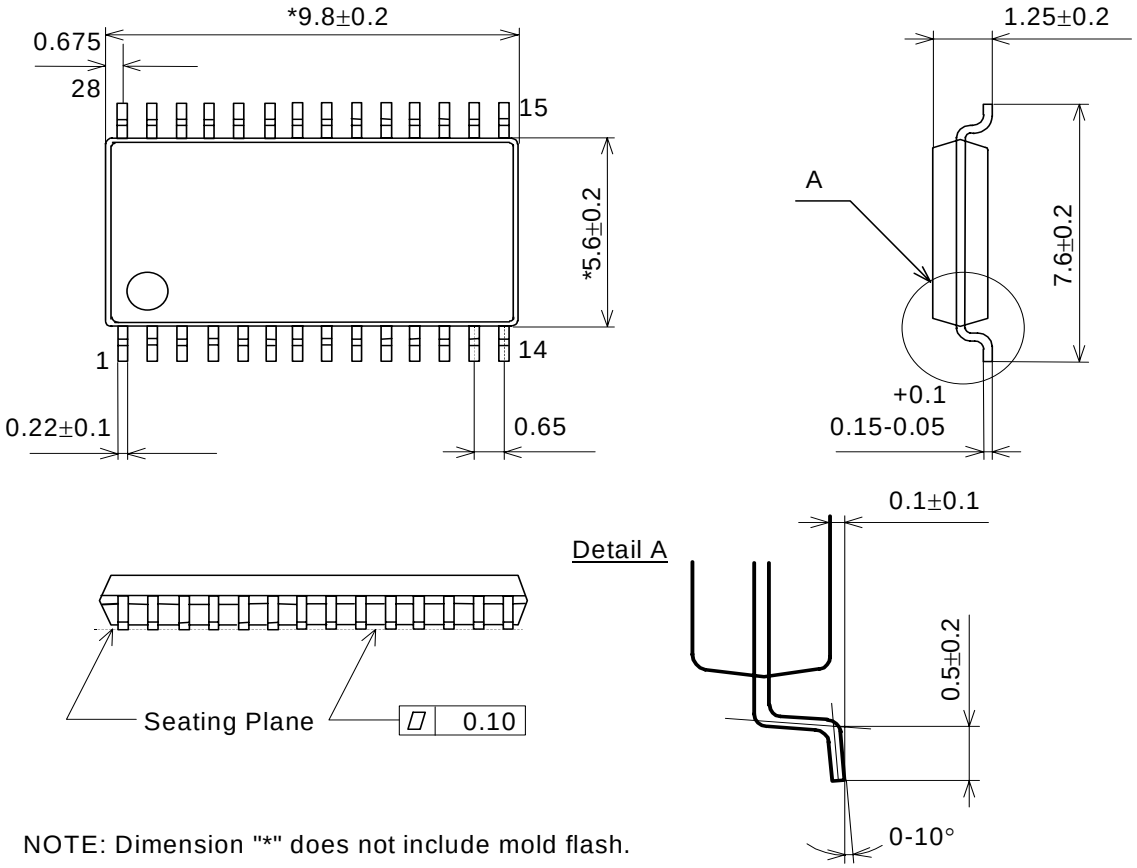
PACKAGE

28pin VSOP (Unit: mm)

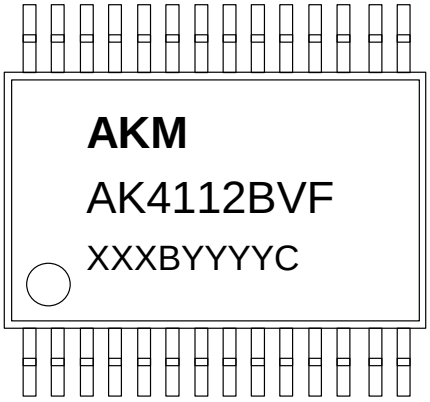


NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



XXXXBYYYYC:	Date code identifier
XXXB:	Lot number (X : Digit number, B : Alpha character)
YYYYC:	Assembly date (Y : Digit number C : Alpha character)