CUSTOMER ADVISORY
ADV2143

Intel® MAX®10 Device Pin Connection Guidelines Update

Description:

Intel® is notifying customers of an update to the MAX® 10 Device Family Pin Connection Guidelines. Below is the update listed in the MAX 10 Device Family Pin Connection Guidelines.

- Updated the 1.0-V VCCIO note in the connection guidelines of the VCCIO [#] pins in the Intel MAX 10 (Single Supply) FPGA and Intel MAX 10 (Dual Supply) FPGA.

The updated MAX 10 Device Family Pin Connection Guidelines can be found here: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/dp/max-10/pcg-01018.pdf

Recommended Actions:

Customers are requested to take note of the changes and determine the impact on their designs.

For questions or support, please contact your local Field Applications Engineer (FAE), or submit a question or request at the My Intel support page, log-in via: https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected:

All MAX 10 devices.

The list of affected part numbers (OPNs) can be downloaded in Excel form:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2143-opn-list.xlsx

Change Implementation:

Table 1

Milestone	Availability
Availability of MAX 10 Device Pin Connection Guidelines Update	Now

Contact:

For more information, please contact your local Field Applications Engineer (FAE), or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Customer Notifications Subscription:

Customers that subscribe to the Intel FPGA customer notification mailing list will receive the notifications automatically via email.

If you would like to receive Intel FPGA customer notifications by email, you can register to the Intel FPGA program and set up your subscription at:
https://www.intel.com/content/www/us/en/programmable/my-intel/malemailsub/technical-updates.html

Revision History

Date	Rev	Description
12/03/2021	1.0.0	Initial Release