Integrated Circuit Systems, Inc.

ICS9148-02

Pentium/Pro™ System Clock Chip

General Description

The **ICS9148-02** is a Clock Synthesizer chip for Pentium and PentiumPro CPU based Desktop/Notebook systems that will provide all necessary clock timing.

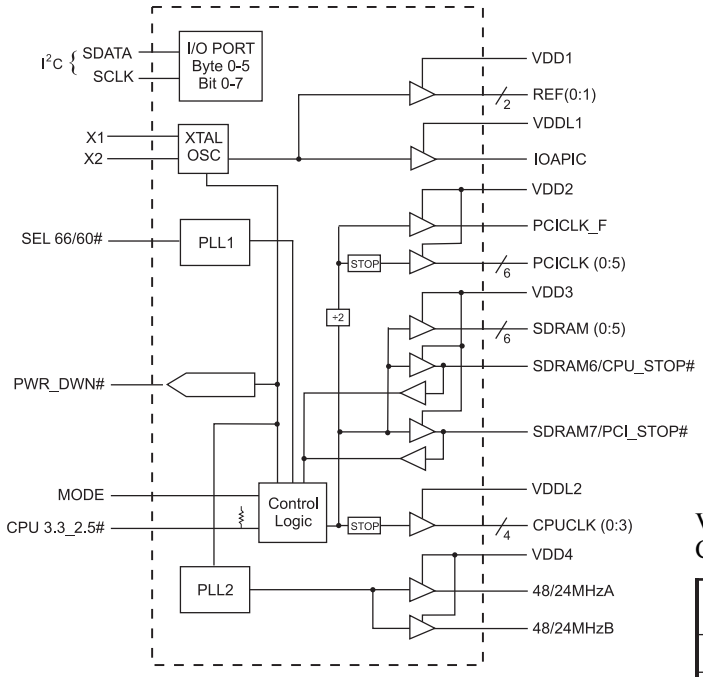
Features include four CPU, seven PCI and eight SDRAM clocks. Two reference outputs are available equal to the crystal frequency. Additionally, the device meets the Pentium power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up.

PWR_DWN# pin allows low power mode by stopping crystal OSC and PLL stages. For optional power management, CPU_STOP# can stop CPU (0:3) clocks and PCI_STOP# will stop PCICLK (0:5) clocks. CPU and IOAPIC output buffer strength controlled by CPU 3.3_2.5# pin to match VDDL voltage.

High drive CPUCLK outputs typically provide greater than 1 V/ns slew rate into 20pF loads. PCICLK outputs typically provide better than 1V/ns slew rate into 30pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

The **ICS9148-02** accepts a 14.318MHz reference crystal or clock as its input and runs on a 3.3V core supply.

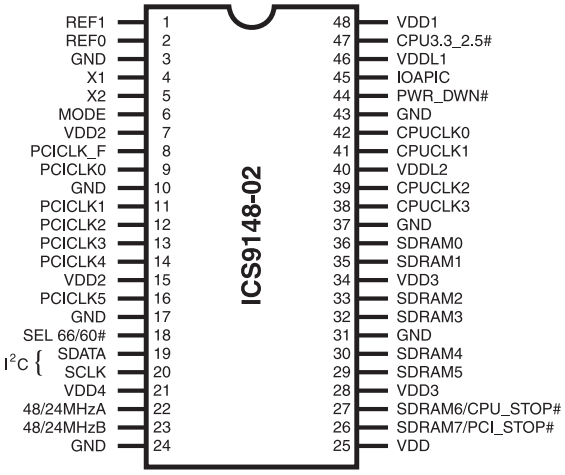
Block Diagram



Features

- Generates system clocks for CPU, IOAPIC, SDRAM, PCI, plus 14.314 MHz REF(0:1), USB, Plus Super I/O
- Supports single or dual processor systems
- I^2C serial configuration interface provides output clock disabling and other functions
- MODE input pin selects optional power management input control pins
- Two fixed outputs separately selectable as 24 or 48MHz
- Separate 2.5V and 3.3V supply pins
- 2.5V or 3.3V outputs: CPU, IOAPIC
- 3.3V outputs: SDRAM, PCI, REF, 48/24 MHz
- CPU 3.3_2.5# logic pin to adjust output strength
- No power supply sequence requirements
- Uses external 14.318MHz crystal
- 48 pin 300 mil SSOP
- Output enable register for serial port control: 1 = enable, 0 = disable

Pin Configuration



48-Pin SSOP

Functionality

VDD (1:4) 3.3V±10%, VDDL1, 2 2.5±5% or 3.3±10% 0-70°C
Crystal (X1, X2) = 14.31818 MHz

SEL	CPUCLK, SDRAM (MHz)	PCICLK (MHz)
0	60	30
1	66.6	33.3

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2, 1	REF (0:1)	OUT	Reference clock Output
3, 10, 17, 24, 31, 37, 43	GND	PWR	Ground (common)
4	X1	IN	Crystal or reference input, has internal crystal load cap
5	X2	OUT	Crystal output, has internal load cap and feedback resistor to X1
6	MODE	IN	Input function selection. If Mode is HIGH, then pins 26 & 27 are configured as outputs (SDRAM7 and SDRAM6). If Mode is LOW, then, pins 26 & 27 are configured as inputs (PCI_STOP# and CPU_STOP#).
7, 15	VDD2	PWR	Supply for PCICLK_F, PCICLK (0:5), nominal 3.3V
8	PCICLK_F	OUT	Free running PCI clock, not affected by PCI_STOP#
9, 11, 12, 13, 14, 16	PCICLK (0:5)	OUT	PCI clocks
18	SEL66/60#	IN	Selects 60MHz or 66.6MHz for SDRAM and CPU
19	SDATA	IN	I^2C data input
20	SCLK	IN	I^2C clock input
21	VDD4	PWR	Supply for 48/24MHzA, 48/24MHzB, nominal 3.3V
22	48/24MHzA	OUT	48/24MHz driver output for USB or Super I/O
23	48/24MHzB	OUT	48/24MHz driver output for USB or Super I/O
25	VDD	PWR	Supply for PLL core, nominal 3.3V
26	SDRAM7	OUT	SDRAM clock 60/66.6MHz (selected)
	PCI_STOP#	IN	Halts PCI Bus (0:5) at logic "0" level when low
27	SDRAM6	OUT	SDRAM clock 60/66.6MHz (selected)
	CPU_STOP#	IN	Halts CPU clocks at logic "0" level when low
28, 34	VDD3	PWR	Supply for SDRAM (0:5), SDRAM6/CPU_STOP#, SDRAM7/PCI_STOP#, nominal 3.3V
40	VDDL2	PWR	Supply for CPUCLK (0:3), either 2.5 or 3.3V nominal
42, 41, 39, 38	CPUCLK (0:3)	OUT	CPUCLK clock output, powered by VDDL2
36, 35, 33, 32, 30, 29	SDRAM (0:5)	OUT	SDRAMs clock at 60 or 66.6MHz (selected)
44	PWR_DWN#	IN	Powers down chip, active low
45	IOAPIC	OUT	IOAPIC clock output, (14.318MHz) powered by VDDL1
46	VDDL1	PWR	Supply for IOAPIC, either 2.5 or 3.3V nominal
47	CPU3.3-2.5#	IN	3.3 or 2.5 VDD buffer strength selection, has pullup to VDD, nominal 30K resistor. When connected to VDD, 3.3V Buffer strength is selected. When connected to GND, 2.5V Buffer strength is selected.
48	VDD1	PWR	Supply for REF (0:1), X1, X2, nominal 3.3V

Power Groups

VDD = Supply for PLL core
VDD1 = REF (0:1), X1, X2
VDD2 = PCICLK_F, PCICLK (0:5)
VDD3 = SDRAM (0:5), SDRAM6/CPU_STOP#, SDRAM7/PCI_STOP#
VDD4 = 48/24MHzA, 48/24MHzB
VDDL1 = IOAPIC
VDDL2 = CPUCLK (0:3)

Power-On Conditions

SEL 66/60#	MODE	PIN #	DESCRIPTION	FUNCTION
1	1	38, 39, 41, 42	CPUCLKs	66.6 MHz - w/serial config enable/disable
		36, 35, 33, 32, 30, 29, 27, 26	SDRAM	66.6 MHz - All SDRAM outputs
		16, 14, 13, 12, 11, 9, 8	PCICLKs	33.3 MHz - w/serial config enable/disable
0	1	38, 39, 41, 42	CPUCLKs	60 MHz - w/serial config enable/disable
		36, 35, 33, 32, 30, 29, 27, 26	SDRAM	60 MHz - w/serial config enable/disable
		16, 14, 13, 12, 11, 9, 8	PCICLKs	30 MHz - w/serial config enable/disable
1	0	26	PCI_STOP#	Power Management, PCI (0:5) Clocks Stopped when low
		27	CPU_STOP#	Power Management, CPU (0:5) Clocks Stopped when low
		8	PCICLK_F	33.3 MHz - 33.3 MHz - PCI Clock Free running for Power Management
		38, 39, 41, 42	CPUCLKs	66.6 MHz - CPU Clocks w/external Stop Control and serial config individual enable/disable.
		36, 35, 33, 32, 30, 29	SDRAM	66.6 MHz - SDRAM Clocks w/serial config individual enable/disable.
		16, 14, 13, 12, 11, 9	PCICLKs	33.3 MHz - PCI Clocks w/external Stop control and serial config individual enable/disable.
0	0	26	PCI_STOP#	Power Management, PCI (0:5) Clocks Stopped when low
		27	CPU_STOP#	Power Management, CPU (0:5) Clocks Stopped when low
		8	PCICLK_F	30 MHz - PCI Clock Free running for Power Management
		38, 39, 41, 42	CPUCLKs	60 MHz - CPU Clocks w/external Stop control and serial config individual enable/disable.
		36, 35, 33, 32, 30, 29	SDRAM	60 MHz - SDRAM Clocks w/serial config individual enable/disable.
		16, 14, 13, 12, 11, 9	PCICLKs	30 MHz - PCI Clocks w/external Stop control and serial config individual enable/disable.

Example:
a) if MODE = 1, pins 26 and 27 are configured as SDRAM7 and SDRAM6 respectively.
b) if MODE = 0, pins 26 and 27 are configured as PCI_STOP# and CPU_STOP# respectively.

Power-On Default Conditions

At power-up and before device programming, all clocks will default to an enabled and “on” condition. The frequencies that are then produced are on the MODE pin as shown in the table below.

CLOCK	DEFAULT CONDITION AT POWER-UP
REF (0:1)	14.31818 MHz
IOAPIC 0	14.31818 MHz
48/24 MHz	48 MHz

Technical Pin Function Descriptions

VDD(1,2,3,4)
This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:1), PCICLK, 48/24MHzA/B and SDRAM(0:7).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2
This is the power supplies for the CPUCLK and IOAPCI output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

X1
This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. See the data tables for the value of this capacitor.

X2
This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor that is connected to ground. See the Data Sheet for the value of this capacitor.

CPUCLK (0:3)
These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks are controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

SDRAM(0:7)
These Output Clocks are use to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD3 of the device, operates at 3.3 volts.

48/24MHzA, B
This is a fixed frequency Clock output that is typically used to drive Super I/O devices. Outputs A and B are defined as 24 or 48MHz by I^2C register (see table).

IOAPIC
This Output is a fixed frequency Output Clock that runs at the Reference Input (typically 14.31818MHz) . Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

REF(0:1)
The REF Outputs are fixed frequency Clocks that run at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F
This Output is equal to PCICLK(0:5) and is FREE RUNNING, and will not be stopped by PCI_STP#.

PCICLK (0:5)
These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency.

SELECT 66.6/60MHz#
This Input pin controls the frequency of the Clocks at the CPU, PCICLK and SDRAM output pins. If a logic "1" value is present on this pin, the 66.6 MHz Clock will be selected. If a logic "0" is used, the 60MHz frequency will be selected.

MODE
This Input pin is used to select the Input function of the I/O pins. An active Low will place the I/O pins in the Input mode and enable those stop clock functions.

Technical Pin Function Descriptions

CPU 3.3_2.5#
This Input pin controls the CPU and IOAPIC output buffer strength for skew matching CPU and SDRAM outputs to compensate for the external VDDL supply condition. It is important to use this function when selecting power supply requirements for VDDL1,2. A logic "0" (ground) will indicate 2.5V operation and a logic "1" will indicate 3.3V operation. This pin has an internal pullup resistor to VDD.

PWR_DWN#
This is an asynchronous active Low Input pin used to Power Down the device into a Low Power state by not removing the power supply. The internal Clocks are disabled and the VCO and Crystal are stopped. Powered Down will also place all the Outputs in a low state at the end of their current cycle. The latency of Power Down will not be greater than 3ms. The I^2C inputs will be Tri-Stated and the device will retain all programming information. This input pin only valid when MODE=0 (Power Management Mode)

CPU_STOP#
This is a synchronous active Low Input pin used to stop the CPUCLK clocks in an active low state. All other Clocks including SDRAM clocks will continue to run while this function is enabled. The CPUCLK's will have a turn ON latency of at least 3 CPU clocks. This input pin only valid when MODE=0 (Power Management Mode)

PCI_STOP#
This is a synchronous active Low Input pin used to stop the PCICLK clocks in an active low state. It will not effect PCICLK_F nor any other outputs. This input pin only valid when MODE=0 (Power Management Mode)

I^2C
The SDATA and SCLOCK Inputs are use to program the device. The clock generator is a slave-receiver device in the I^2C protocol. It will allow read-back of the registers. See configuration map for register functions. The I^2C specification in Philips I^2C Peripherals Data Handbook (1996) should be followed.

General I²C serial interface information

A. For the clock generator to be addressed by an I²C controller, the following address must be sent as a start sequence, with an acknowledge bit between each byte.

Clock Generator Address (7 bits)	ACK	+ 8 bits dummy command code	ACK	+ 8 bits dummy Byte count	ACK	Then Byte 0, 1, 2, etc in sequence until STOP.
A(6:0) & R/W#						
D2(H)						

B. The clock generator is a slave/receiver I²C component. It can "read back "(in Philips I²C protocol) the data stored in the latches for verification. (set R/W# to 1 above). There is no BYTE count supported, so it does not meet the Intel SMB PIIX4 protocol.

Clock Generator Address (7 bits)	ACK	Byte 0	ACK	Byte 1	ACK	Byte 0, 1, 2, etc in sequence until STOP.
A(6:0) & R/W#						
D3(H)						

C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)

D. The input is operating at 3.3V logic levels.

E. The data byte format is 8 bit bytes.

F. To simplify the clock generator I²C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.

G In the power down mode (PWR_DWN# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.

H. At power-on, all registers are set to a default condition. See Byte 0 detail for default condition, Bytes 1 through 5 default to a 1 (Enabled output state)

Serial Configuration Command Bitmaps

Byte 0: Functional and Frequency Select Clock Register (default on Bits 7, 6, 5, 4, 1, 0 = 0)

Note: PWD = Power-Up Default **(default on Bits 3, 2 = 1)**

BIT	PIN#	DESCRIPTION	PWD
Bit 7	-	Reserved	0
Bit 6	-	Must be 0 for normal operation	0
Bit 5	-	In Spread Spectrum, Controls type (0=centered, 1=down spread)	0
Bit 4		In Spread Spectrum, Controls Spreading (0=1.8% 1=0.6%)	0
Bit 3	23	48/24 MHz (Frequency Select) 1=48 MHz, 0=24 MHz	1
Bit 2	22	48/24 MHz (Frequency Select) 1=48 MHz, 0=24 MHz	1
Bit 1 Bit 0	-	Bit1 Bit0 1 1 - Tri-State 1 0 - Spread Spectrum Enable 0 1 - Testmode 0 0 - Normal operation	 0 0

I²C is a trademark of Philips Corporation

Select Functions

Functionality	CPU	PCI, PCI_F	SDRAM	REF	IOAPIC	24 MHz Selection	48 MHz Selection
Tristate	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z	HI - Z
Testmode	TCLK/2[1]	TCLK/4[1]	TCLK/2[1]	TCLK[1]	TCLK[1]	TCLK/4[1]	TCLK/2[1]

Notes:
1. TCLK is a test clock driven on the X1 (crystal in pin) input during test mode.

Byte 1: CPU, 24/48 MHz Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	23	1	48/24 MHz (Act/Inact)
Bit 6	22	1	48/24 MHz (Act/Inact)
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	38	1	CPUCLK3 (Act/Inact)
Bit 2	39	1	CPUCLK2 (Act/Inact)
Bit 1	41	1	CPUCLK1 (Act/Inact)
Bit 0	42	1	CPUCLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: PCICLK Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLK_F (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 3: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	26	1	SDRAM7 (Act/Inact)
Bit 6	27	1	SDRAM6 (Act/Inact)
Bit 5	29	1	SDRAM5 (Act/Inact)
Bit 4	30	1	SDRAM4 (Act/Inact)
Bit 3	32	1	SDRAM3 (Act/Inact)
Bit 2	33	1	SDRAM2 (Act/Inact)
Bit 1	35	1	SDRAM1(Act/Inact)
Bit 0	36	1	SDRAM0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Note: PWD = Power-Up Default

Byte 5: Peripheral Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	45	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	1	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low
Note: PWD = Power-Up Default

Byte 6: Optional Register for Future

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes:
1. Byte 6 is reserved by Integrated Circuit Systems for future applications.

Power Management

Clock Enable Configuration

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	Other Clocks, SDRAM, REF, IOAPICs, 48/24 MHz A 48/24 MHz B	Crystal	VCOs
X	X	0	Low	Low	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running
0	1	1	Low	33.3/30 MHz	Running	Running	Running
1	0	1	66.6/60 MHz	Low	Running	Running	Running
1	1	1	66.6/60 MHz	33.3/30 MHz	Running	Running	Running

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PWR PD# select pin will not cause clocks of a short or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

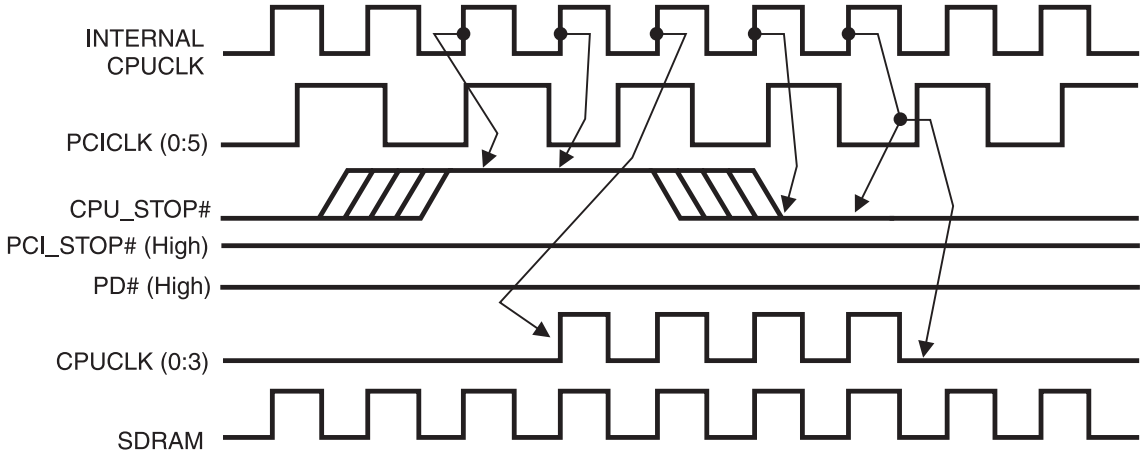
ICS9148-02 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency No. of rising edges of free running PCICLK
CPU_ STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PCI_STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PWR_DWN#	1 (Normal Operation)[3]	3mS
	0 (Power Down)[4]	2max

Notes.
1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, SDRAM, PCICLK only.
   The REF and IOAPIC will be stopped independant of these.

CPU_STOP# Timing Diagram

CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9148-02**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

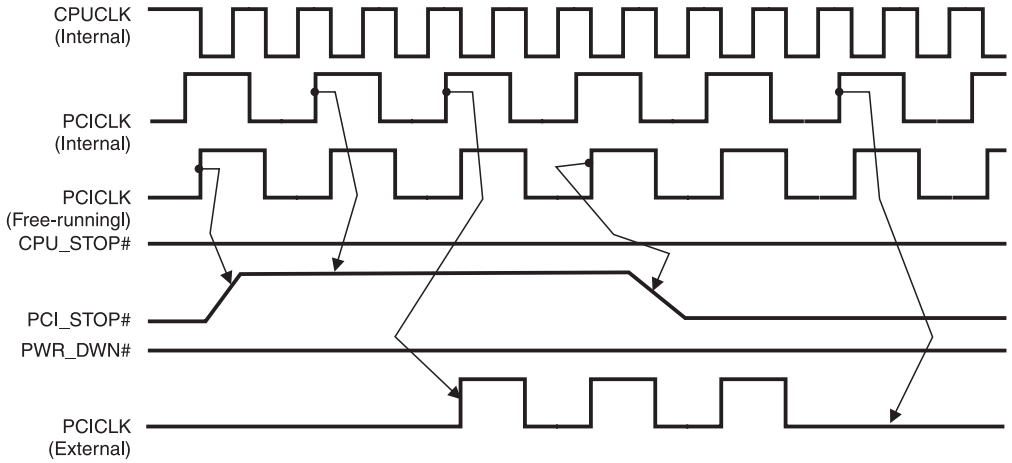


Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9148-02**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9148-02**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9148-02** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

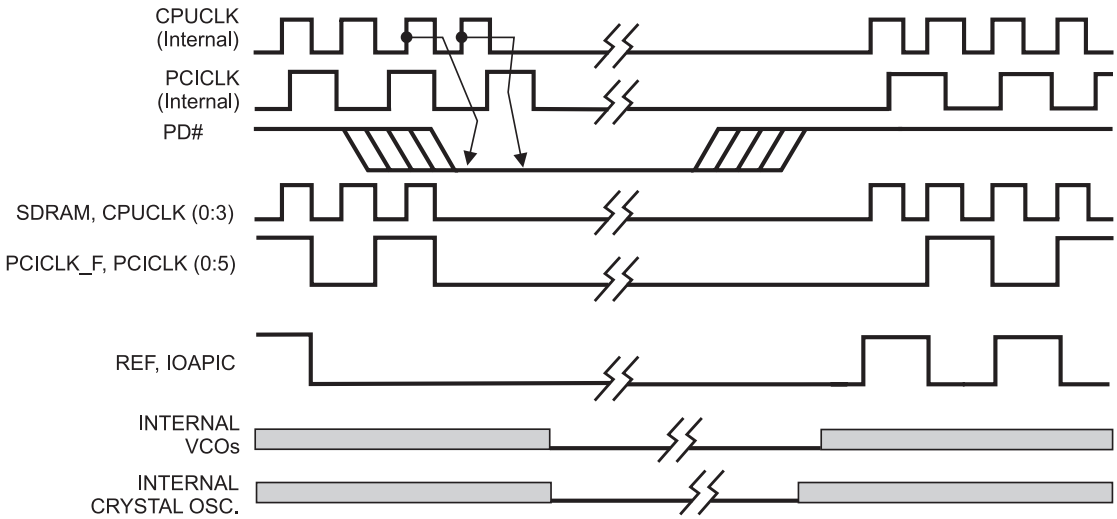
(Drawing shown on next page.)



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the **ICS9148-02** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3mS. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9148.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M		60	100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND		400	600	µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	ps
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.				ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-SDRAM1}$	V_T = 1.5 V		200	500	ps
	$T_{CPU-PCI1}$	V_T = 1.5 V;	1.5	3.2	4.5	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0 pF; Select @ 66M		5	20	mA
Power Down Supply Current	$I_{DD2.5PD}$	C_L = 0 pF;		0.21	1.0	µA
Skew[1]	$T_{CPU-SDRAM2}$	V_T = 1.5 V; V_{TL} = 1.25 V; SDRAM Leads		150	500	ps
	$T_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V; CPU Leads	1	2.8	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O2}		60		66	MHz
Output Impedance	R_{DSP2A}[1]	V_O = V_{DD}*(0.5)	10		20	Ω
Output Impedance	R_{DSN2A}[1]	V_O = V_{DD}*(0.5)	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4	2.5		V
Output Low Voltage	V_{OL2A}	I_{OL} = 27 mA		0.35	0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V		-52	-48	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	49.3	59		mA
Rise Time	t_{r2A}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.1	2.85	ns
Fall Time	t_{f2A}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.95	2.85	ns
Duty Cycle	d_{t2A}[1]	V_T = 1.5 V	45	51	55	%
Skew	t_{sk2A}[1]	V_T = 1.5 V		80	250	ps
Jitter	$t_{jcyc-cyc2A}$[1]	V_T = 1.5 V		170	250	ps
	t_{j1s2A}[1]	V_T = 1.5 V		60	150	ps
	t_{jabs2A}[1]	V_T = 1.5 V	-250	100	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O2}		60		66	MHz
Output Impedance	R_{DSP2B}[1]	V_O = V_{DD}*(0.5)	10		25	Ω
Output Impedance	R_{DSN2B}[1]	V_O = V_{DD}*(0.5)	10		25	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -13.0 mA	2	2.2		V
Output Low Voltage	V_{OL2B}	I_{OL} = 14 mA		0.3	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-20	-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	22	26		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.42	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		0.95	1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	49.5	55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V		60	250	ps
Jitter	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		150	250	ps
	t_{j1s2B}[1]	V_T = 1.25 V		80	150	ps
	t_{jabs2B}[1]	V_T = 1.25 V	-250	80	+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}		30	-	33	MHz
Output Impedance	R_{DSP1}[1]	V_O = V_{DD}*(0.5)	12		55	Ω
Output Impedance	R_{DSN1}[1]	V_O = V_{DD}*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -14.5 mA	2.4	2.7		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-47	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	17.1	47.5		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.1	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		100	500	ps
Jitter	t_{j1s1}[1]	V_T = 1.5 V		50	150	ps
	t_{jabs1}[1]	V_T = 1.5 V	-250	120	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O3}		60		66	MHz
Output Impedance	R_{DSP3}[1]	V_O = V_{DD}*(0.5)	10		24	Ω
Output Impedance	R_{DSN3}[1]	V_O = V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -24 mA	2.4	2.5		V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA		0.35	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-47	-40	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	41	47.5		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.45	1.7	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.2	1.5	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45	51	55	%
Skew	T_{sk3}[1]	V_T = 1.5 V		80	500	ps
Jitter	T_{j1s3}[1]	V_T = 1.5 V		40	150	ps
	T_{jabs3}[1]	V_T = 1.5 V	-250	-	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF0

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 45 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O7}			14.318		MHz
Output Impedance	R_{DSP7}	V_O = V_{DD}*(0.5)	10		24	Ω
Output Impedance	R_{DSN7}	V_O = V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH7}	I_{OH} = -24 mA	2.4	2.5		V
Output Low Voltage	V_{OL7}	I_{OL} = 23 mA		0.35	0.4	V
Output High Current	I_{OH7}	V_{OH} = 2.0 V		-47	-40	mA
Output Low Current	I_{OL7}	V_{OL} = 0.8 V	41	47.5		mA
Rise Time	T_{r7}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	2	ns
Fall Time	T_{f7}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	D_{t7}[1]	V_T = 1.5 V	45	52	45	%
Jitter	T_{j1s7}[1]	V_T = 1.5 V		150	350	ps
	T_{jabs7}[1]	V_T = 1.5 V	-600	-	600	pS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24M, 48M, REF1

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O24M}			24		MHz
Output Frequency	F_{O48M}			48		MHz
Output Frequency	F_{OREF}			14.318		MHz
Output Impedance	R_{DSP5}[1]	V_O = V_{DD}*(0.5)	20		60	Ω
Output Impedance	R_{DSN5}[1]	V_O = V_{DD}*(0.5)	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4	2.5		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.2	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-29	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	25		mA
Rise Time	t_{r5}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	4	ns
Fall Time	t_{f5}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.7	4	ns
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45	51	55	%
Jitter	t_{j1s5A}[1]	V_T = 1.5 V; Fixed Clocks		50	150	pS
	t_{j1s5B}[1]	V_T = 1.5 V; Ref Clocks		150	350	
	t_{jabs5A}[1]	V_T = 1.5 V; Fixed Clocks	-250	120	250	
	t_{jabs5B}[1]	V_T = 1.5 V; Ref Clocks	-600	-	600	pS

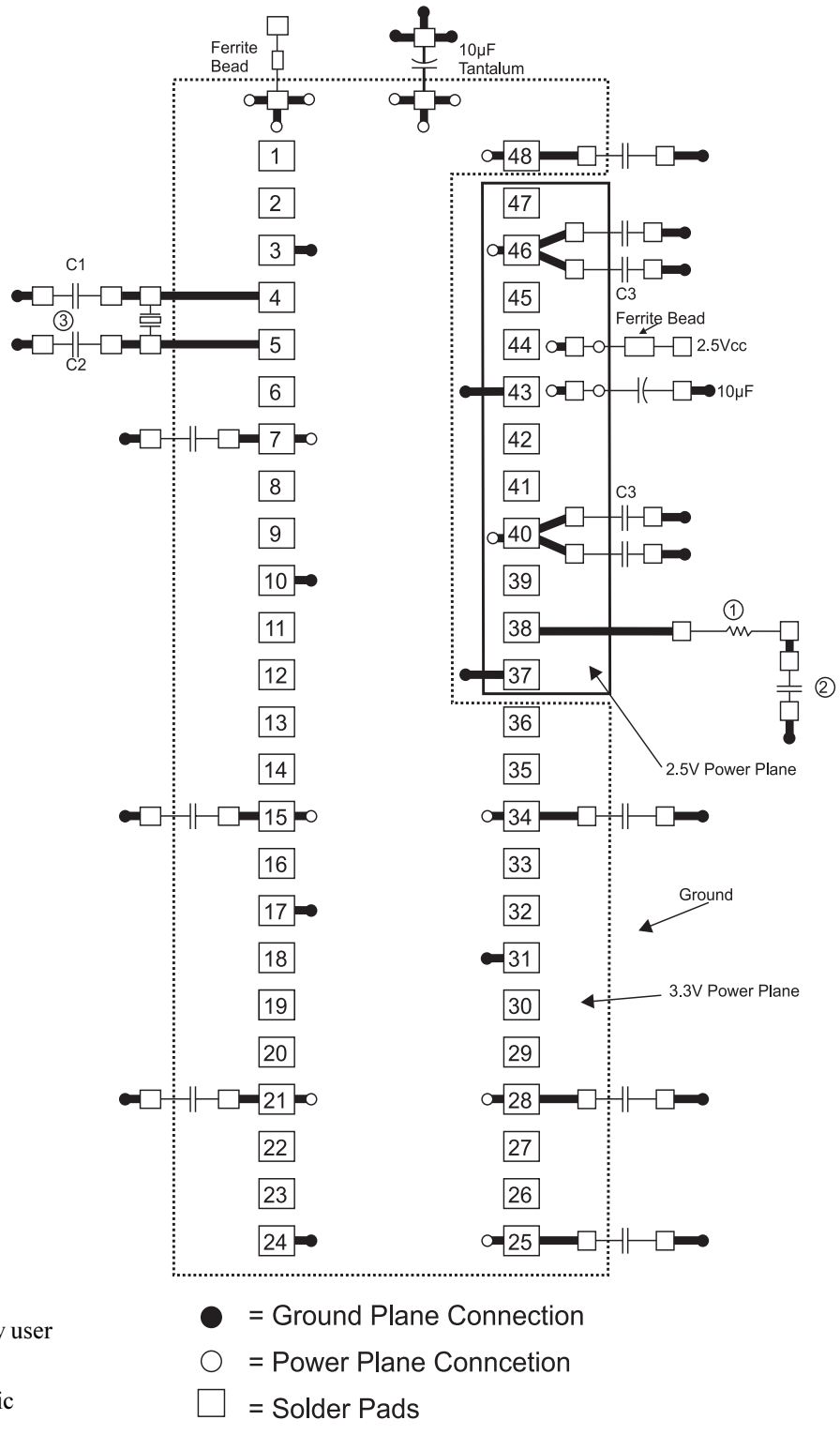
[1]Guarenteed by design, not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

1 All clock outputs should have series terminating resistor. Not shown in all places to improve readibility of diagram
2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
3 Optional crystal load capacitors are recommended.

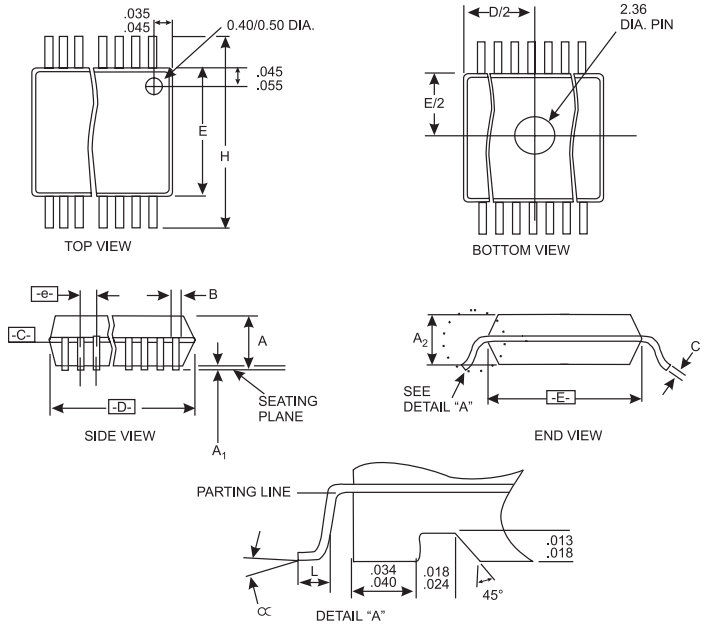


Capacitor Values:

C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	.006	.0085					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

This table in inches

Ordering Information

ICS9148F-02

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device