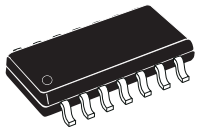
L6491

High voltage high and low-side 4 A gate driver

Datasheet - production data



SO-14

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability: 4 A source/sink
- Switching times 15 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Comparator for fault protections
- Smart shutdown function
- Adjustable deadtime
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Effective fault protection
- Flexible, easy and fast design

Applications

- Motor driver for home appliances, factory automation, industrial drives and fans
- HID ballasts
- Power supply unit
- Induction heating
- Wireless chargers
- Industrial inverters
- UPS

Description

The L6491 is a high voltage device manufactured with the BCD6 “OFF-LINE” technology. It is a single-chip half-bridge gate driver for N-channel power MOSFET or IGBT.

The high-side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing microcontroller/DSP.

An integrated comparator is available for fast protection against overcurrent, overtemperature, etc.

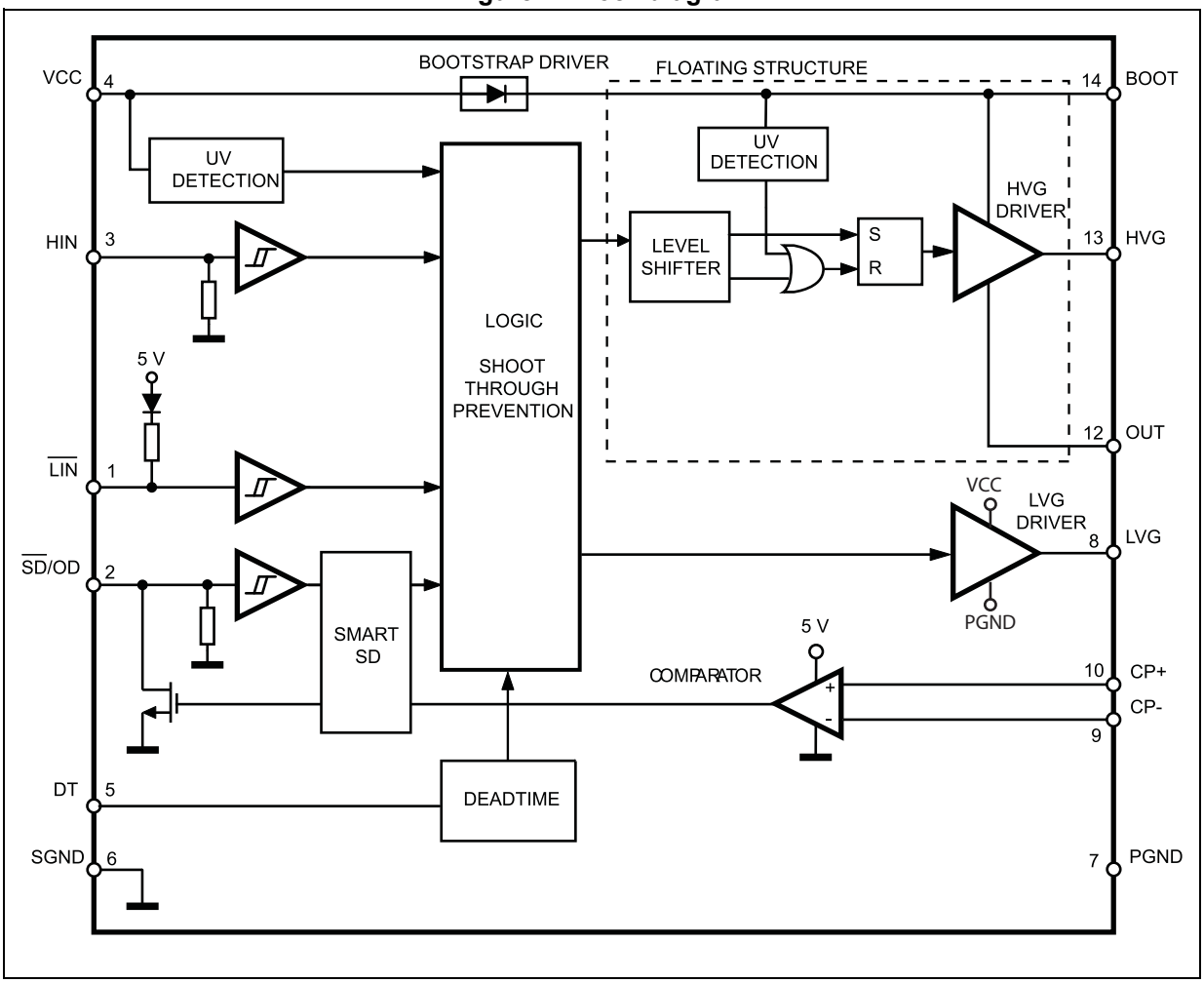
Table 1. Device summary

Order code	Package	Packaging
L6491D	SO-14	Tube
L6491DTR	SO-14	Tape and reel

Contents

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

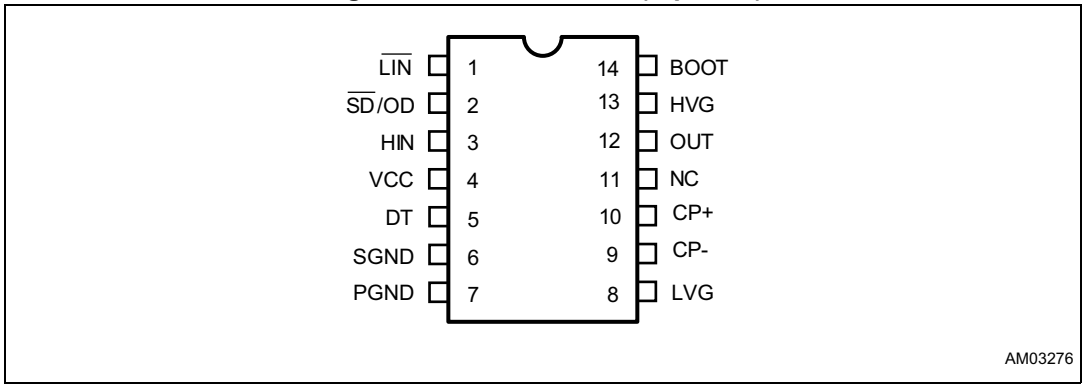


Table 2. Pin description

Pin number	Pin name	Type	Function
1	$\overline{LIN}$	I	Low-side driver logic input (active low)
2	$\overline{SD}$/OD(1)	I/O	Shutdown logic input (active low)/open-drain comparator output
3	HIN	I	High-side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Deadtime setting
6	SGND	P	Signal ground
7	PGND	P	Power ground
8	LVG(1)	O	Low-side driver output
9	CP-	I	Comparator negative input
10	CP+	I	Comparator positive input
11	NC		Not connected
12	OUT	P	High-side (floating) common voltage
13	HVG(1)	O	High-side driver output
14	BOOT	P	Bootstrapped supply voltage

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.
When the $\overline{SD}$ is set low, gate driver outputs are forced low and assure low impedance.

3 Truth table

Table 3. Truth table

Input			Output	
$\overline{SD}$	$\overline{LIN}$	HIN	LVG	HVG
L	X(1)	X(1)	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

1. X: don't care.

4 Electrical data

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings(1)

Symbol	Parameter	Value		Unit
		Min.	Max.	
VCC	Supply voltage	-0.3	21	V
V_{PGND}	Low-side driver ground	VCC - 21	VCC + 0.3	V
V_{out}	Output voltage	V_{boot} - 21	V_{boot} + 0.3	V
V_{boot}	Bootstrap voltage	-0.3	620	V
V_{hvg}	High-side gate output voltage	V_{out} - 0.3	V_{boot} + 0.3	V
V_{lvg}	Low-side gate output voltage	PGND - 0.3	V_{CC} + 0.3	V
V_{cp-}	Comparator negative input voltage(2)	-0.3	5.5	V
V_{cp+}	Comparator positive input voltage(2)	-0.3	5.5	V
V_i	Logic input voltage	-0.3	15	V
V_{OD}	Open-drain voltage	-0.3	15	V
dv_{out} / dt	Allowed output slew rate		50	V/ns
P_{tot}	Total power dissipation (T_A = 25 °C)		1.0	W
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

1. Each voltage referred to SGND unless otherwise specified.
2. Spikes up to 20 V can be tolerated if the duration is shorter than 50 ns (f_{SW} = 120 kHz).

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	SO-14	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	120	°C/W

4.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Pin	Parameter	Test conditions	Min.	Max.	Unit
VCC	4	Supply voltage		10	20	V
V_{PS}(1)	7 - 6	Low-side driver ground		-1.5	+1.5	V
V_{BO}(2)	14 - 12	Floating supply voltage		9.3	20	V
V_{out}	12	DC output voltage		- 9(3)	580	V
V_{CP-}	9	Comparator negative input pin voltage	$V_{CP+} \leq 2.5$ V		5(4)	V
V_{CP+}	10	Comparator positive input pin voltage	$V_{CP-} \leq 2.5$ V		5(4)	V
f_{sw}		Switching frequency	HVG, LVG load C_L = 1 nF		800	kHz
T_J		Junction temperature		-40	125	°C

1. $V_{PS} = V_{PGND}$ - SGND.
2. $V_{BO} = V_{boot} - V_{out}$.
3. LVG off. V_{CC} = 12.5 V. Logic is operational if V_{boot} > 5 V.
4. At least one of the comparator's inputs must be lower than 2.5 V to guarantee proper operation.

5 Electrical characteristics

5.1 AC operation

Table 7. AC operation electrical characteristics (VCC = 15 V; PGND = SGND; T_J = +25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}	1 vs. 8 3 vs 13	High/low-side driver turn-on propagation delay	OUT = 0 V BOOT = VCC C_L = 1 nF V_i = 0 to 3.3 V see *Figure 3*		85	120	ns
t_{off}		High/low-side driver turn-off propagation delay			85	120	ns
t_{sd}	2 vs. 8, 13	Shutdown to high/low-side driver propagation delay			85	120	ns
t_{isd}		Comparator triggering to high/low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CP+; CP- = 0.5 V		175	220	ns
MT		Delay matching, HS and LS turn-on/off(1)				30	ns
DT	5	Deadtime setting range see *Figure 4*	R_{DT} = 0 Ω, C_L = 1 nF	0.12	0.18	0.24	µs
			R_{DT} = 100 kΩ, C_L = 1 nF, C_{DT} = 100 nF	1.2	1.4	1.6	µs
			R_{DT} = 200 kΩ, C_L = 1 nF, C_{DT} = 100 nF	2.2	2.6	3	µs
MDT		Matching deadtime(2)	R_{DT} = 0 Ω, C_L = 1 nF			50	ns
			R_{DT} = 100 kΩ, C_L = 1 nF, C_{DT} = 100 nF			165	ns
			R_{DT} = 200 kΩ, C_L = 1 nF, C_{DT} = 100 nF			260	ns
t_r	8,13	Rise time	C_L = 1 nF		15	40	ns
t_f		Fall time	C_L = 1 nF		15	40	ns

1. MT = max. ($|t_{on(LVG)} - t_{off(LVG)}|$, $|t_{on(HVG)} - t_{off(HVG)}|$, $|t_{off(LVG)} - t_{on(HVG)}|$, $|t_{off(HVG)} - t_{on(LVG)}|$).
2. MDT = $|DT_{LH} - DT_{HL}|$ (see *Figure 5 on page 14*).

Figure 3. Timing

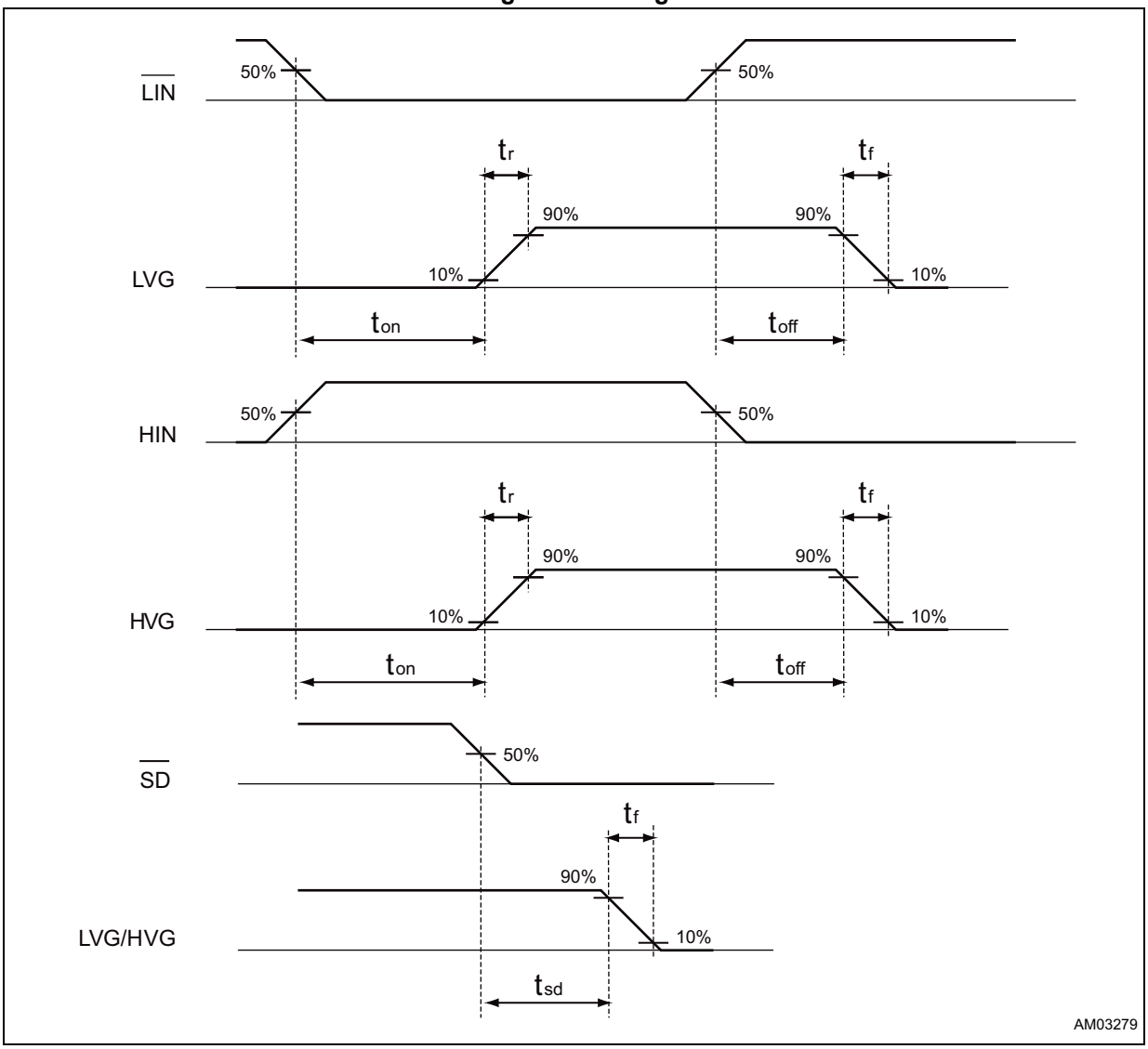
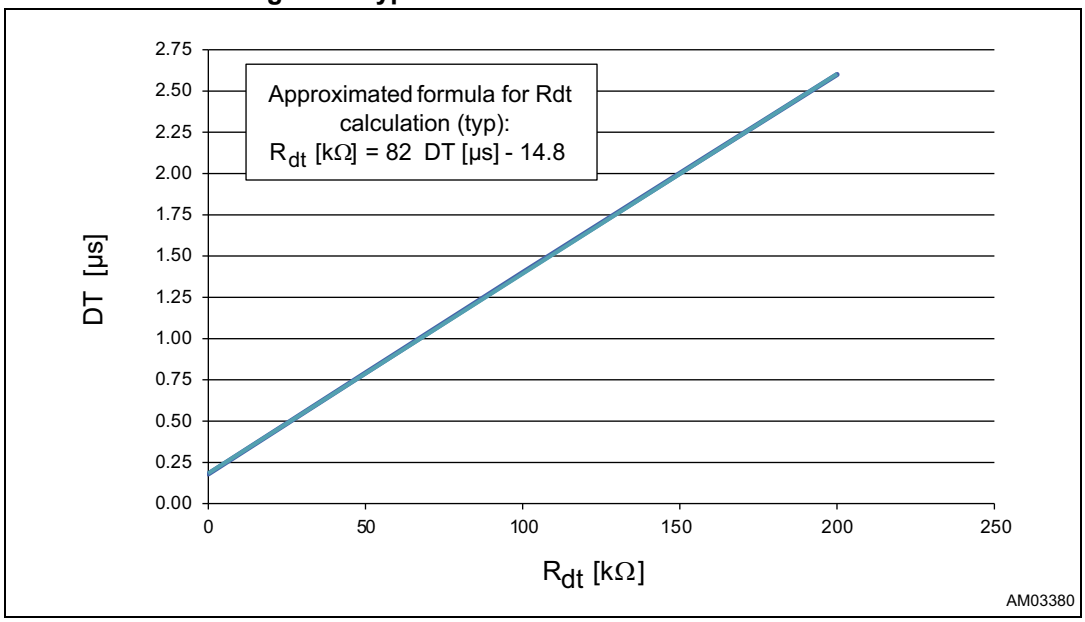


Figure 4. Typical deadtime vs. DT resistor value



5.2 DC operation

Table 8. DC operation electrical characteristics
(VCC = 15 V; PGND = SGND; T_J = + 25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc_hys}	4	VCC UV hysteresis		0.5	0.6	0.72	V
V_{cc_thON}		VCC UV turn-ON threshold		8.7	9.3	9.8	V
V_{cc_thOFF}		VCC UV turn-OFF threshold		8.2	8.7	9.2	V
I_{qccu}		Undervoltage quiescent supply current	VCC = 8 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = SGND; R_{DT} = 0 Ω; CP+ = SGND; CP- = 5 V		160	210	µA
I_{qcc}		Quiescent current	VCC = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ = 5 V; HIN = SGND; R_{DT} = 0 Ω; CP+ = SGND; CP- = 5 V		540	700	µA
Bootstrapped supply voltage section(1)							
V_{BO_hys}	14-12	V_{BO} UV hysteresis		0.48	0.6	0.7	V
V_{BO_thON}		V_{BO} UV turn-ON threshold		8	8.6	9.1	V
V_{BO_thOFF}		V_{BO} UV turn-OFF threshold		7.5	8.0	8.5	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	VCC = V_{BO} = 7 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+ = SGND; CP- = 5 V		20	30	µA
I_{QBO}		V_{BO} quiescent current	V_{BO} = 15 V $\overline{SD}$ = 5 V; $\overline{LIN}$ and HIN = 5 V; R_{DT} = 0 Ω; CP+ = SGND; CP- = 5 V		90	120	µA
I_{LK}		High voltage leakage current	BOOT = HVG = OUT = 600 V			8	µA
$R_{DS(on)}$		Bootstrap driver on resistance(2)			175		Ω

Table 8. DC operation electrical characteristics (VCC = 15 V; PGND = SGND; T_J = + 25 °C) (continued)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Driving buffer section							
I_{so}	8, 13	High/low-side source peak current	LVG/HVG ON T_J = 25 °C	3.5	4		A
			Full temperature range	2.5			A
I_{si}		High/low-side sink peak current	LVG/HVG OFF T_J = 25 °C	3.5	4		A
			Full temperature range	2.5			A
Logic inputs							
V_{il}	1, 2, 3	Low level logic threshold		0.95		1.45	V
V_{ih}		High level logic threshold voltage		2		2.5	V
V_{SSD}	2	SmartSD unlatch threshold				0.8	V
V_{il_S}	1, 3	Single input voltage	$\overline{LIN}$ and HIN connected together and floating			0.8	V
I_{HINh}	3	HIN logic “1” input bias current	HIN = 15 V	120	200	260	µA
I_{HINl}		HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	1	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 0 V	5	10	15	µA
I_{LINh}		$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 15 V			1	µA
I_{SDh}	2	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 15 V	20	40	60	µA
I_{SDl}		$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 0 V			1	µA

1. $V_{BO} = V_{boot} - V_{out}$.
2. $R_{DS(on)}$ is tested in the following way:
$R_{DS(on)} = [(VCC - V_{BOOT1}) - (VCC - V_{BOOT2})] / [I_1(VCC, V_{BOOT1}) - I_2(VCC, V_{BOOT2})]$ where I_1 is pin 14 current when $V_{BOOT} = V_{BOOT1}$, I_2 when $V_{BOOT} = V_{BOOT2}$.

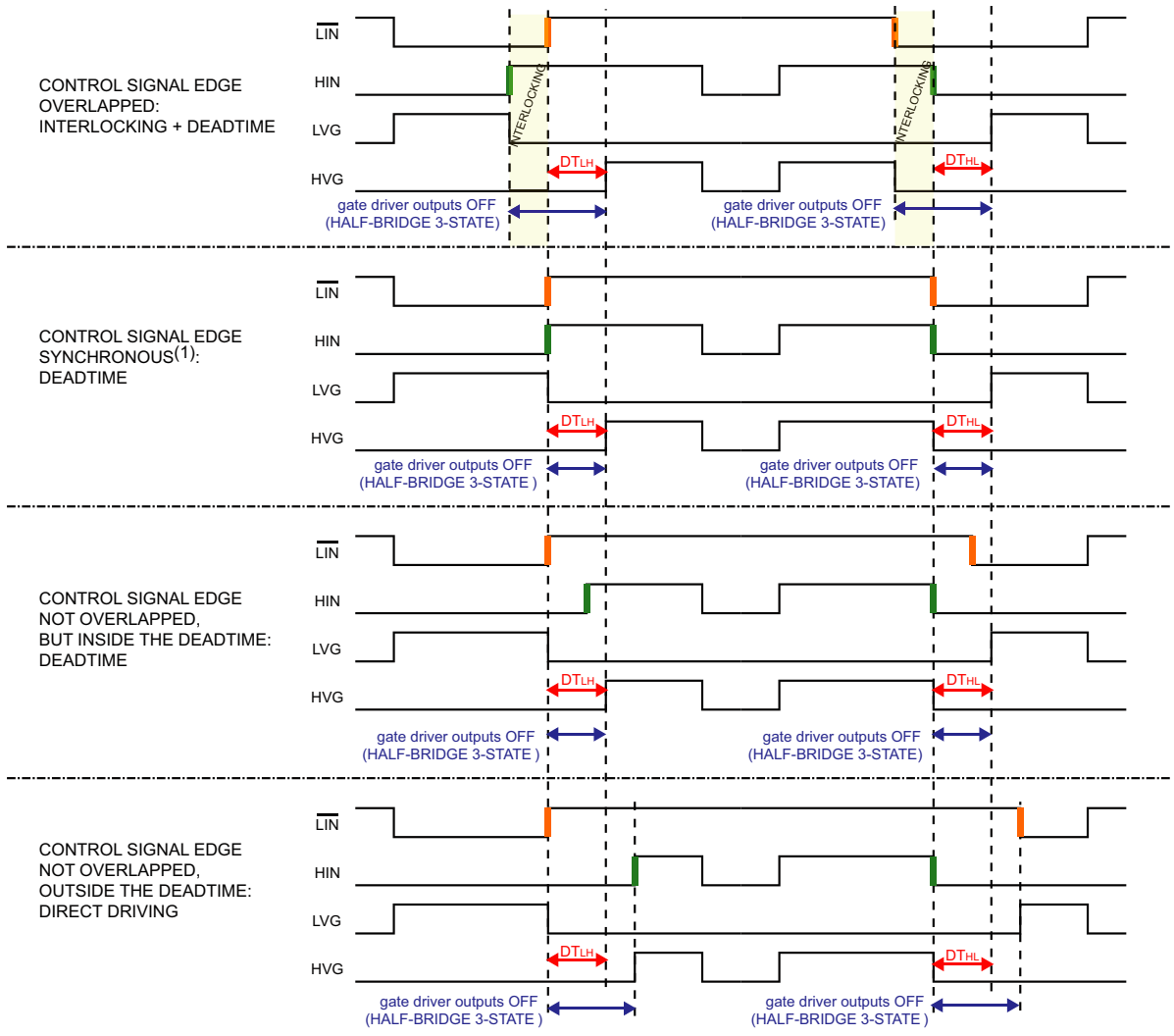
Table 9. Sense comparator(1) (V_{CC} = 15 V, T_J = +25 °C)

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	9, 10	Input offset voltage		-15		15	mV
I_{ib}	9, 10	Input bias current	V_{CP+} = 1 V, V_{CP-} = 1 V			1	µA
I_{OD}	2	Open-drain low level sink current	SD\OD = 400 mV, V_{CP}+ = 1 V; V_{CP} - = 0.5 V;	13	20	27	mA
t_{d_comp}		Comparator delay	Rpu = 100 kΩ to 5 V; V_{CP} - = 0.5 V; voltage step on CP+ = 0 to 3.3 V; 50% CP+ to 90% SD		100	155	ns
SR	2	Slew rate	C_L = 10 nF; Rpu = 5 kΩ to 5 V; 90% SD to 10% SD		10		V/µs

1. Comparator is disabled when VCC is in UVLO condition.

6 Waveform definitions

Figure 5. Deadtime and interlocking waveform definitions



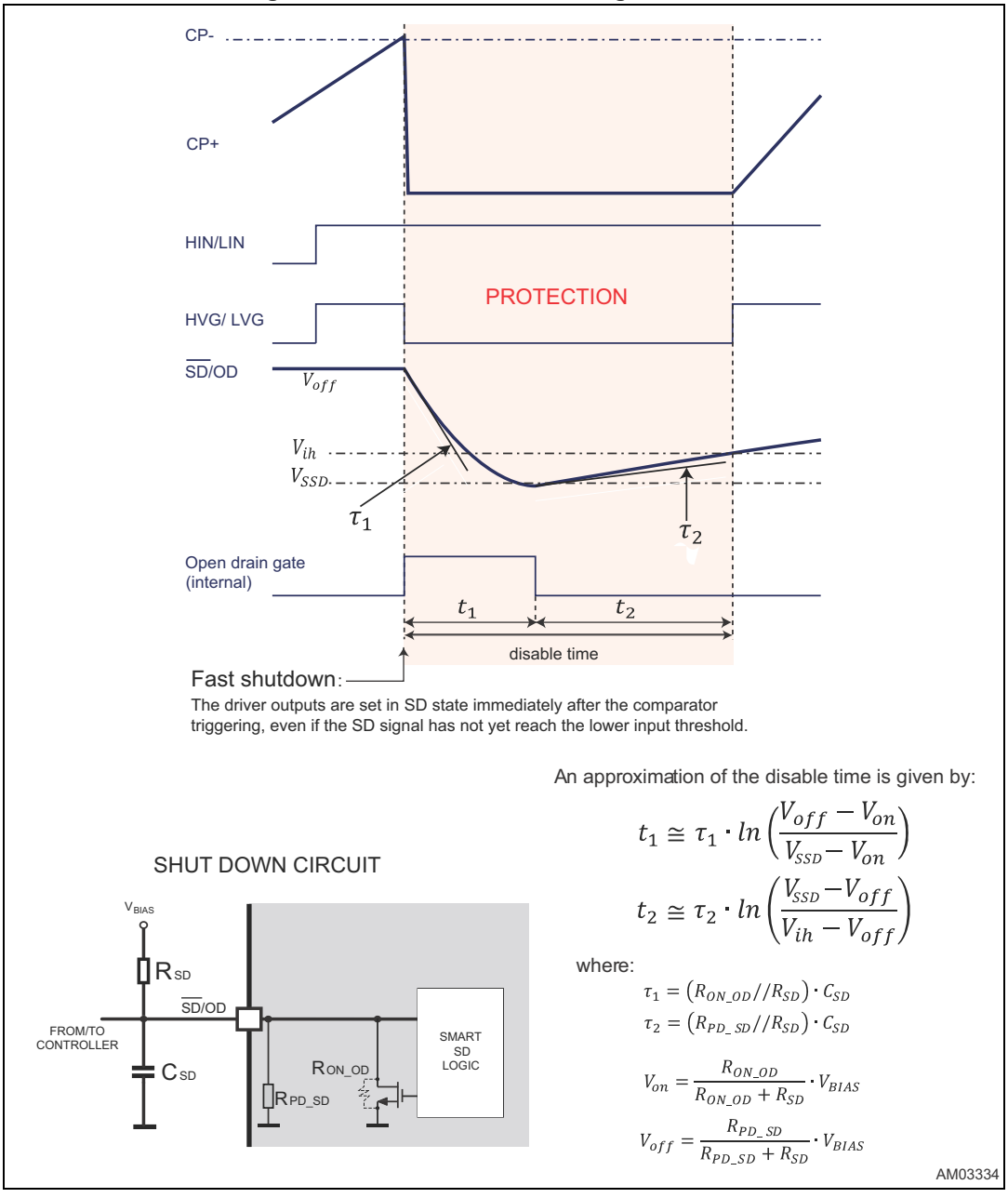
(1) HIN and $\overline{\text{LIN}}$ can be connected togheter and driven by just one control signal.

7 Smart shutdown function

The L6491 device integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function.

The output signal of the comparator is fed to an integrated MOSFET with the open-drain output available on pin 2, shared with the $\overline{SD}$ input. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low level leaving the half-bridge in 3-state.

Figure 6. Smart shutdown timing waveforms



In common overcurrent protection architectures, the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$/OD line in order to provide a monostable circuit, which implements a protection time following the fault condition. Differently from the common fault detection systems, the L6491 smart shutdown architecture allows immediate turn-off of the output gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the current output switch-off. In fact the time delay between the fault and the output turn-off is no longer dependent on the RC value of the external network connected to the $\overline{SD}$/OD pin. In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering. At the same time, the internal logic turns on the open-drain output and holds it on until the $\overline{SD}$ voltage goes below the smartSD unlatch threshold V_{SSD}. When such threshold is reached, the open-drain output is turned off, allowing the external pull-up to recharge the capacitor. The driver outputs restart following the input pins as soon as the voltage at the $\overline{SD}$/OD pin reaches the higher threshold of the $\overline{SD}$ logic input. The smart shutdown system gives the possibility to increase the time constant of the external RC network (that determines the disable time after the fault event) up to very large values without increasing the delay time of the protection.

Any external signal provided to the $\overline{SD}$ pin is not latched and can be used as control signal in order to perform, for instance, PWM chopping through this pin. In fact when a PWM signal is applied to the $\overline{SD}$ input and the logic inputs of the gate driver are stable, the outputs switch from the low level to the state defined by the logic inputs and vice versa.

8 Typical application diagram

Figure 7. Typical application diagram

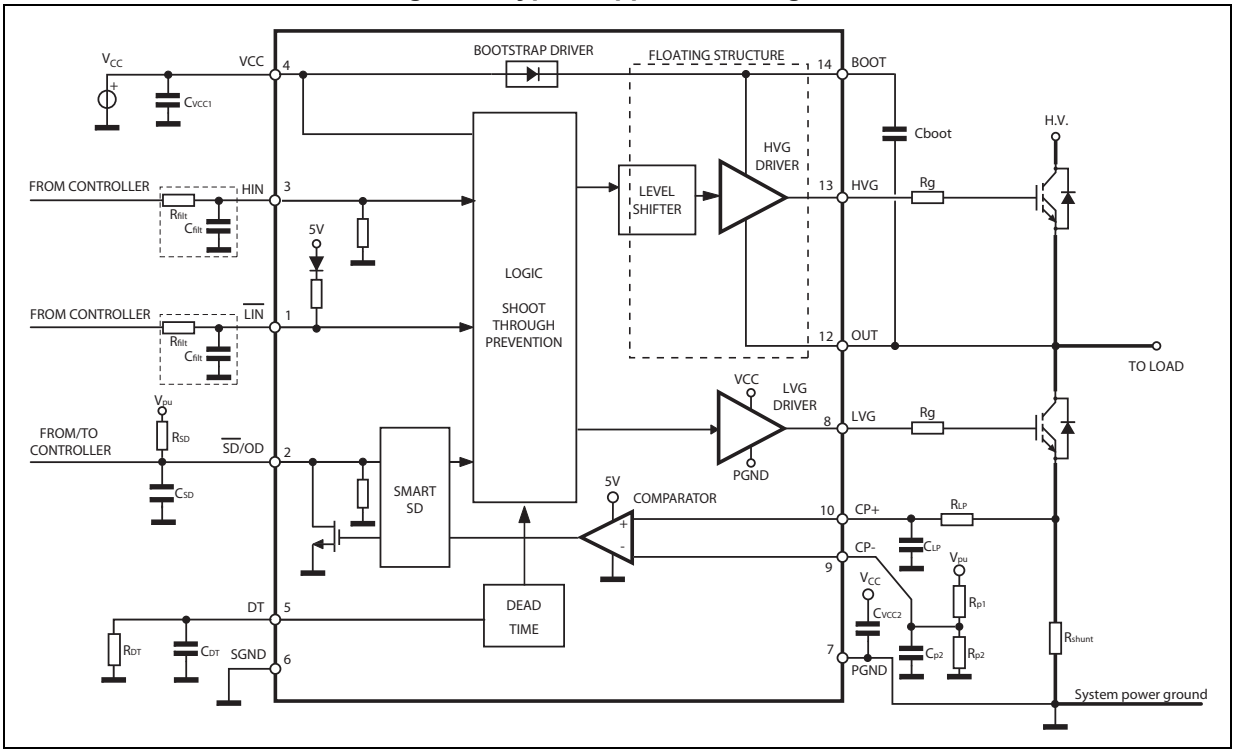
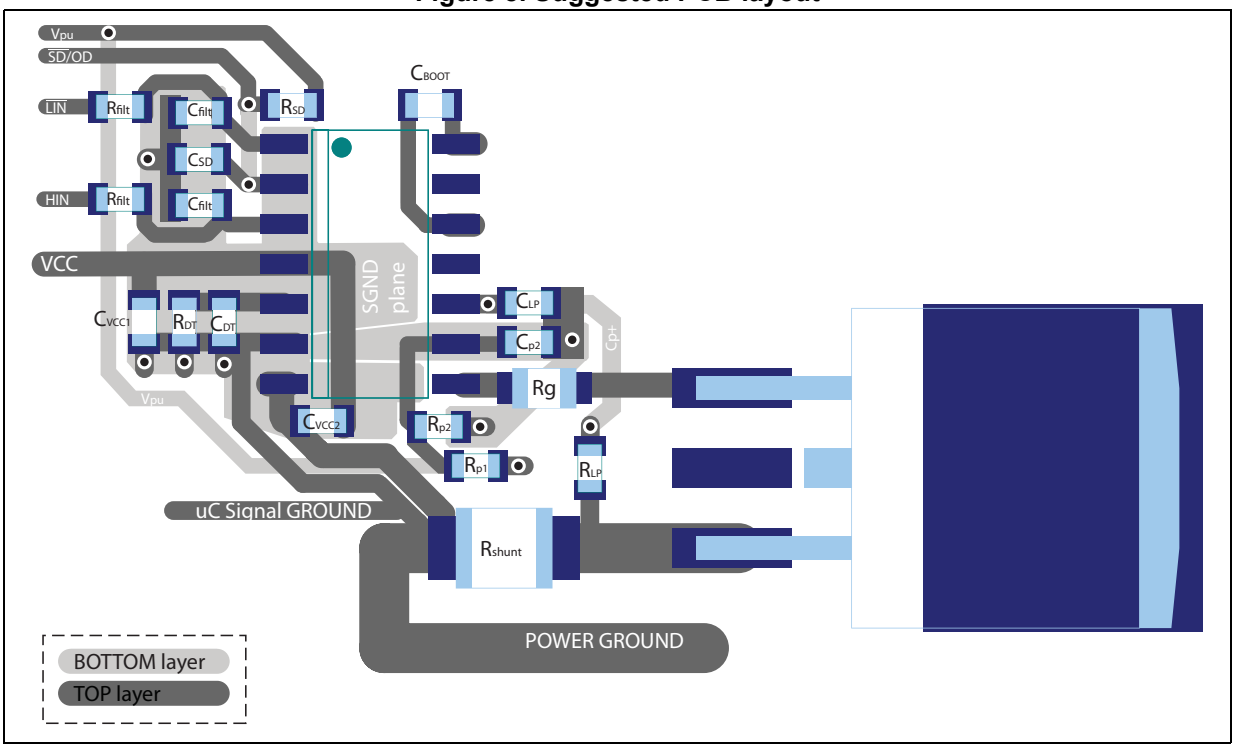


Figure 8. Suggested PCB layout



9 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is usually accomplished by a high voltage fast recovery diode (*Figure 9*). In the L6491 an integrated structure replaces the external diode.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} >>> C_{EXT}$$

if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop is 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has also to take into account the leakage and quiescent losses.

HVG steady-state consumption is lower than 120 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply C_{EXT} with 0.6 µC. This charge on a 1 µF capacitor means a voltage drop of 0.6 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to SGND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 175 Ω). At low frequency this drop can be neglected. Anyway, the rise of frequency has to take into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{DS(on)}$$

where Q_{gate} is the gate charge of the external power MOS, $R_{DS(on)}$ is the on resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

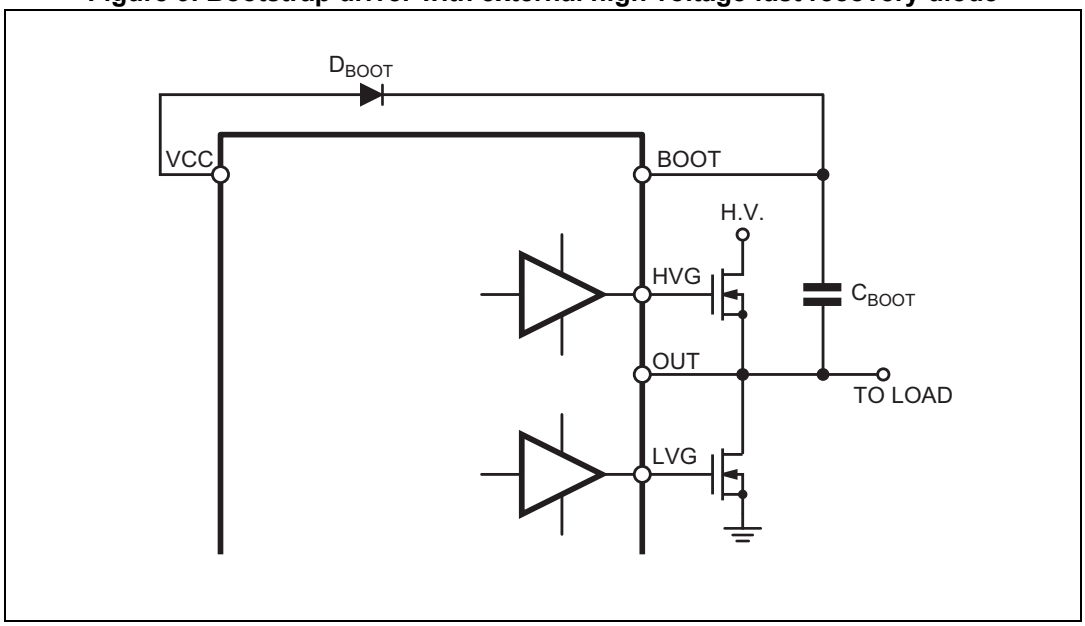
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 175\Omega \sim 1V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 9. Bootstrap driver with external high voltage fast recovery diode



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 10. SO-14 package outline

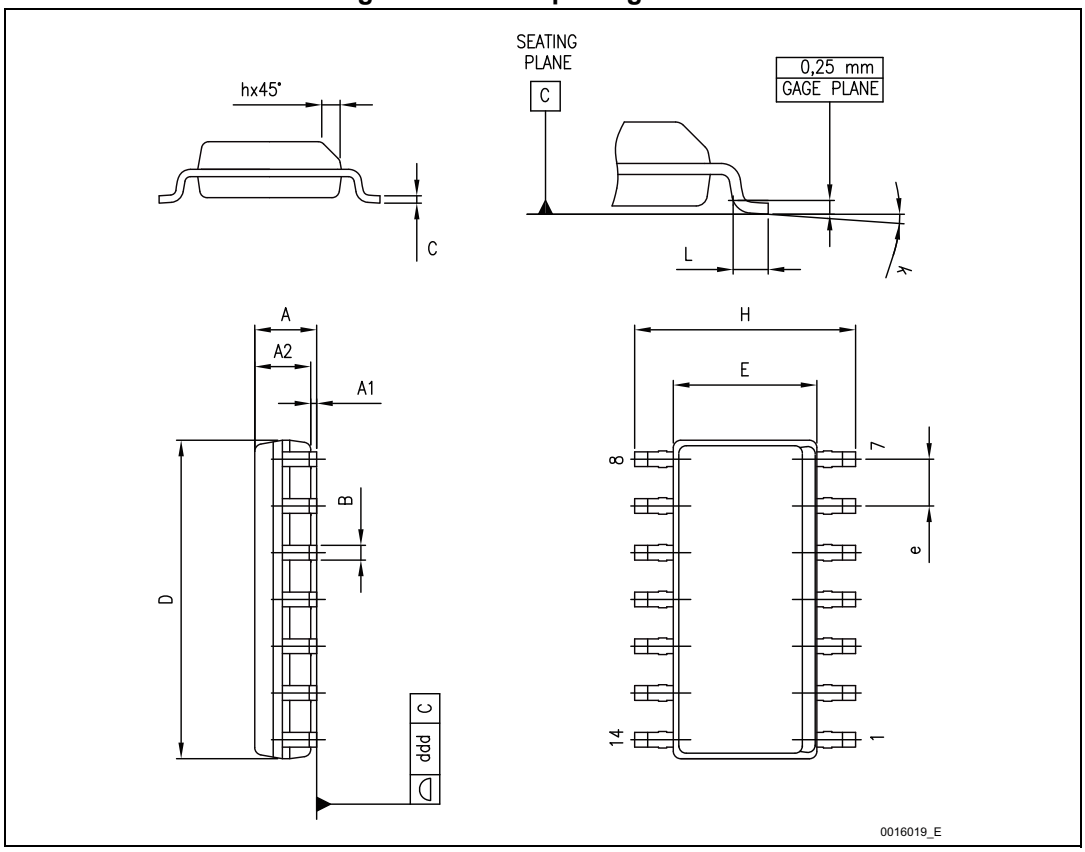
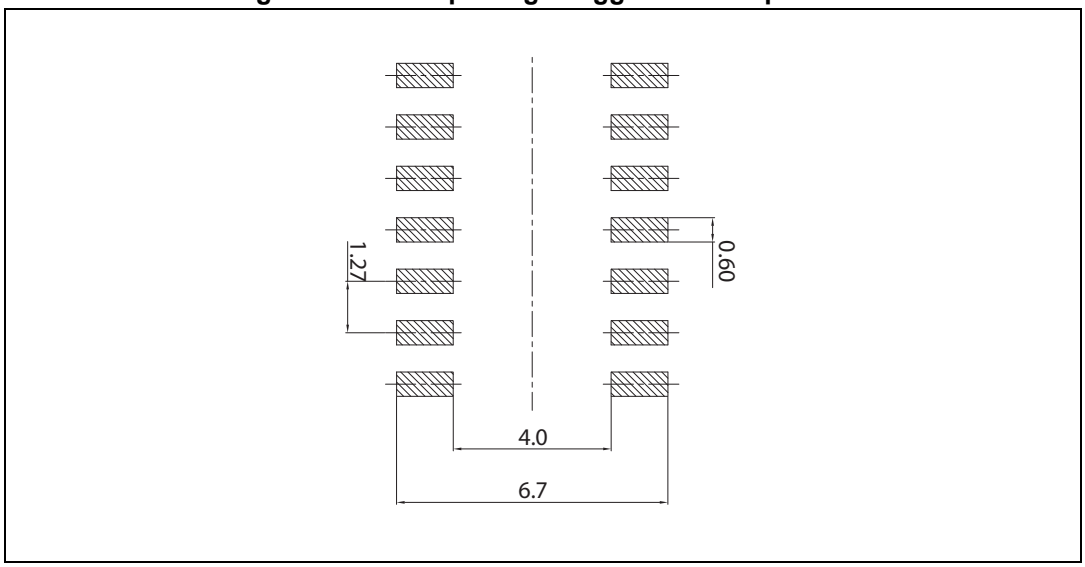


Table 10. SO-14 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	8.55		8.75
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
k	0		8
ddd			0.10

Figure 11. SO-14 package suggested land pattern



11 Revision history

Table 11. Document revision history

Date	Revision	Changes
11-Mar-2015	1	Initial release.