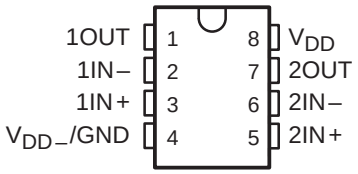
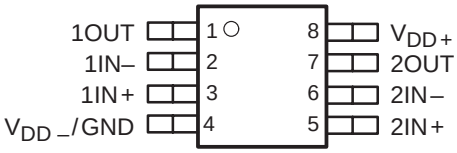
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  T_A = –40°C to 85°C . . . 2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail and up to V_{DD} –1 V at T_A = 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

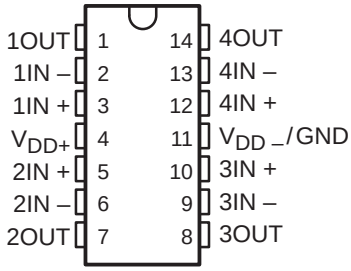
TLV2322
D OR P PACKAGE
(TOP VIEW)



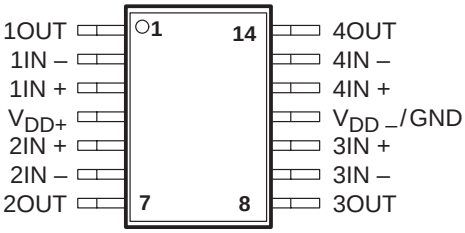
TLV2322
PW PACKAGE
(TOP VIEW)



TLV2324
D OR N PACKAGE
(TOP VIEW)



TLV2324
PW PACKAGE
(TOP VIEW)



description

The TLV232x operational amplifiers are in a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low-power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier specified at only 27 μA over its full temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES				CHIP FORM§ (Y)
		SMALL OUTLINE† (D)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP‡ (PW)	
–40°C to 85°C	9 mV	TLV2322ID	—	TLV2322IP	TLV2322IPWLE	TLV2322Y
	10 mV	TLV2324ID	TLV2324IN	—	TLV2324IPWLE	TLV2324Y

† The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2322IDR).
‡ The PW package is only available left-end taped and reeled (e.g., TLV2322IPWLE).
§ Chip forms are tested at 25°C only.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon-gate LinCMOS technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

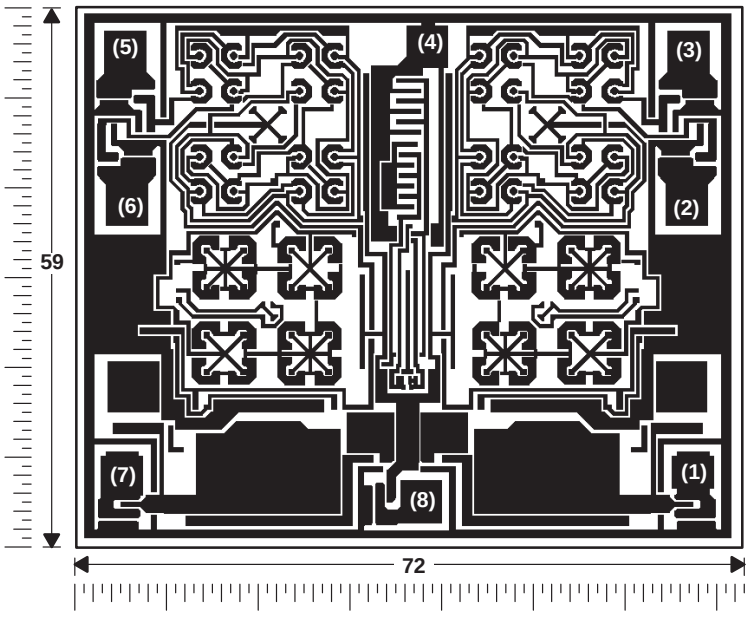
To facilitate the design of small portable equipment, the TLV232x is made available in a wide range of package options, including the small-outline and thin-shrink small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

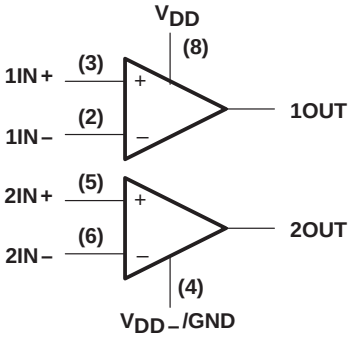
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV232x incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD can result in the degradation of the device parametric performance.

TLV2322Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2322I. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

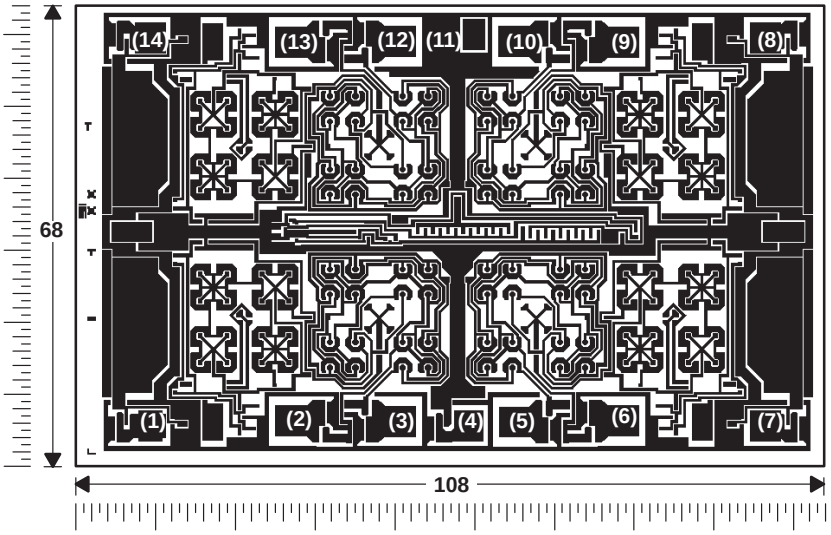
TOLERANCES ARE ±10%.

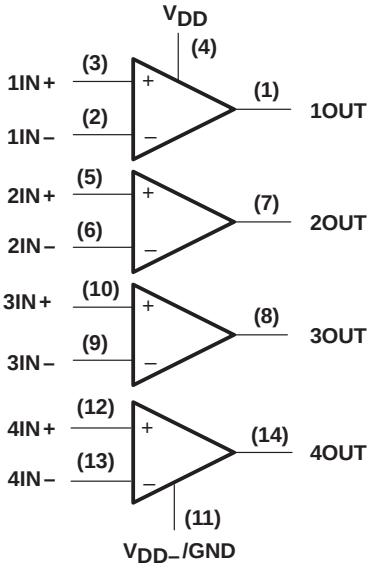
ALL DIMENSIONS ARE IN MILS.

TLV2324Y chip information

This chip, when properly assembled, display characteristics similar to the TLV2324. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

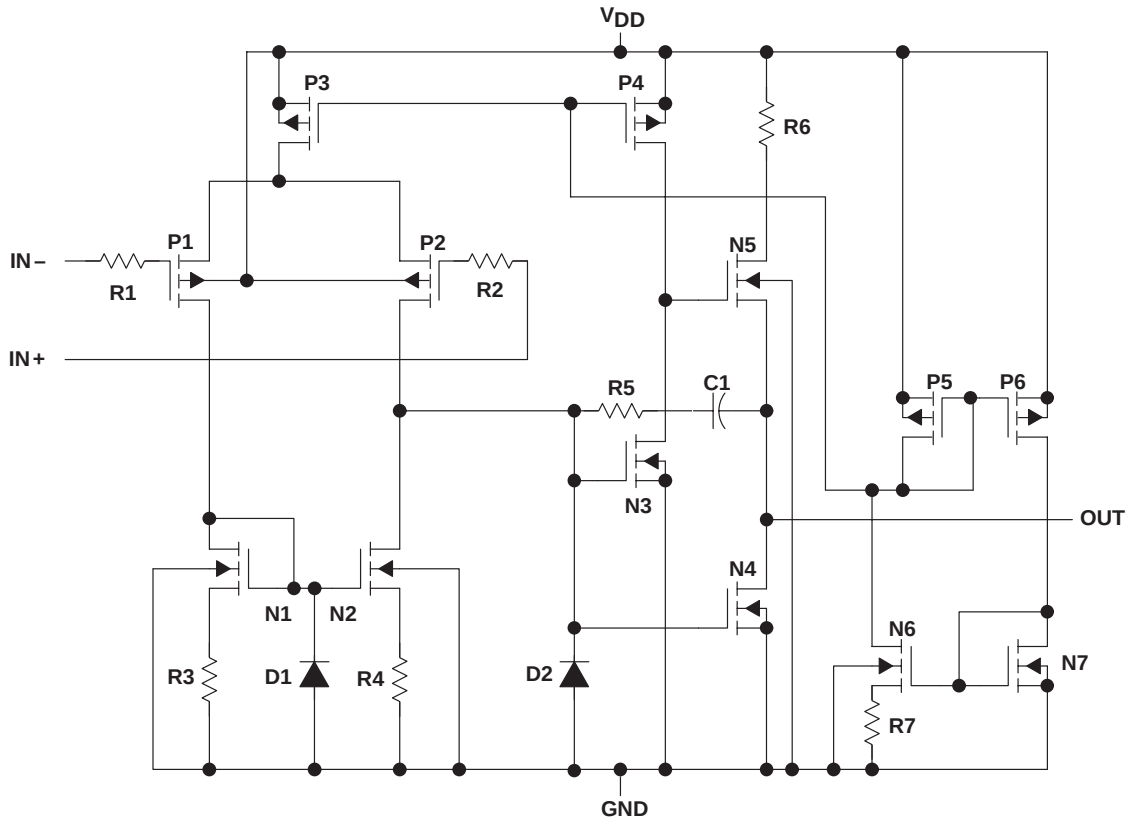
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (12) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	**TLV2342**	**TLV2344**
Transistors	54	108
Resistors	14	28
Diodes	4	8
Capacitors	2	4

† Includes both amplifiers and all ESD, bias, and trim circuitry.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 8 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $V_{DD}\pm$
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . ±30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D–8	725 mW	5.8 mW/°C	377 mW
D–14	950 mW	7.6 mW/°C	494 mW
N	1575 mW	12.6 mW/°C	819 mW
P	1000 mW	8.0 mW/°C	520 mW
PW–8	525 mW	4.2 mW/°C	273 mW
PW–14	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	–0.2	1.8	V
	V_{DD} = 5 V	–0.2	3.8	
Operating free-air temperature, T_A		–40	85	°C

TLV2322 electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2322						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = − 100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		12	34		20	34	μA
			Full range			54			54	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5

TLV2322 operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 35	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f= B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

TLV2322 operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2322			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 35	$V_{I(PP)}$ = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

TLV2324I electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLV2324I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ,	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OH} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		24	68		39	68	µA
			Full range			108			108	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, $V_{O(PP)}$ = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TLV2324I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, See Figure 35	$V_{I(PP)}$ = 1 V, C_L = 20 pF,	25°C		0.02		V/µs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f = B_1, R_L = 1 MΩ,	−40°C		39°		
				25°C		34°		
				85°C		28°		

TLV2324I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	TLV2324I			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 35	$V_{I(PP)}$= 1 V	25°C		0.03		V/µs
				85°C		0.03		
			$V_{I(PP)}$ = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 36	R_S = 20 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 35	25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_I = 10 mV, R_L = 1 MΩ,	C_L = 20 pF, See Figure 37	25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_I = 10 mV, C_L = 20 pF, See Figure 37	f = B_1, R_L = 1 MΩ,	−40°C		38°		
				25°C		34°		
				85°C		28°		

TLV2322Y electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2322Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 1 MΩ		1.1			1.1		mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)				–0.3 to 2.3			–0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = –1 mA	V_{ID} = –100 mV,		1.9			3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = 100 mV,		115			95		mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 1 MΩ,		400			520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,		88			94		dB
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{ID})	V_O = 1 V, R_S = 50 Ω	V_{IC} = 1 V,		86			86		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		12			20		μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TLV2322Y electrical characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS		TLV2324Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, R_S = 50 Ω,	V_{IC} = 1 V, R_L = 1 MΩ		1.1			1.1		mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V,	V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)				–0.3 to 2.3			–0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, I_{OH} = –1 mA	V_{ID} = 100 mV,		1.9			3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, I_{OL} = 1 mA	V_{ID} = 100 mV,		115			95		mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, See Note 6	R_L = 1 MΩ,		400			520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, R_S = 50 Ω	V_{IC} = V_{ICR}min,		88			94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{ID}$)	V_O = 1 V, R_S = 50 Ω	V_{IC} = 1 V,		86			86		dB
I_{DD}	Supply current	V_O = 1 V, No load	V_{IC} = 1 V,		24			39		μA

NOTES: 4. The typical values of input bias current offset current below 5 pA are determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1 – 4
α_{VIO}	Input offset voltage temperature coefficient	Distribution	5 – 8
I_{IB}	Input bias current	vs Free-air temperature	9
I_{IO}	Input offset current	vs Free-air temperature	9
V_{IC}	Common-mode input voltage	vs Supply voltage	10
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	11 12 13
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Free-air temperature vs Differential input voltage vs Low-level output current	14 15, 16 17 18
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	19 20 21, 22
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	23 24, 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	28
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	29 30
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	31 32 33
	Phase shift	vs Frequency	21, 22
V_n	Equivalent input noise voltage	vs Frequency	34

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE**

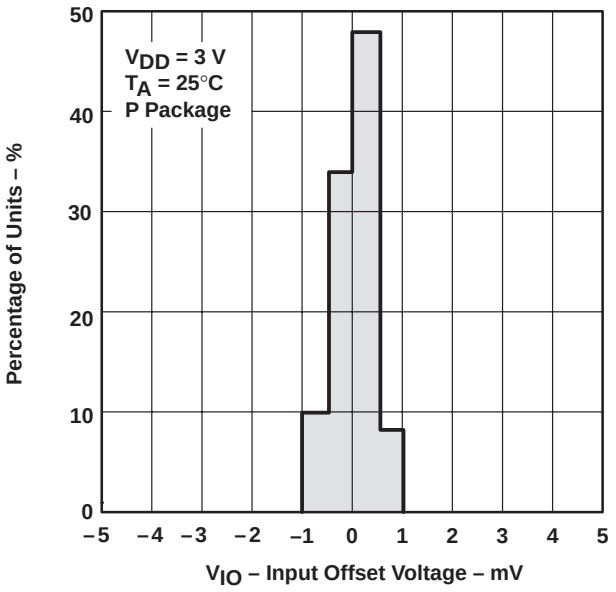


Figure 1

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE**

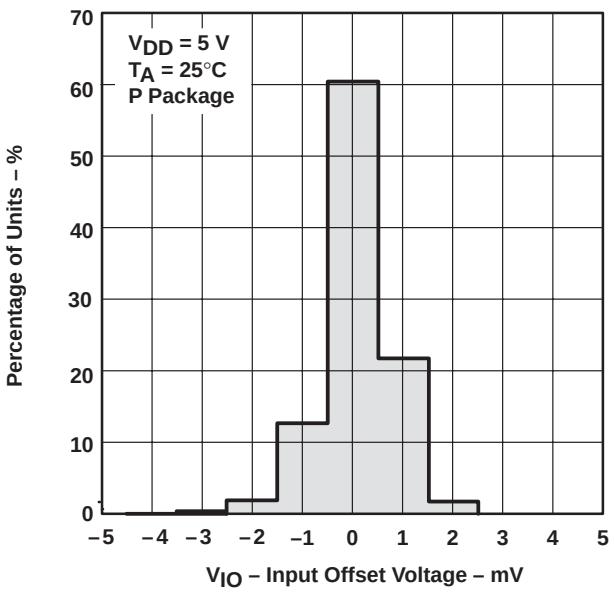


Figure 2

**DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE**

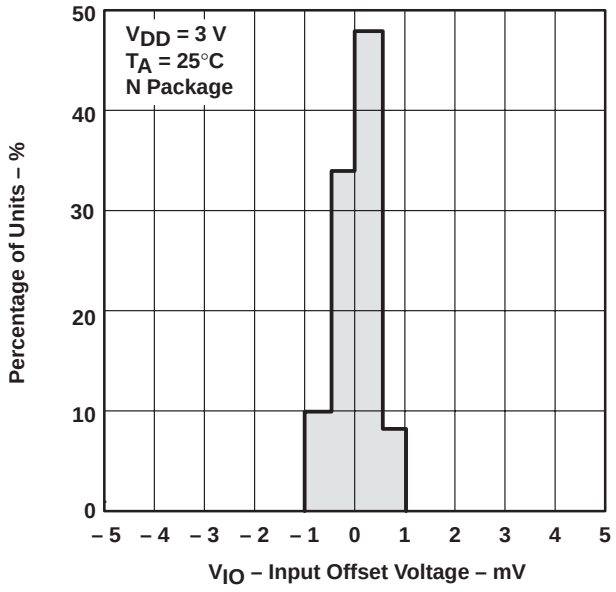


Figure 3

**DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE**

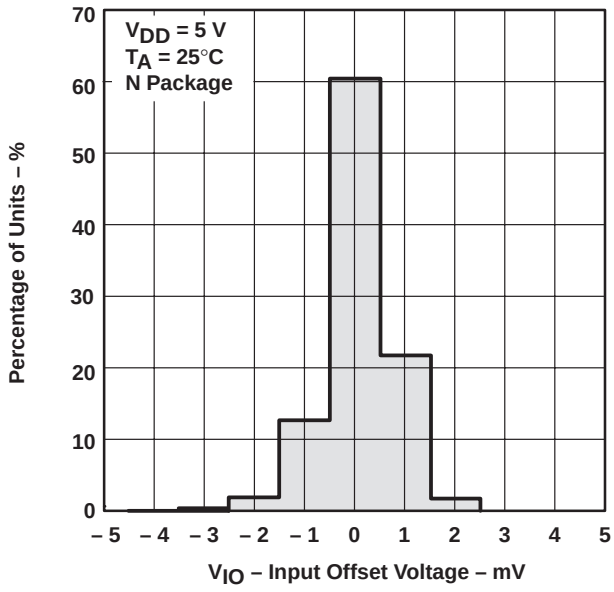


Figure 4

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

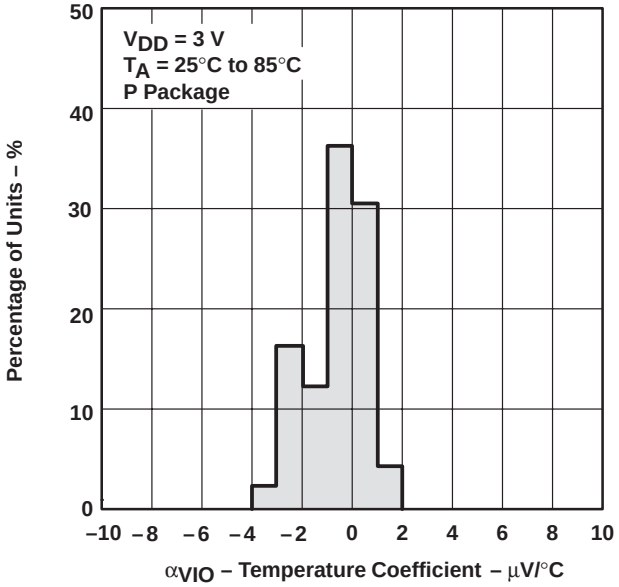


Figure 5

**DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

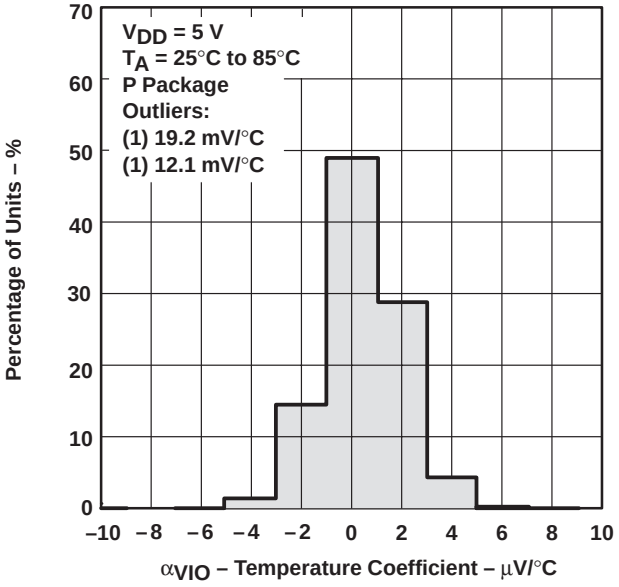


Figure 6

**DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

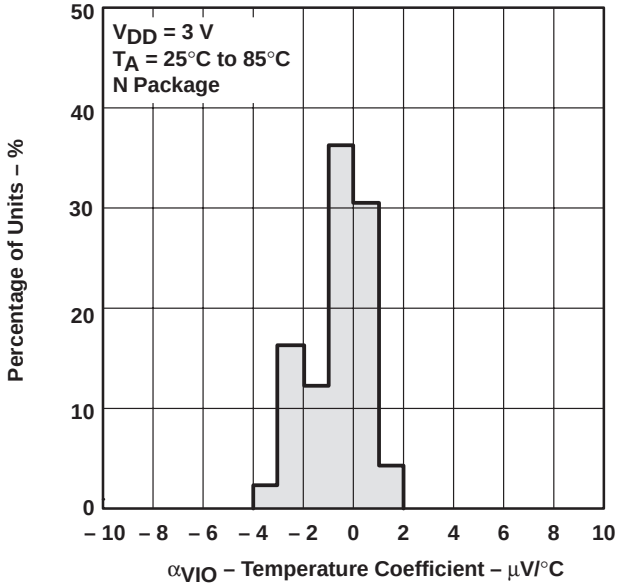


Figure 7

**DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

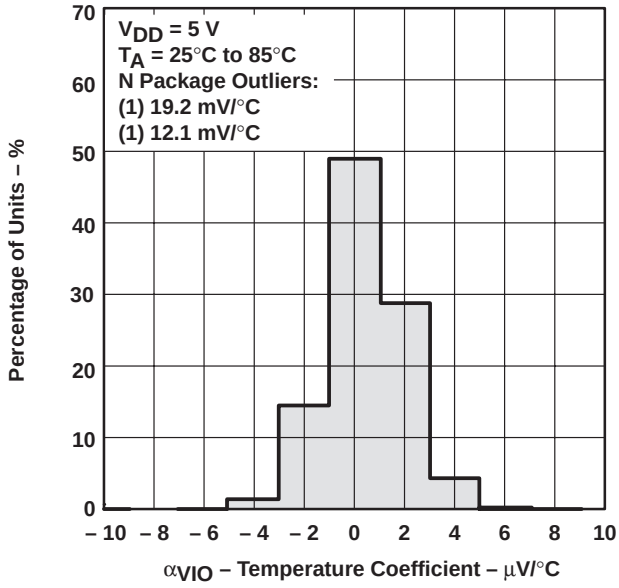
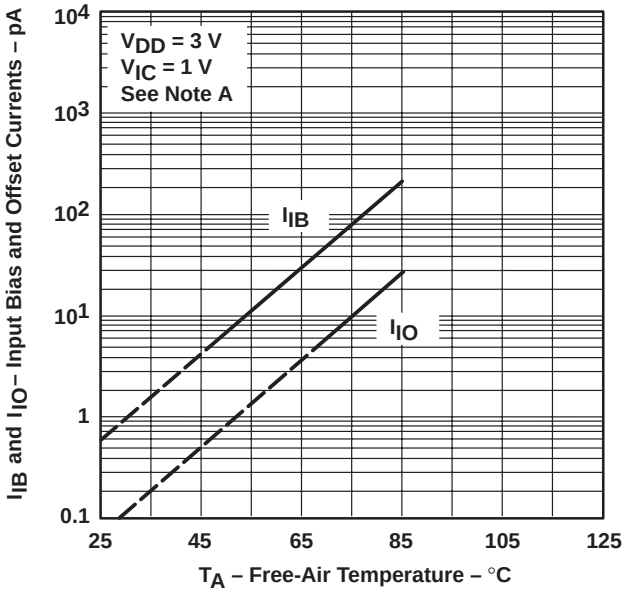


Figure 8

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 9

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

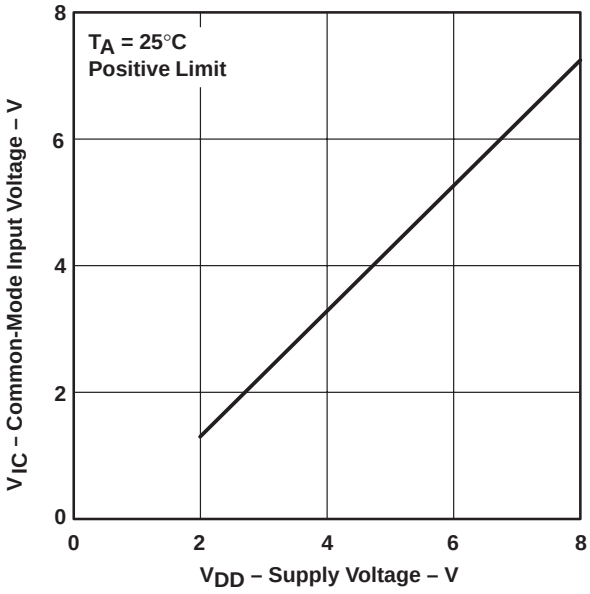


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

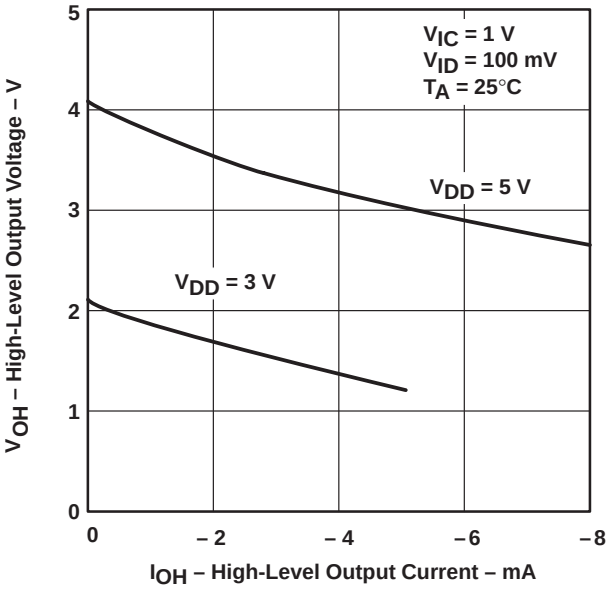


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

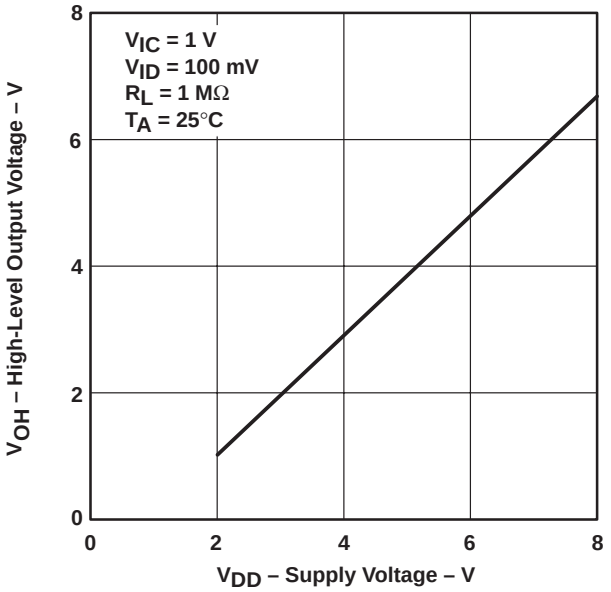


Figure 12

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

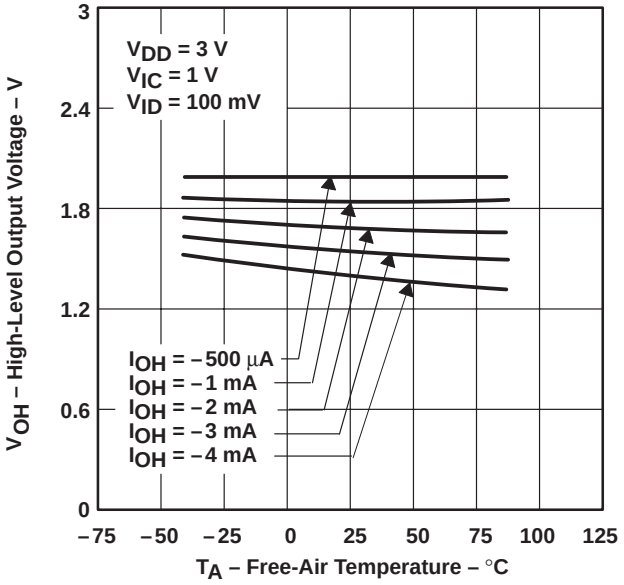


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

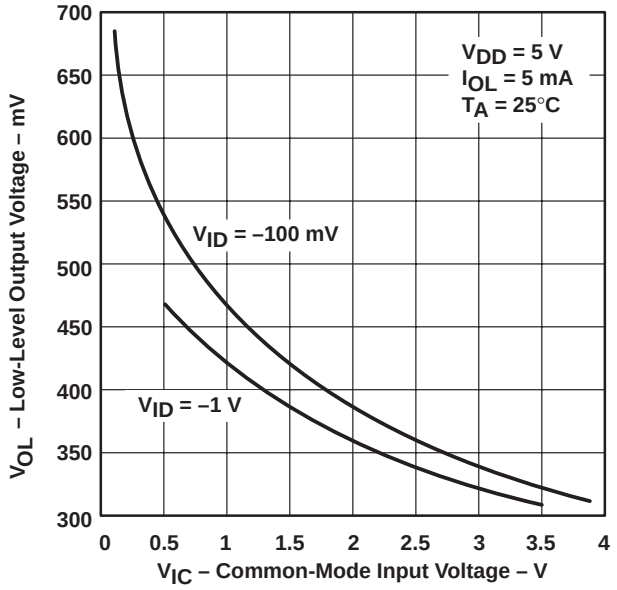


Figure 14

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

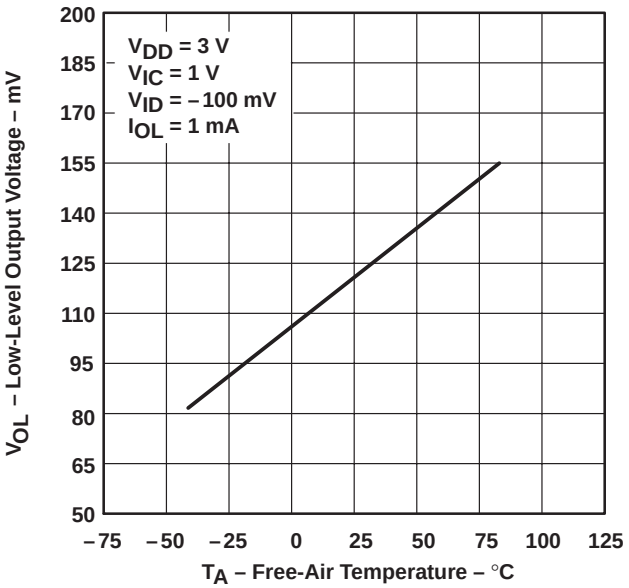


Figure 15

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

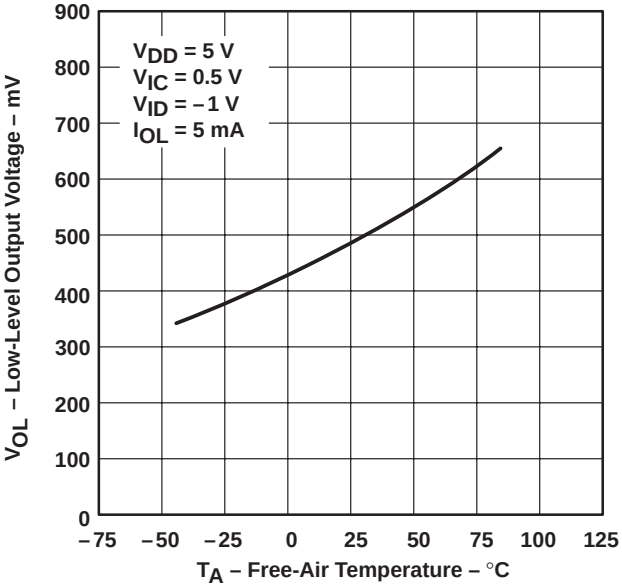


Figure 16

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

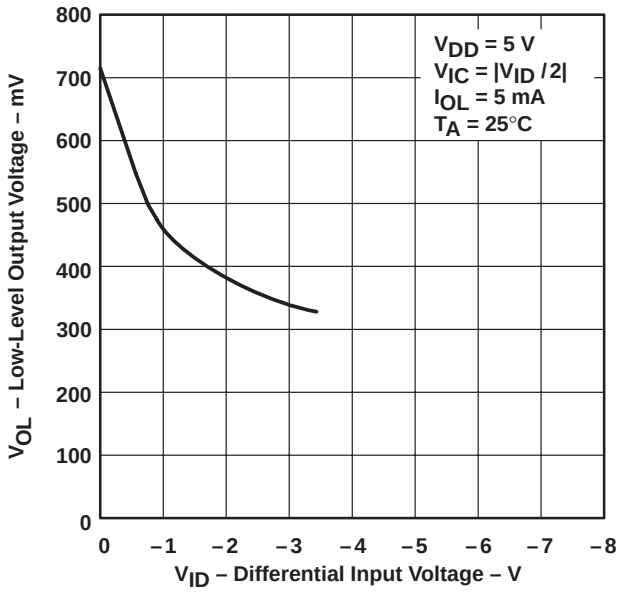


Figure 17

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

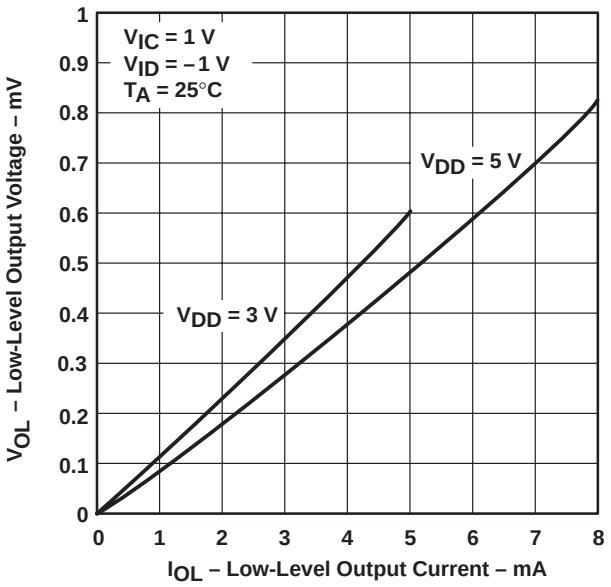


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

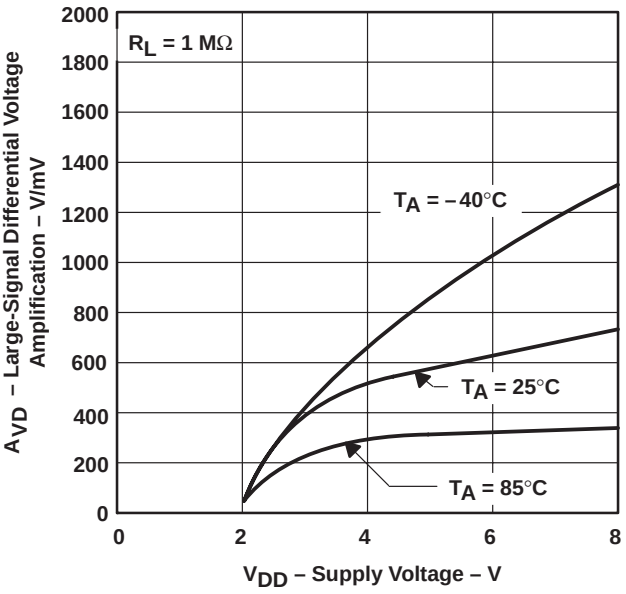


Figure 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

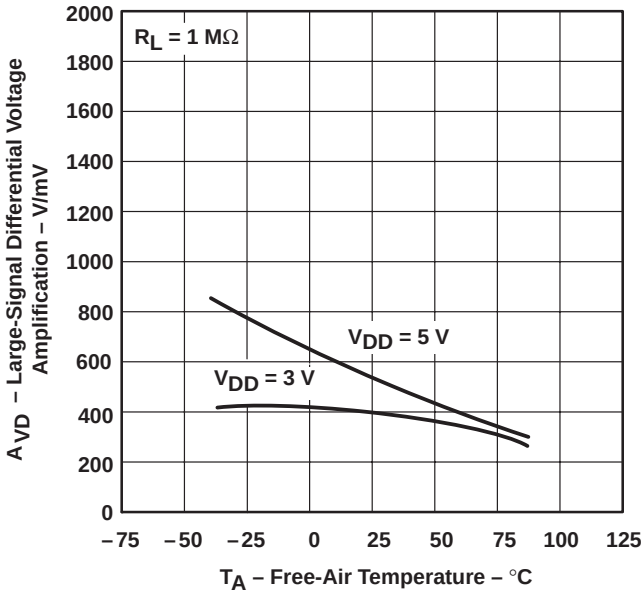


Figure 20

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

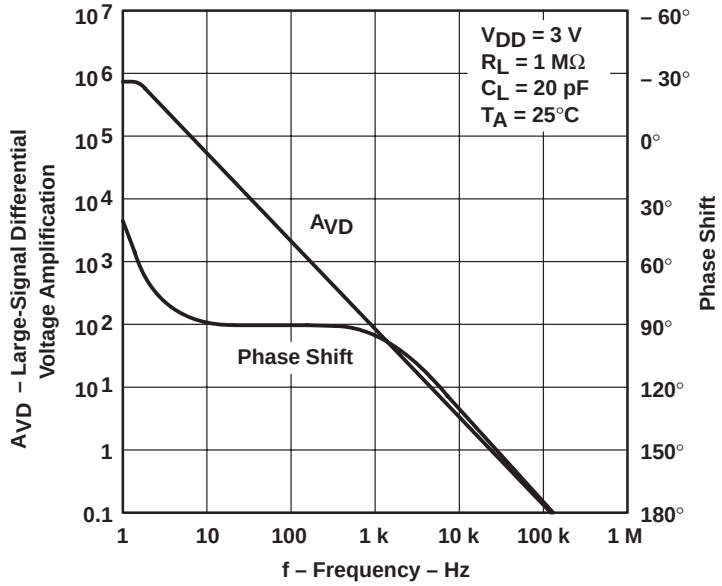


Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

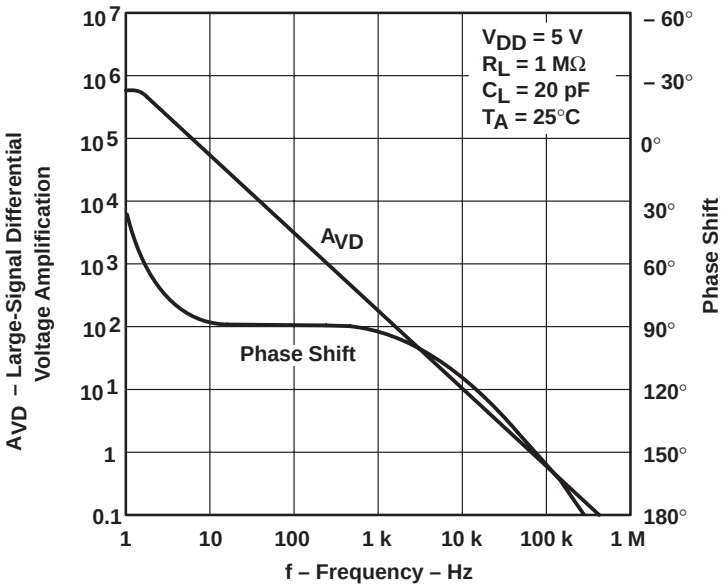


Figure 22

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

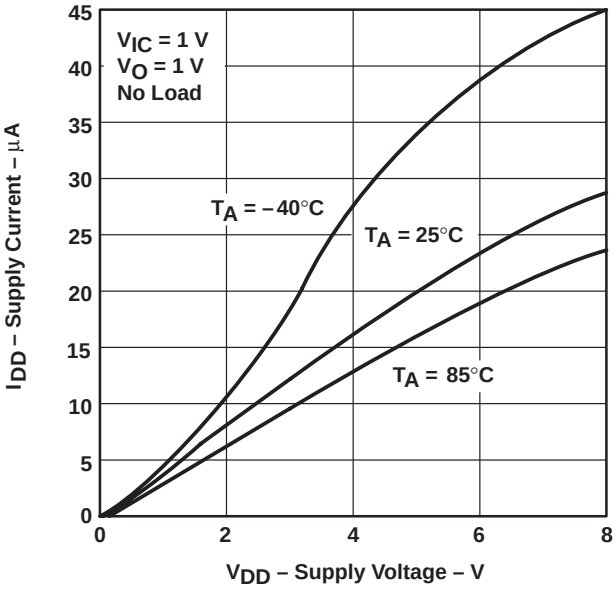


Figure 23

TLV2322 SUPPLY CURRENT vs FREE-AIR TEMPERATURE

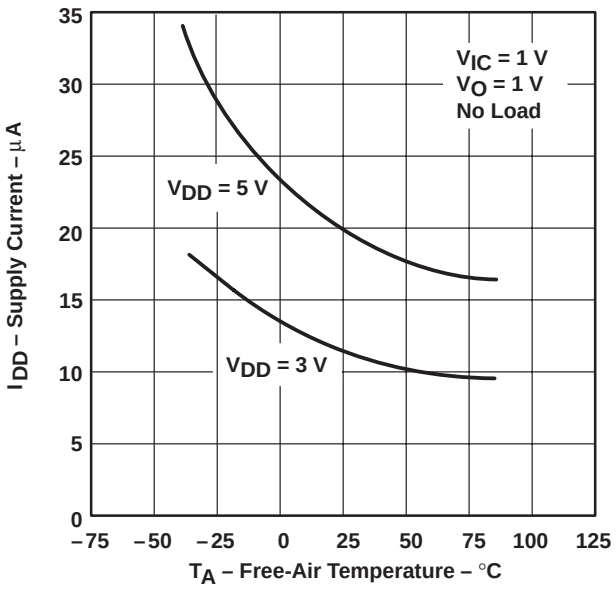


Figure 24

TLV2324 SUPPLY CURRENT vs FREE-AIR TEMPERATURE

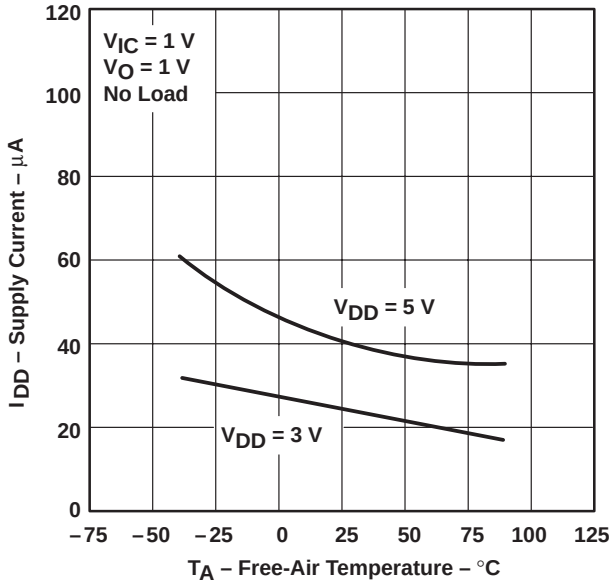


Figure 25

SLEW RATE vs SUPPLY VOLTAGE

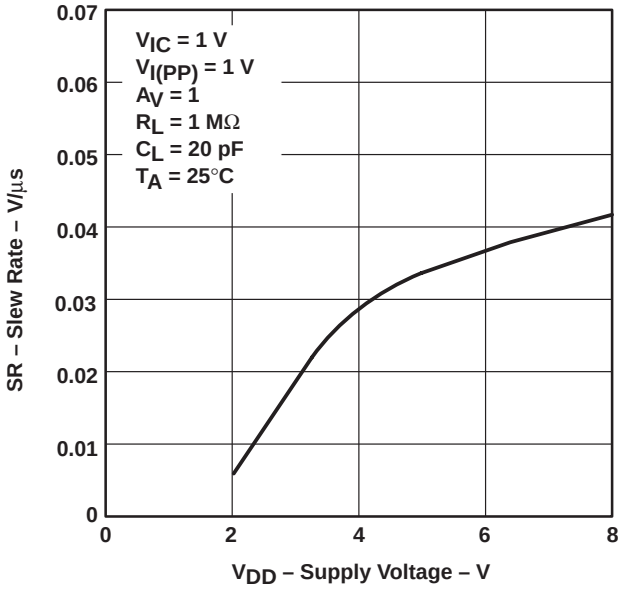


Figure 26

TYPICAL CHARACTERISTICS

SLEW RATE vs FREE-AIR TEMPERATURE

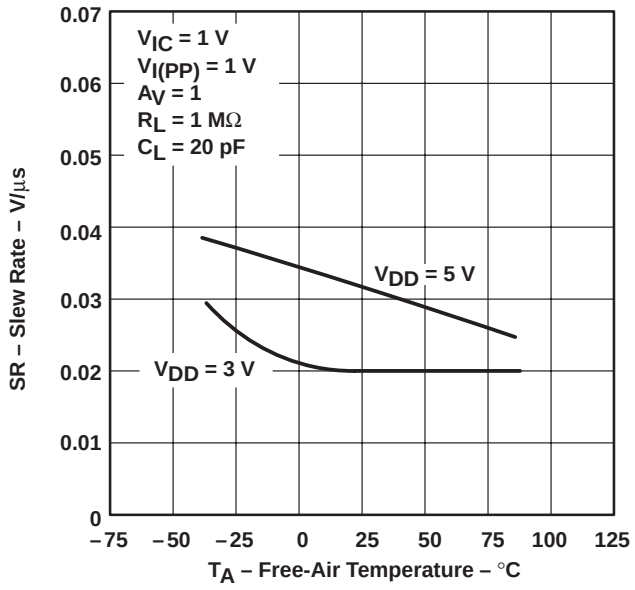


Figure 27

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

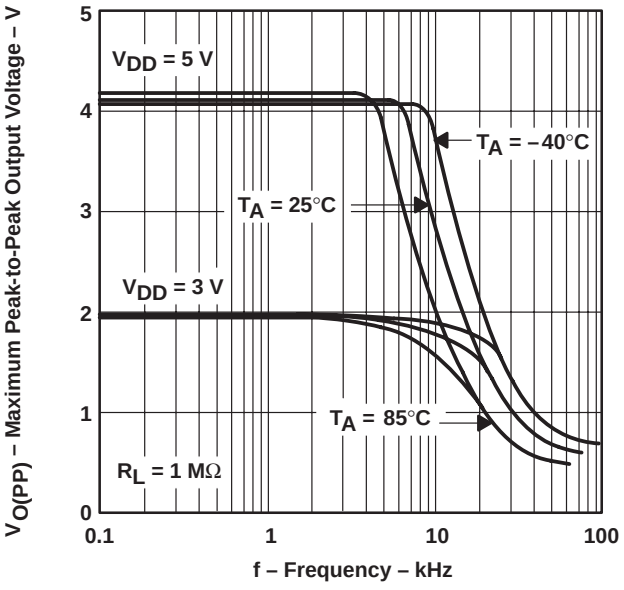


Figure 28

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

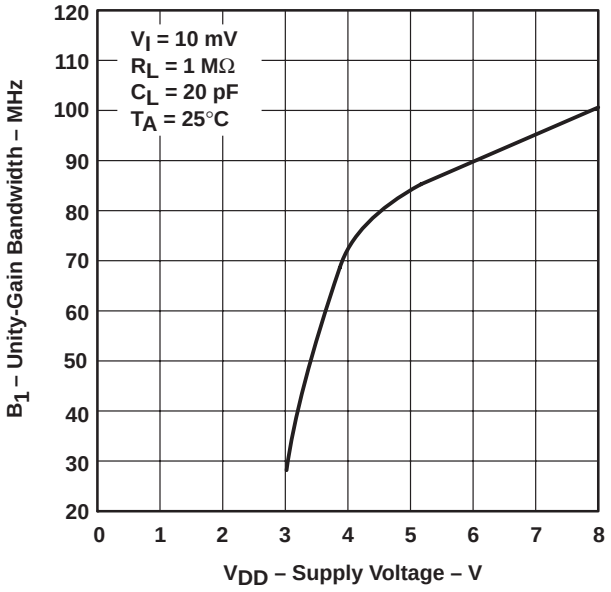


Figure 29

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

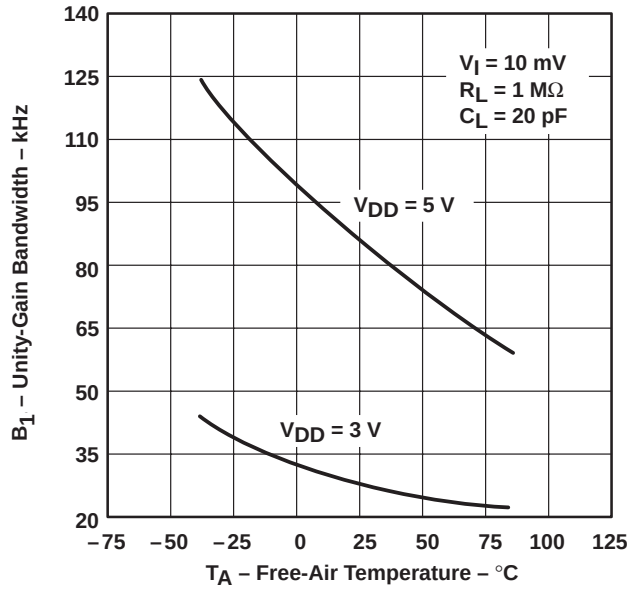


Figure 30

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

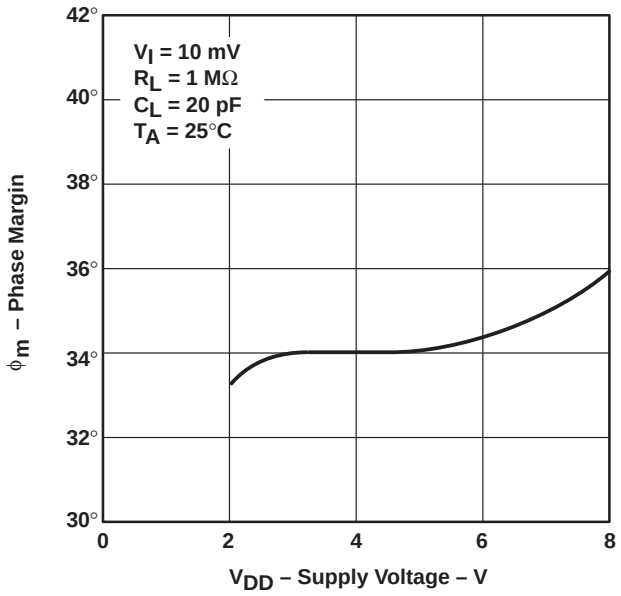


Figure 31

PHASE MARGIN vs FREE-AIR TEMPERATURE

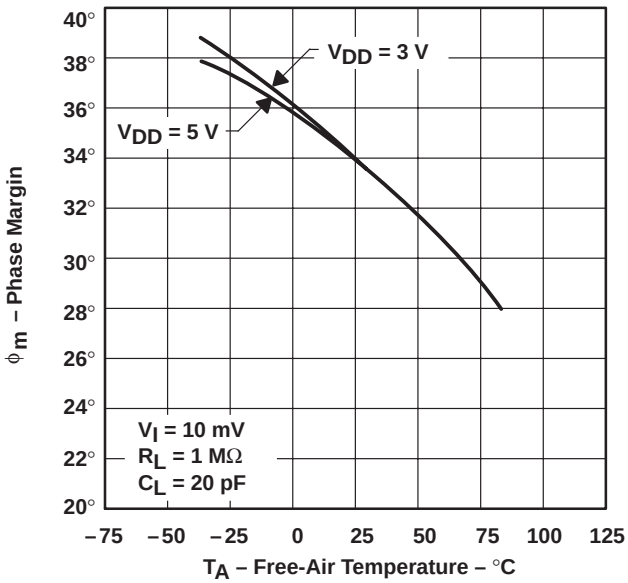


Figure 32

PHASE MARGIN vs LOAD CAPACITANCE

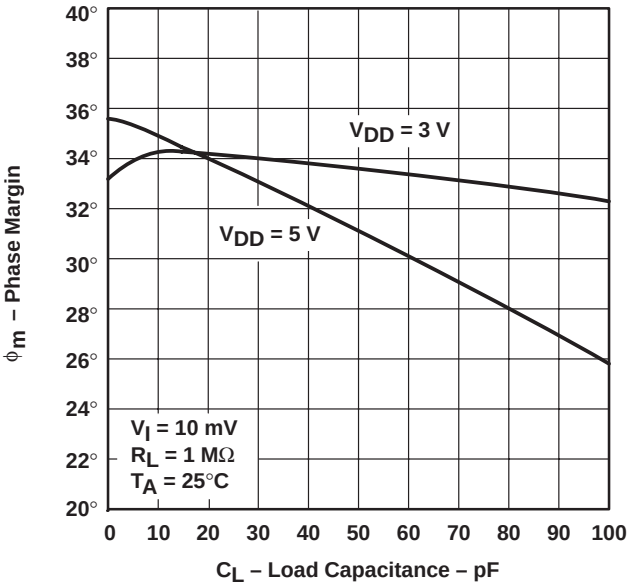


Figure 33

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

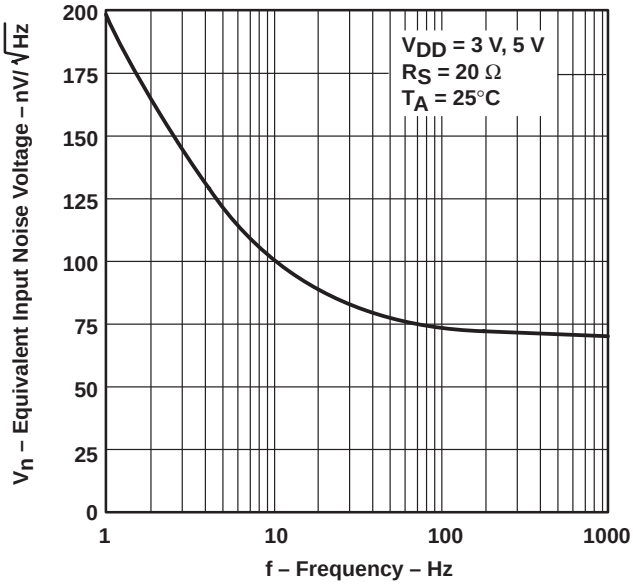
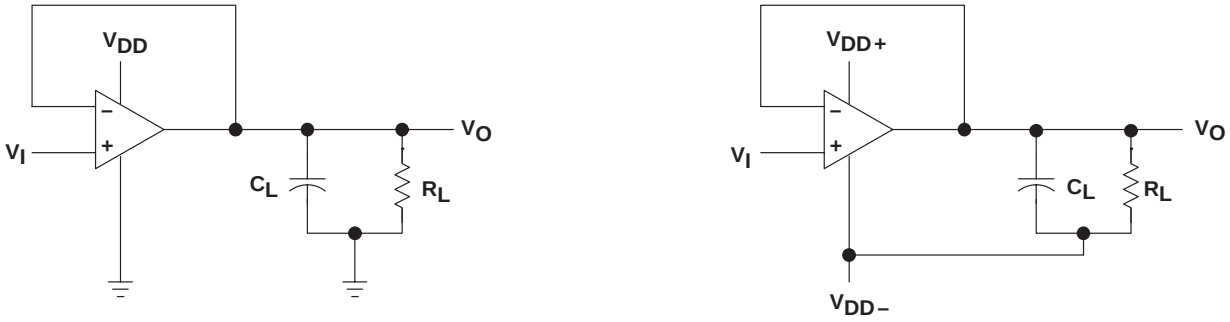


Figure 34

PARAMETER MEASUREMENT INFORMATION

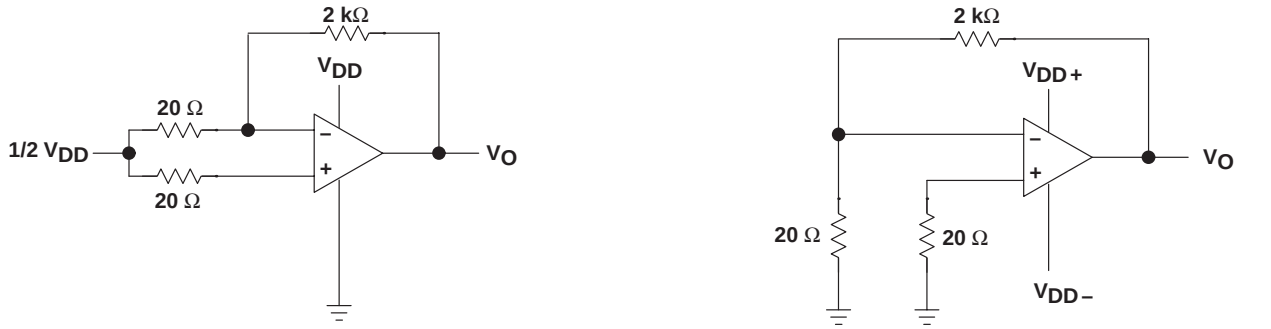
single-supply versus split-supply test circuits

Because the TLV232x is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.



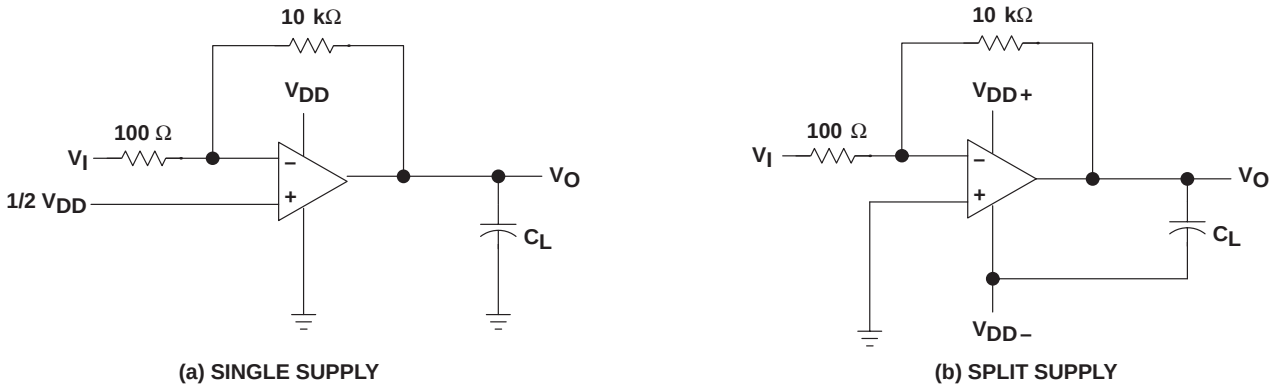
(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 35. Unity-Gain Amplifier



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 36. Noise-Test Circuits



(a) SINGLE SUPPLY (b) SPLIT SUPPLY

Figure 37. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV232x operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 38). Leakages that would otherwise flow to the inputs are shunted away.
- Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

  Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into a test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

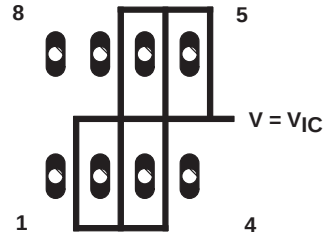


Figure 38. Isolation Metal Around Device Inputs (P package)

low-level output voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance that can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. These measurements should be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 35. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 39). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

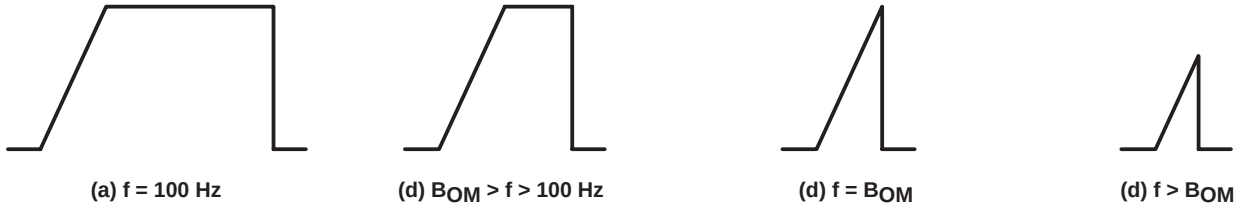


Figure 39. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

APPLICATION INFORMATION

single-supply operation

While the TLV232x performs well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

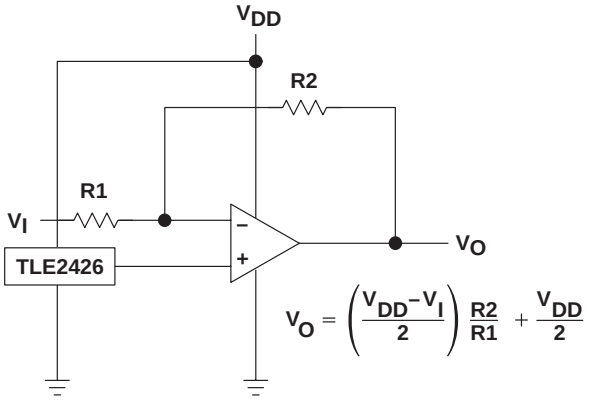


Figure 40. Inverting Amplifier With Voltage Reference

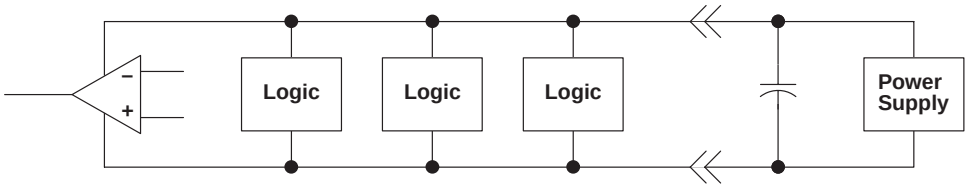
Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a preferred technique is to use a virtual-ground generator such as the TLE2426 (see Figure 40). The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power and is suitable for supply voltages of greater than 4 V.

APPLICATION INFORMATION

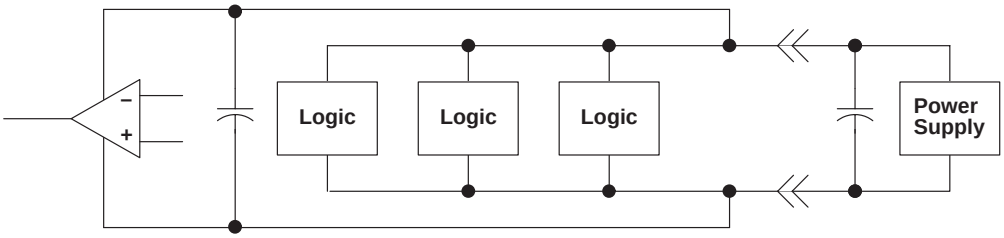
single-supply operation (continued)

The TLV232x works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- Power the linear devices from separate bypassed supply lines (see Figure 41); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON-SUPPLY RAILS



(b) SEPARATE-BYPASSED SUPPLY RAILS (preferred)

Figure 41. Common Versus Separate Supply Rails

input characteristics

The TLV232x is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower the range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV232x very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLV232x is well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 38 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 42).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

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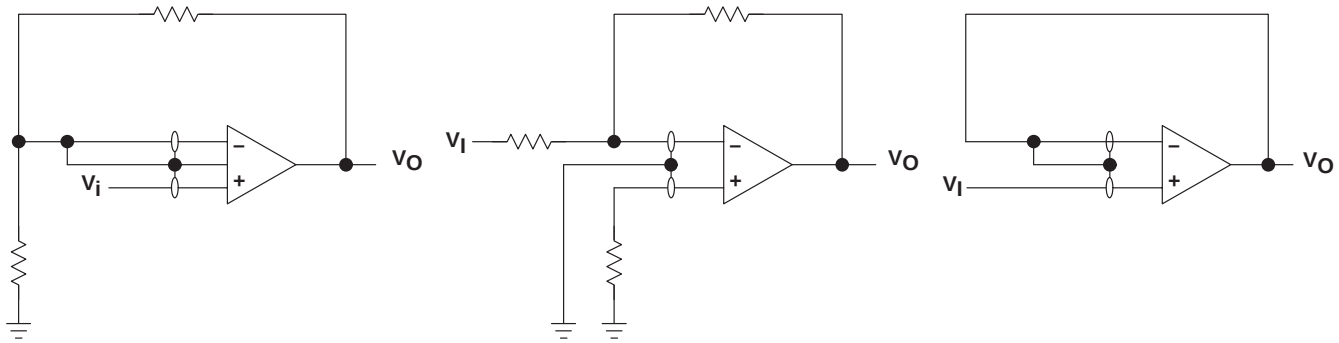
input characteristics (continued)



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 42. Guard-Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLV232x result in a very low noise current, which is insignificant in most applications. This feature makes the device especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

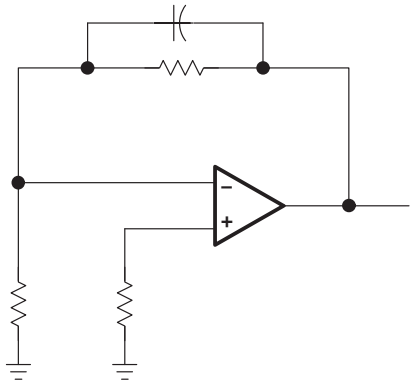


Figure 43. Compensation for Input Capacitance

electrostatic-discharge protection

The TLV232x incorporates an internal electrostatic-discharge (ESD)-protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD can result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV232x inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal-protection diodes should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage

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by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV232x is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although the TLV232x possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 44). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

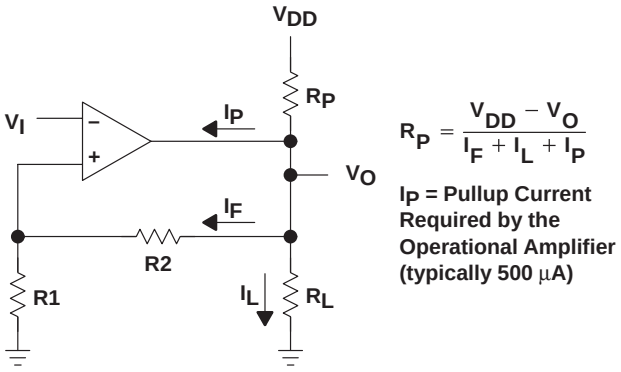


Figure 44. Resistive Pullup to Increase V_{OH}

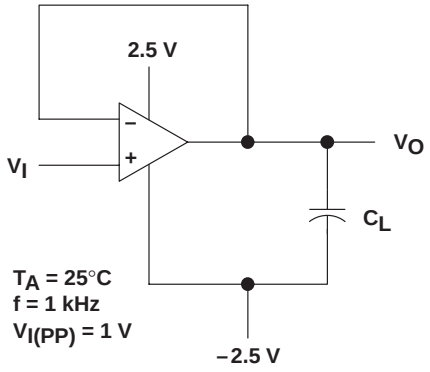
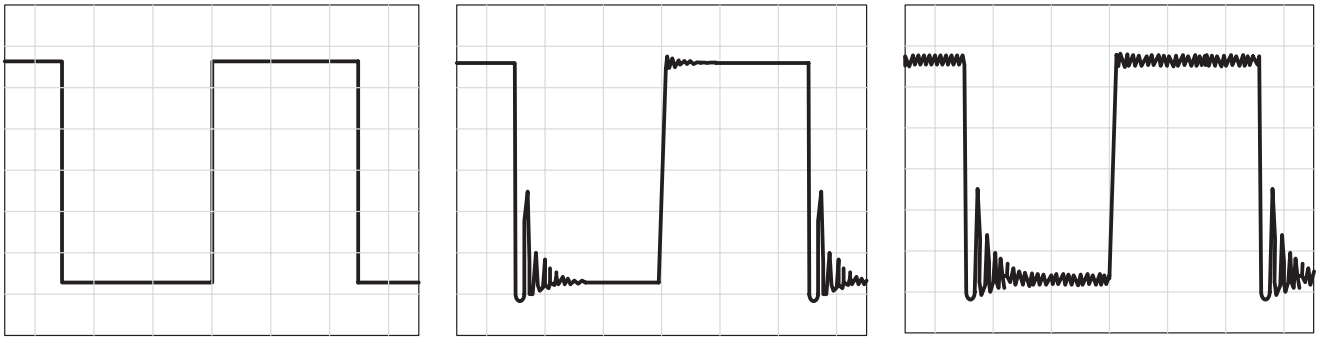


Figure 45. Test Circuit for Output Characteristics

All operating characteristics of the TLV232x are measured using a 20-pF load. The device drives higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 45 and Figure 46). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.

APPLICATION INFORMATION

output characteristics (continued)



(a) C_L = 20 pF, R_L = NO LOAD

(b) C_L = 260 pF, R_L = NO LOAD

(c) C_L = 310 pF, R_L = NO LOAD

Figure 46. Effect of Capacitive Loads

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2322ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2322I	
TLV2322IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2322I	Samples
TLV2322IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLV2322IP	Samples
TLV2322IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2322	Samples
TLV2324ID	LIFEBUY	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV2324I	
TLV2324IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV2324I	Samples
TLV2324IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TLV2324IN	Samples
TLV2324IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2324	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

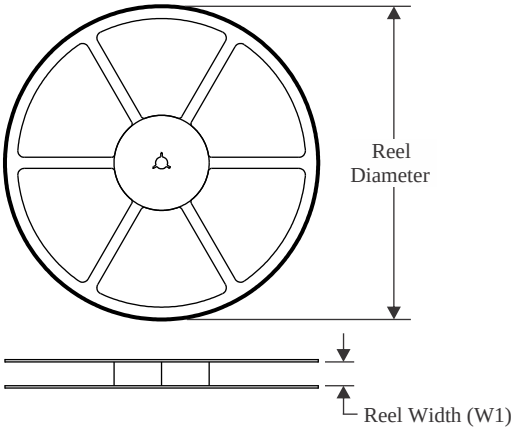
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

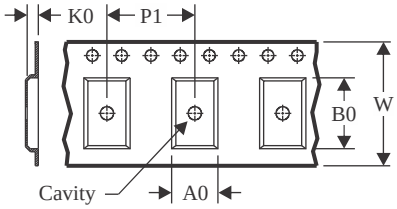
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

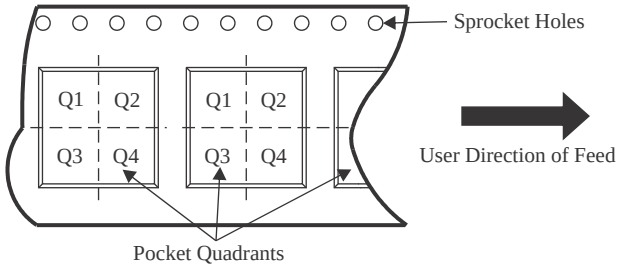


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

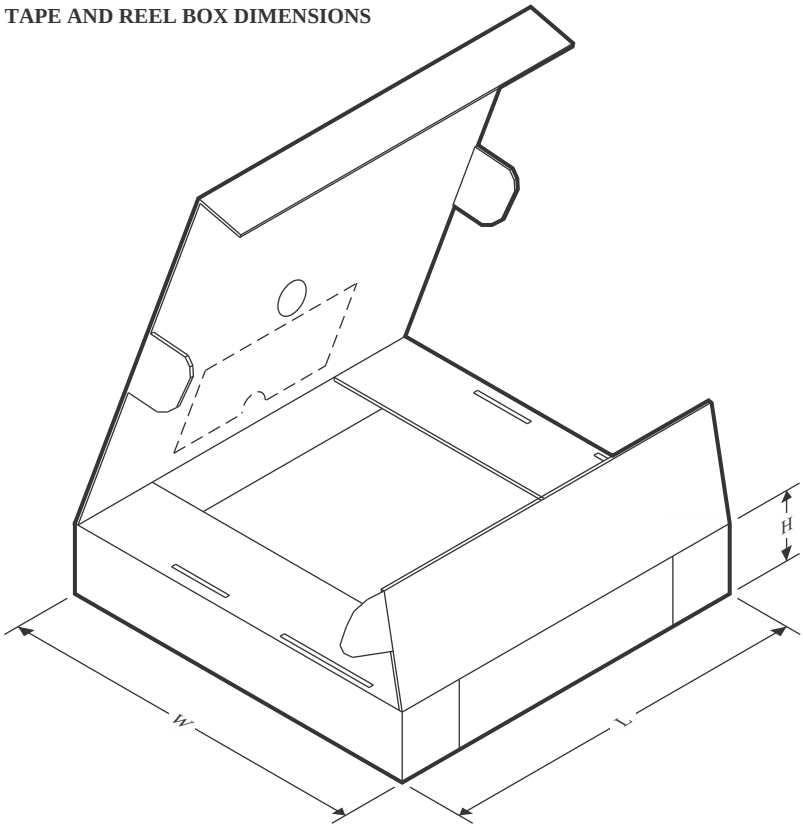
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2322IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2322IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

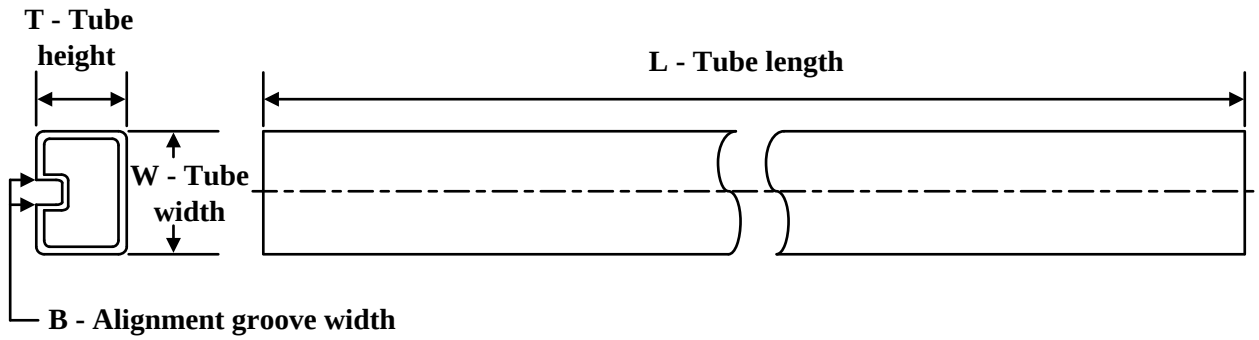
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2322IDR	SOIC	D	8	2500	340.5	336.1	25.0
TLV2322IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV2324IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2324IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2322ID	D	SOIC	8	75	507	8	3940	4.32
TLV2322ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2322IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2324ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2324IN	N	PDIP	14	25	506	13.97	11230	4.32

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