



Product Change Notification / SYST-16OGOQ119

Date:

20-Jul-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - AVR128DA28/32/48/64 Preliminary Data Sheet

Affected CPNs:

[SYST-16OGOQ119_Affected_CPN_07202021.pdf](#)

[SYST-16OGOQ119_Affected_CPN_07202021.csv](#)

Notification Text:

SYST-16OGOQ119

Microchip has released a new Product Documents for the AVR128DA28/32/48/64 Preliminary Data Sheet of devices. If you are using one of these devices please read the document located at [AVR128DA28/32/48/64 Preliminary Data Sheet](#).

Notification Status: Final

Description of Change: The following is the list of modifications:

1. Document section.
 - General improvement of the documentation and its structure
 - Updated terminology used throughout the data sheet:
 - Master is replaced by host
 - Slave is replaced by client
2. Device section:
 - Memories
 - Improved BODCFG fuse description
 - Peripherals and Architecture
 - Updated the Interrupt Vector Mapping table
 - Updated the REVID.MAJOR bit field description from 0x00 = A, 0x01 = B to 0x01 = A, 0x02 = B
 - Ordering Information

- Added note for automotive-grade ordering codes (VAO suffix)
- Package Drawings
 - Added note in the Online Package Drawings section
 - Added the Package Marking section
 - Updated 64-Pin VQFN style from MR to R4X
 - Added 32, 48 and 64-Pin VQFN Wettable Flanks packages
- 3. Hardware Guidelines section:
 - Digital Power Supply
 - Updated primary decoupling capacitor value to 100 nF
 - Added optional decoupling capacitor (C3)
 - Added note
- 4. CPU section:
 - Updated the AVR® CPU Architecture figure
 - Improved description for the RAMPZ register
- 5. NVMCTRL section:
 - Updated the NVMCTRL Block Diagram figure
 - Removed offset column from the Available Interrupt Vectors and Sources table
- 6. CLKCTRL section:
 - Updated the Phase-Locked Loop (PLL) section. Added initialization example.
 - The Auto-Tune section renamed to Manual Tuning and Auto-Tune. Added the new Manual Tuning section.
 - CLKCTRL.PLLCTRLA added to the list of registers requiring Configuration Change Protection (in the Registers Under Configuration Change Protection table)
 - Improved description of the RUNSTBY bit in the OSCHFCTRLA, OSCHFTUNE, PLLCTRLA, OSC32KCTRLA and XOSC32KCTRLA registers
 - Improved description of the XOSC32KCTRLA bit fields
 - Updated the name of the MULFAC bit field in the PLLCTRLA register from Frequency Select to Multiplication Factor
 - Improved description of the PLLCTRLA.MULFAC bit field
- 7. SLPCTRL section:
 - Improved the Sleep modes section
 - Updated the Sleep Mode Activity Overview tables
 - Added the Configuration Change Protection section
 - Updated description for the VREGCTRL.HTLLEN bit field
- 8. RSTCTRL section:
 - Figures updated:
 - Block Diagram
 - MCU Start-up, RESET Tied to VDD
 - Brown-out Detector Reset
 - External Reset Characteristics
 - Figures added:
 - Watchdog Reset
 - Software Reset
 - Updated the Logic Domains Affected by Various Resets table
 - Updated the Reset Time section
- 8. CPUINT section:
 - Updated the CPUINT - Registers under Configuration Change Protection table
 - Improved the Non-Maskable Interrupts section
- 9. PORT section:
 - System Clock renamed to Peripheral clock
 - Added initialization code example in the Multi-Pin Configuration section
 - Added clarification notes in following sections:
 - Multi-Pin Configuration
 - Virtual Ports
 - PINCONFIG.ISC bit field description
- 10. BOD section:
 - The VLMCTRL register renamed to VLMCTRLA
- 11. TCA section:
 - Improved the Frequency (FRQ) Waveform Generation section:
 - Added description on WOn offset
 - Added the Offset When Counting Up and Inverting Waveform Output figures
 - Added the Offset Equation Overview table
 - Added the Single-Slope Pulse-Width Modulation in Split Mode figure

- Figures updated:
 - Timer/Counter Block Diagram
 - Single-Slope Pulse-Width Modulation
 - Dual-Slope Pulse-Width Modulation
- Added clarification notes in the following sections:
 - Single-Slope Pulse-Width Modulation
 - Dual-Slope Pulse-Width Modulation
 - Events
- Improved the Split Mode - Two 8-Bit Timer/Counters section
- Improved bit fields and register description:
 - Added clarification note in the CTRLC register description
 - Improved description for the LUPD bit field in the CTRLCLR and CTRLSET registers
 - Improved description for UPDOWN value of the EVACTA/B bit field in the EVCTRL register
- 12. TCB section:
 - General improvement of the documentation.
- 13. TCD section:
 - Updated the FAULTCTRL register bit fields name:
 - CMPxEN renamed to CMPEN
 - CMPx renamed to CMP
- 14. RTC section:
 - Removed note from the RTC Functional Description - Configure RTC section
 - Removed note from the PIT Functional Description - Initialization section
- 15. USART section:
 - Updated terminology:
 - Master is replaced by host
 - Slave is replaced by client
- 16. SPI section:
 - General improvement of the documentation
 - Updated terminology:
 - Master is replaced by host
 - Slave is replaced by client
- 17. TWI section:
 - Improved description for the Client Initialization section
 - Improved description for register bit fields:
 - The SDASETUP bit field from the CTRLA register
 - The INPUTLVL, FMPEN and SDAHOLD bit fields from the DUALCTRL register
 - The FLUSH bit field from the MCTRLB register
 - The BUSSTATE bit field from the MSTATUS register – The SCMD bit field from the SCTRLB register
- 18. CCL section:
 - Updated the Truth Table Output Value Selection figure
 - Updated the Linked LUT Input Selection figure
 - Improved description for the TRUTHn registers
 - Updated terminology:
 - Master is replaced by host
 - Slave is replaced by client
- 19. ADC section:
 - Added information on warm-up time in the Sleep Mode Operation section
 - Updated the Temperature Measurement section to include INITDLY and SAMPLEN configuration in the initialization steps
- 20. DAC section:
 - Removed conversion rate from the Feature section
 - Updated the DAC Block Diagram figure
 - Added the Signal Description section
 - Restructured the Operation section
 - Added the DAC Output section
 - The DAC as Source For Internal Peripheral section renamed as Unbuffered Output as Source For Internal Peripherals
 - The DAC Output on Pin section renamed as Buffered Output
- 20. UPDI section:
 - Renamed UPDICKDIV to UPDICKSEL
 - Updated the UPDI Clock Domains figure
 - Improved the Clocks section
 - Improved figures in the UPDI Instruction Set section

- Updated Reset value for the STATUSA.UPDIREV bit field
- Renamed the ASI_KEY_STATUS.CHIPERASE bit field to ASI_KEY_STATUS.CHER
- Renamed the ASI_CTRLA.UPDICKDIV bit field to ASI_CTRLA.UPDICKSEL
- Renamed the ASI_SYS_STATUS.UPDICKDIV bit field to ASI_SYS_STATUS.UPDICKSEL

21. Electrical characteristics section:

- Updated the Electrical Characteristics section
- Added the Characteristics Graphs section

Impacts to Data Sheet: See above details

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 July 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[AVR128DA28/32/48/64 Data Sheet](#)

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Affected Catalog Part Numbers (CPN)

AVR128DA28-E/SO
AVR128DA28-E/SP
AVR128DA28-E/SS
AVR128DA28-E/SSVAO
AVR128DA28-I/SO
AVR128DA28-I/SP
AVR128DA28-I/SS
AVR128DA28T-E/SO
AVR128DA28T-E/SS
AVR128DA28T-E/SSVAO
AVR128DA28T-I/SO
AVR128DA28T-I/SS
AVR128DA32-E/PT
AVR128DA32-E/PTVAO
AVR128DA32-E/RXB
AVR128DA32-E/RXBVAO
AVR128DA32-I/PT
AVR128DA32-I/RXB
AVR128DA32T-E/PT
AVR128DA32T-E/PTVAO
AVR128DA32T-E/RXB
AVR128DA32T-E/RXBVAO
AVR128DA32T-I/PT
AVR128DA32T-I/RXB
AVR128DA48-E/6LX
AVR128DA48-E/6LXVAO
AVR128DA48-E/PT
AVR128DA48-E/PTVAO
AVR128DA48-I/6LX
AVR128DA48-I/PT
AVR128DA48T-E/6LX
AVR128DA48T-E/6LXVAO
AVR128DA48T-E/PT
AVR128DA48T-E/PTVAO
AVR128DA48T-I/6LX
AVR128DA48T-I/PT
AVR128DA64-E/MR
AVR128DA64-E/MRVAO
AVR128DA64-E/PT
AVR128DA64-I/MR
AVR128DA64-I/PT
AVR128DA64T-E/MR
AVR128DA64T-E/MRVAO
AVR128DA64T-E/PT
AVR128DA64T-E/PTV01
AVR128DA64T-E/PTVAO

AVR128DA64T-I/MR

AVR128DA64T-I/PT