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June 2014

FQA160N08

N-Channel QFET® MOSFET 80 V, 160 A, 7 mΩ

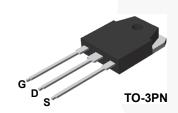
Description

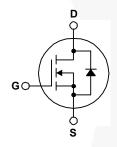
This N-Channel enhancement mode power MOSFET is • 160 A, 80 V, $R_{DS(on)}$ = 7 m Ω (Max.) @ V_{GS} = 10 V, produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state • Low Gate Charge (Typ. 220 nC) resistance, and to provide superior switching performance and • Low Crss (Typ. 530 pF) high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor • 100% Avalanche Tested control, and variable switching power applications.

Features

- $I_D = 80 A$

- 175°C Maximum Junction Temperature Rating





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQA160N08	Unit
V_{DSS}	Drain-Source Voltage		80	V
I _D	Drain Current - Continuous (T _C = 25°C)		160	Α
	- Continuous (T _C = 100°C)		113	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	640	Α
V _{GSS}	Gate-Source Voltage		± 25	V
E _{AS}	Single Pulsed Avalanche Energy	(Note 2)	1600	mJ
I _{AR}	Avalanche Current	(Note 1)	160	Α
E _{AR}	Repetitive Avalanche Energy		37.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.5	V/ns
P_D	Power Dissipation (T _C = 25°C)		375	W
	- Derate above 25°C		2.5	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T _L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds.		300	°C

Thermal Characteristics

Symbol	Parameter	FQA160N08	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.4	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA160N08	FQA160N08	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Uni
Off Cha	aracteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$				V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.08		V/°C
I _{DSS}	Zara Cata Valtana Dunin Courset	V _{DS} = 80 V, V _{GS} = 0 V		-	1	μΑ
	Zero Gate Voltage Drain Current	V _{DS} = 64 V, T _C = 150°C		-	10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 25 V, V _{DS} = 0 V			100	nA
$I_{\rm GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -25 \text{ V}, V_{DS} = 0 \text{ V}$		-	-100	nA
On Cha	aracteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 80 A		0.0056	0.007	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 30 V, I _D = 80 A		92		S
Dynam	ic Characteristics				•	
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,		6100	7900	pF
C _{oss}	Output Capacitance	f = 1.0 MHz		2400	3100	pF
C _{rss}	Reverse Transfer Capacitance			530	690	pF
Switchi	ing Characteristics					
t _{d(on)}	Turn-On Delay Time	V - 40 V I - 400 A		85	180	ns
t _r	Turn-On Rise Time	$V_{DD} = 40 \text{ V}, I_{D} = 160 \text{ A},$ $R_{G} = 25 \Omega$		970	2000	ns
t _{d(off)}	Turn-Off Delay Time	(Note4)		260	530	ns
t _f	Turn-Off Fall Time			410	830	ns
Qg	Total Gate Charge	V _{DS} = 64 V, I _D = 160 A,		225	290	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		43		nC
Q _{gd}	Gate-Drain Charge	(Note4)		120		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current (Note 5)				160	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	Forward Current			640	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 160 A			1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 160 A,		125		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs		510		nC

- Notes:
 1. Repetitive rating : pulse-width limited by maximum junction temperature.
 2. L = 0.115 mH, I_{AS} = 140 A, V_{DD} = 25 V, R_{G} = 25 Ω , starting T_{J} = 25°C.
 3. I_{SD} = 140 A, di/dt \leq 300 A/ μ s, V_{DD} \leq BV $_{DSS}$ starting T_{J} = 25°C.
 4. Essentially independent of operating temperature.
 5. Continuous drain current calculated by maximum junction temperature : limited by package.

Typical Characteristics

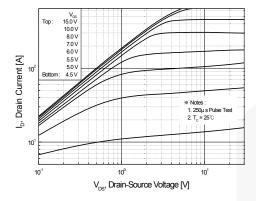


Figure 1. On-Region Characteristics

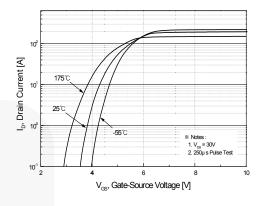


Figure 2. Transfer Characteristics

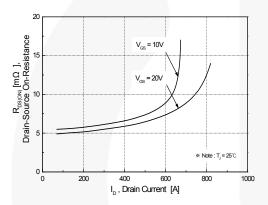


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

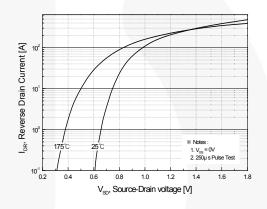


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

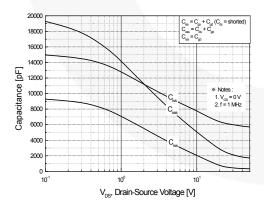


Figure 5. Capacitance Characteristics

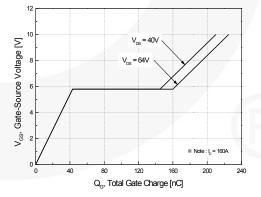
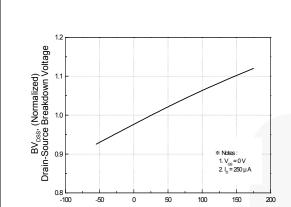


Figure 6. Gate Charge Characteristics

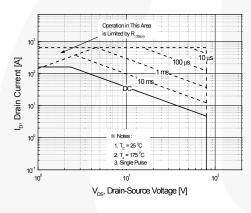


Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

T,, Junction Temperature [°C]

Figure 8. On-Resistance Variation vs. Temperature



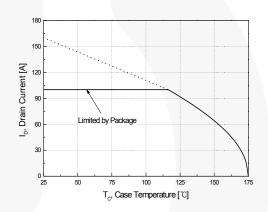


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

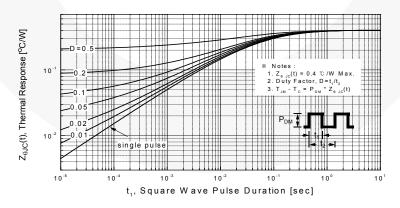


Figure 11. Transient Thermal Response Curve

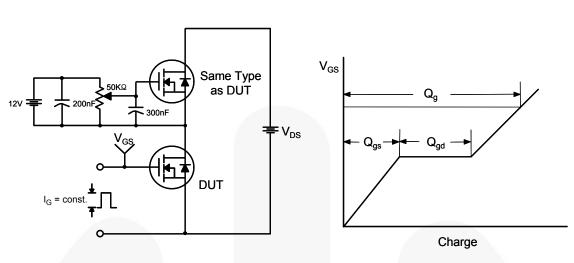


Figure 12. Gate Charge Test Circuit & Waveform

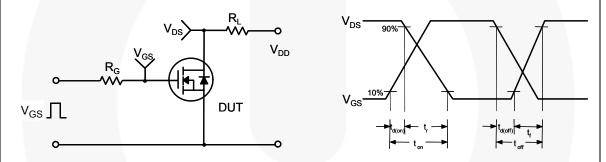


Figure 13. Resistive Switching Test Circuit & Waveforms

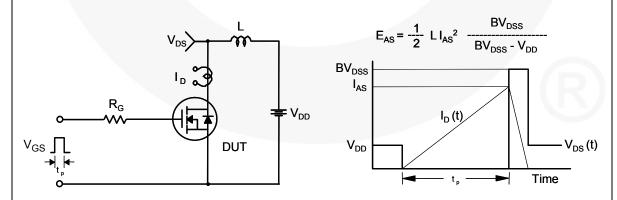
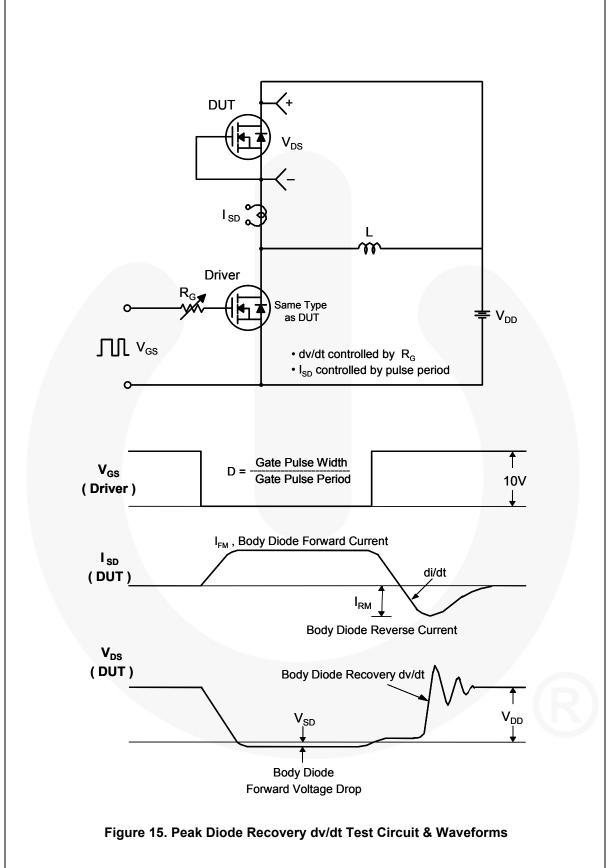
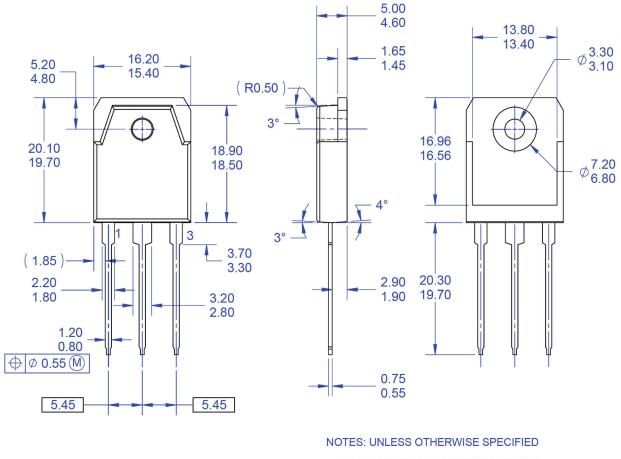
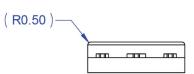


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions





- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.

 E) DRAWING FILE NAME: TO3PN03AREV1.

 F) FAIRCHILD SEMICONDUCTOR.

Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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