HMC253ALC4

GaAs MIMIC SP8T NON-REFLECTIVE SWITCH, DC - 3.5 GHz

Typical Applications

The HMC253ALC4 is ideal for:

- Basestations & Repeaters
- WiMAX/WiBro & Fixed Wireless
- Cellular/3G Infrastructure
- CATV/DBS
- Military & Hi-Rel

Features

Ceramic, RoHS Compliant 4x4 mm SMT Package

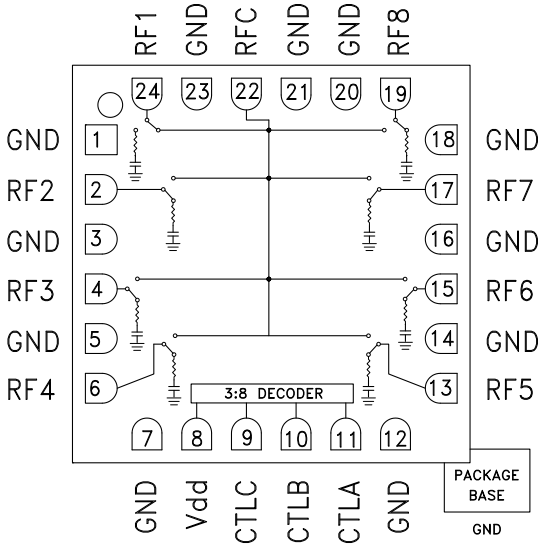
Non-Reflective Topology

Low Insertion Loss: 1.6 dB

Single Positive Supply: Vdd = +5V

Integrated 3:8 TTL/CMOS Decoder: 0/+3V

Functional Diagram



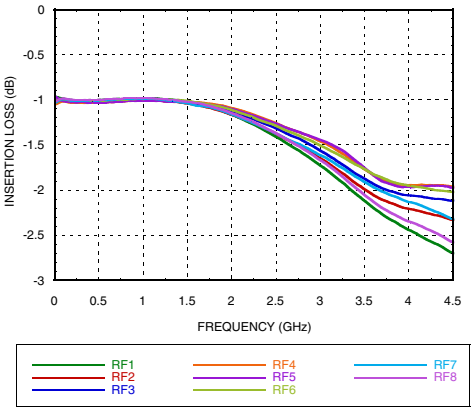
General Description

The HMC253ALC4 is a non-reflective SP8T switch in a leadless RoHS compliant 4x4 mm ceramic SMT package featuring wideband operation from DC to 3.5 GHz. The switch offers a single positive bias and true TTL/CMOS compatibility enabling it to operate with 0/+3V control and a +5V supply. A 3:8 decoder is integrated on the switch requiring only 3 control lines and a positive bias to select each path. The HMC253ALC4 SP8T will replace multiple configurations of SP4T and SPDT MMIC switches.

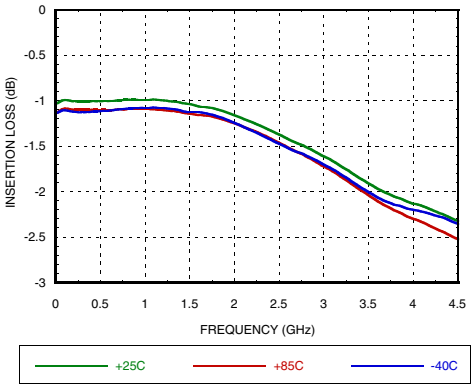
Electrical Specifications, T_A = +25° C, For TTL Control and Vdd = +5V in a 50 Ohm system

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 2.0 GHz DC - 3.0 GHz DC - 3.5 GHz		1.1 1.6 1.9	1.5 2.0 2.4	dB dB dB
Isolation	DC - 2.0 GHz DC - 3.0 GHz DC - 3.5 GHz	38 34 30	43 39 35		dB dB dB
Return Loss "On State"	0.3 - 3.0 GHz 0.3 - 3.5 GHz		13 10		dB dB
Return Loss (RF1-8) "Off State"	0.3 - 3.5 GHz 0.5 - 3.5 GHz		10 14		dB dB
Input Power for 1 dB Compression	0.5 - 3.5 GHz	20	24		dBm
Input Third Order Intercept (Two-Tone Input Power = +10 dBm Each Tone)	0.5 - 3.5 GHz	40	43		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	0.3 - 3.5 GHz		 30 100		 ns ns

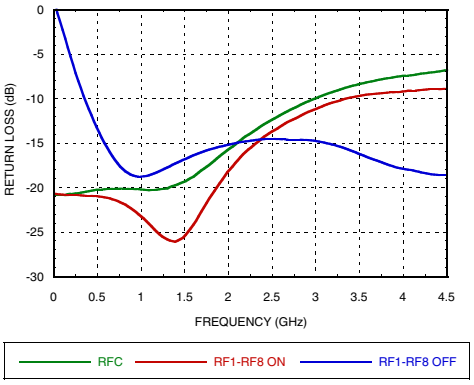
Insertion Loss



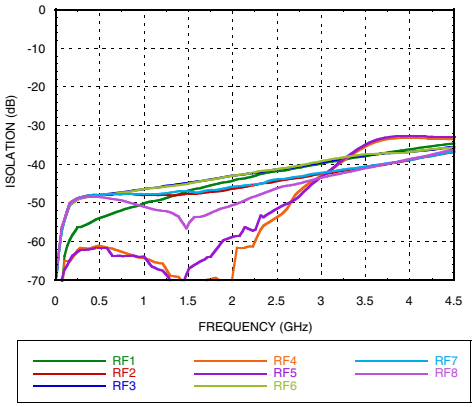
Insertion Loss vs. Temperature



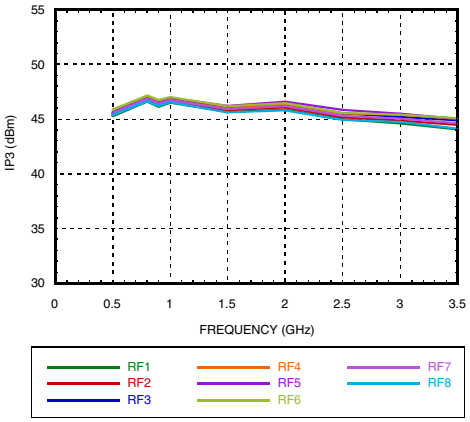
Return Loss



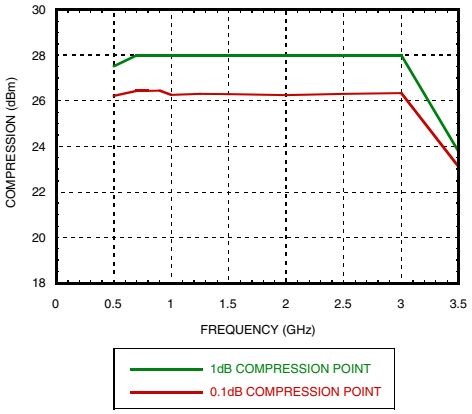
Isolation



Input IP3



Input Compression



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Bias Voltage & Current

Vdd Range = +5 Vdc ± 10%		
Vdd (Vdc)	Idd (Typ.) (mA)	Idd (Max.) (mA)
+5	4.5	7.5

TTL/CMOS Control Voltages

State	Bias Condition
Low	0 to +0.8 Vdc @ <1 µA Typ.
High	+2.0 to +5 Vdc @ 60 µA Typ.

Truth Table

Control Input			Signal Path State
A	B	C	RFCOM to:
Low	Low	Low	RF1
High	Low	Low	RF2
Low	High	Low	RF3
High	High	Low	RF4
Low	Low	High	RF5
High	Low	High	RF6
Low	High	High	RF7
High	High	High	RF8

NOTE:
DC Blocking capacitors are required at ports RFC and RF1, 2, 3, 4, 5, 6, 7, 8.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Absolute Maximum Ratings

Bias Voltage Range (Port Vdd)	+7.0 Vdc
Control Voltage Range (A, B, C)	-0.5V to Vdd +1Vdc
Channel Temperature	150 °C
Thermal Resistance (channel to package ground paddle) Through Path Termination Path	 183 °C/W 274 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
Maximum Input Power (Vdd = +5V) Through Path Terminated Path	 +20 dBm (0.05 - 0.5 GHz) +25 dBm (0.5 - 3.5 GHz) +20 dBm (0.05 - 0.5 GHz) +23.5 dBm (0.5 - 3.5 GHz)
ESD Sensitivity (HBM)	Class 1A

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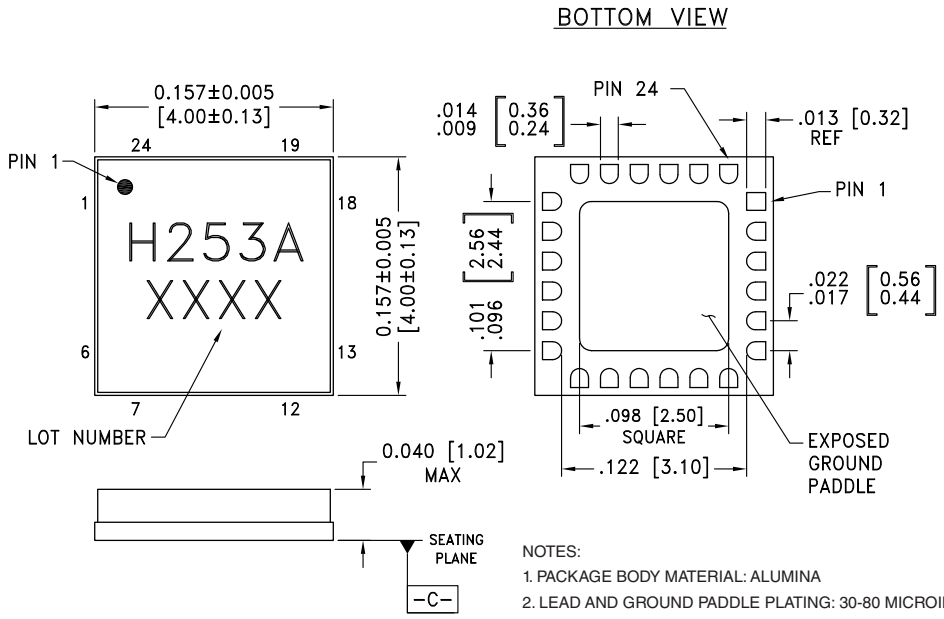
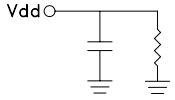
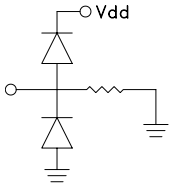
Outline Drawing



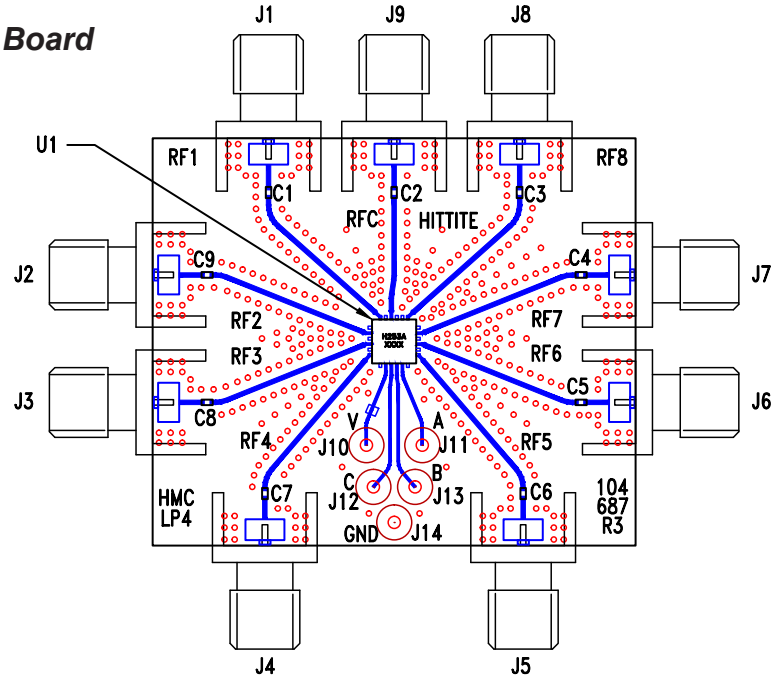
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5, 7, 12, 14, 16, 18, 20, 21, 23	GND	Package bottom has exposed metal paddle that must also be connected to RF ground.	
2, 4, 6, 13, 15, 17, 19, 22, 24	RF1 - RF8 & RFC	This pin is DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
8	Vdd	Supply Voltage +5 Vdc ±10%	
9	CTLC	See truth table and control voltage table.	
10	CTLB		
11	CTLA		

Evaluation Circuit Board



List of Materials for Evaluation PCB EV1HMC253ALC4 [1]

Item	Description
J1 - J9	PCB Mount SMA Connector
J10 - J14	DC Pin
C1 - C9	100 pF Capacitor, 0402 Pkg.
U1	HMC253ALC4 SP8T Switch
PCB [2]	104687 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF ports should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown above. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.