PCN Number:	20190703002	PCN Date:	Aug. 8, 2019
Title:	Datasheet for ADS54J60		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

ADS54J60

SBAS706D – APRIL 2015 – REVISED APRIL 2019

Changes from Revision C (January 2017) to Revision D **Page**

- Changed *FFT for 170-MHz Input Signal* figure 1
- Changed the description of the CLKINM, CLKINP, SYSREFM, SYSREFP, and PDN pins in *Pin Functions* table 6
- Changed typical values across parameters in *AC Characteristics* table 9
- Changed value of A_{IN} from *–1 dBFS* to *–3 dBFS* in *470 MHz* test condition across all parameters in *AC Characteristics* table 9
- Added ENOB parameter to *AC Characteristics* table 11
- Changed the first footnote in *Timing Characteristics* table 13
- Changed the typical value of *FOVR latency* from *18 + 4 ns* to *18* in *Timing Characteristics* table 13
- Changed parameter name from t_{PD} to t_{PDI} in *Timing Characteristics* table 13
- Changed *FFT for 170-MHz Input Signal* figure 15
- Changed *FFT for 470-MHz Input Signal at –3 dBFS* figure, title, and conditions 16
- Changed conditions of *FFT for 720-MHz Input Signal at –6 dBFS* figure 16
- Changed *Spurious-Free Dynamic Range vs Input Frequency* figure 17
- Changed *DDC Block* figure 27
- Deleted register address 53 from *Register Address for Power-Down Modes* table 33
- Added last sentence to Step 4 in *Serial Register Readout: Analog Bank* section 36
- Added last sentence to Step 4 in *Serial Register Readout: JESD Bank* section 37
- Added *SDOUT Timing Diagram* figure 38
- Deleted unrelated patterns in in *JESD204B Test Patterns* section 40
- Changed *Serial Interface Registers* figure 45
- Added register addresses 1h and 2h and their descriptions to *GENERAL REGISTERS* in *Register Map* section 46
- Changed the name of *MASTER PAGE (80h)* to *MASTER PAGE (ANALOG BANK PAGE SEL= 80h* in *Register Map* table 46
- Changed register *53h* and *54h*, and their descriptions to MASTER PAGE (ANALOG BANK PAGE SEL = 80h) in

Register Map section 46
- Changed the name of *ADC PAGE (0Fh)* to *ADC PAGE (ANALOG BANK PAGE SEL= 0Fh)* in *Register Map* table 46
- Changed the name of *MAIN DIGITAL PAGE (6800h)* to *MAIN DIGITAL PAGE (JESD BANK PAGE SEL=6800h)* in *Register Map* table 46
- Changed bit 5, register 4E of *MAIN DIGITAL PAGE (JESD BANK PAGE SEL = 6800h)* from *0* to *IMPROVE IL PERF* 46
- Changed the name of *JESD DIGITAL PAGE (6900h)* to *JESD DIGITAL PAGE (JESD BANK PAGE SEL=6900h)* in *Register Map* table 47
- Changed the name of *JESD ANALOG PAGE (6A00h)* to *JESD ANALOG PAGE (JESD BANK PAGE SEL=6A00h)* in *Register Map* table 47
- Changed bit 1, register 12 of *JESD ANALOG PAGE (6A00h)* from 0 to *ALWAYS WRITE 1* 47
- Changed bits 5 and 3, register 17 of *JESD ANALOG PAGE (JESD BANK PAGE SEL = 6A00h)* from *0* to *LANE PDN 1* and from *0* to *LANE PDN 0* respectively 47
- Added *OFFSET READ Page* and *OFFSET LOAD Page* registers to *Register Map* table 47
- Added *ADS54J60 Access Type Codes* table, deleted legends from *Register Descriptions* section 49
- Added register 1h and 2h to *Register Descriptions* section 50
- Changed description of *Registers 3h and 4h (address = 3h and 4h)* in *General Registers Page* 51
- Changed description of bit 0 in *Register 4Fh (address = 4Fh), Master Page (080h)* 55
- Changed the description of registers 53h and 54h 56
- Changed *9.5 dB* to *12 dB* in description of bits 6-0 in Register 44h (address = 44h), Main Digital Page (6800h) 59
- Changed bit 5 from *0* the *IMPROVE IL PERF* and changed *Register 4Eh Field Descriptions* table in *Register 4Eh (address = 4Eh), Main Digital Page (6800h)* 61
- Changed bit 1 from 0 to ALWAYS WRITE 1 in Register 12h (address = 12h), JESD Analog Page (6A00h) 68
- Changed bit 1 from *ALWAYS WRITE 1* to *0* in register 15h bit register 69
- Added *x (where x = 0, 2, or 3)* to bits 7-2 in *Register 13h-15h Field Descriptions* table of *Registers 13h-15h (address = 13h-15h), JESD Analog Page (6A00h)* 69
- Changed bit 6 from *W* to *R/W*, bit 5 from *0* to *LANE PDN 1* and from *W* to *R/W*, and changed bit 3 from *0* to *LANE PDN 0* and from *W* to *R/W* in *Register 17h* bit register table of *Register 17h (address = 17h), JESD Analog Page (6A00h)* 70
- Changed bits 5-0 of *Register 17h Field Descriptions* table in *Register 17h (address = 17h), JESD Analog Page (6A00h)* 70
- Added *Offset Read Page Register* and *Offset Load Page Register* sections to *Register Descriptions* section 72
- Added *DC Offset Correction Block in the ADS54J60* section 78
- Changed ±512 codes to ±1024 codes in *DC Offset Correction Block in the ADS54J60* section 78
- Added *Idle Channel Histogram* section 82
- Added transformer TC1-1-13M+ to *Transformer-Coupled Circuits* section 84
- Added note to *Layout Guidelines* section 87

The datasheet number will be changing.

Device Family	Change From:	Change To:
ADS54J60	SBAS706C	SBAS706D

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/ADS54J60

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

ADS54J60IRMP	ADS54J60IRMPT		

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
WW PCN Team	PCN_ww_admin_team@list.ti.com

IMPORTANT NOTICE AND DISCLAIMER