Features

- Programmable μ-Law/A-Law codec and filters
- Programmable CCITT (G.711)/sign-magnitude coding
- Programmable transmit, receive and side-tone gains
- DSP-based:
  - Speakerphone switching algorithm
  - DTMF and single tone generator
  - Tone Ringer
- Differential interface to telephony transducers
- Differential audio paths
- Single 5 volt power supply

Applications

- Fully featured digital telephone sets
- Cellular phone sets
- Local area communications stations

February 2005

Ordering Information

MT9094AP	44 Pin PLCC	Tubes
MT9094APR	44 Pin PLCC	Tape & Reel
MT9094AP1	44 Pin PLCC*	Tubes
MT9094APR1	44 Pin PLCC*	Tape & Reel

*Pb Free Matte

-40°C to +85°C

Description

The MT9094 DPhone-II is a fully featured integrated digital telephone circuit. Voice band signals are converted to digital PCM and vice versa by a switched capacitor Filter/Codec. The Filter/Codec uses an ingenious differential architecture to achieve low noise operation over a wide dynamic range with a single 5 V supply. A Digital Signal Processor provides handsfree speaker-phone operation. The DSP is also used to generate tones (DTMF, Ringer and Call Progress) and control audio gains. Internal registers are accessed through a serial microport conforming to INTEL MCS-51™ specifications. The device is fabricated in Zarlink's low power ISO²-CMOS technology.

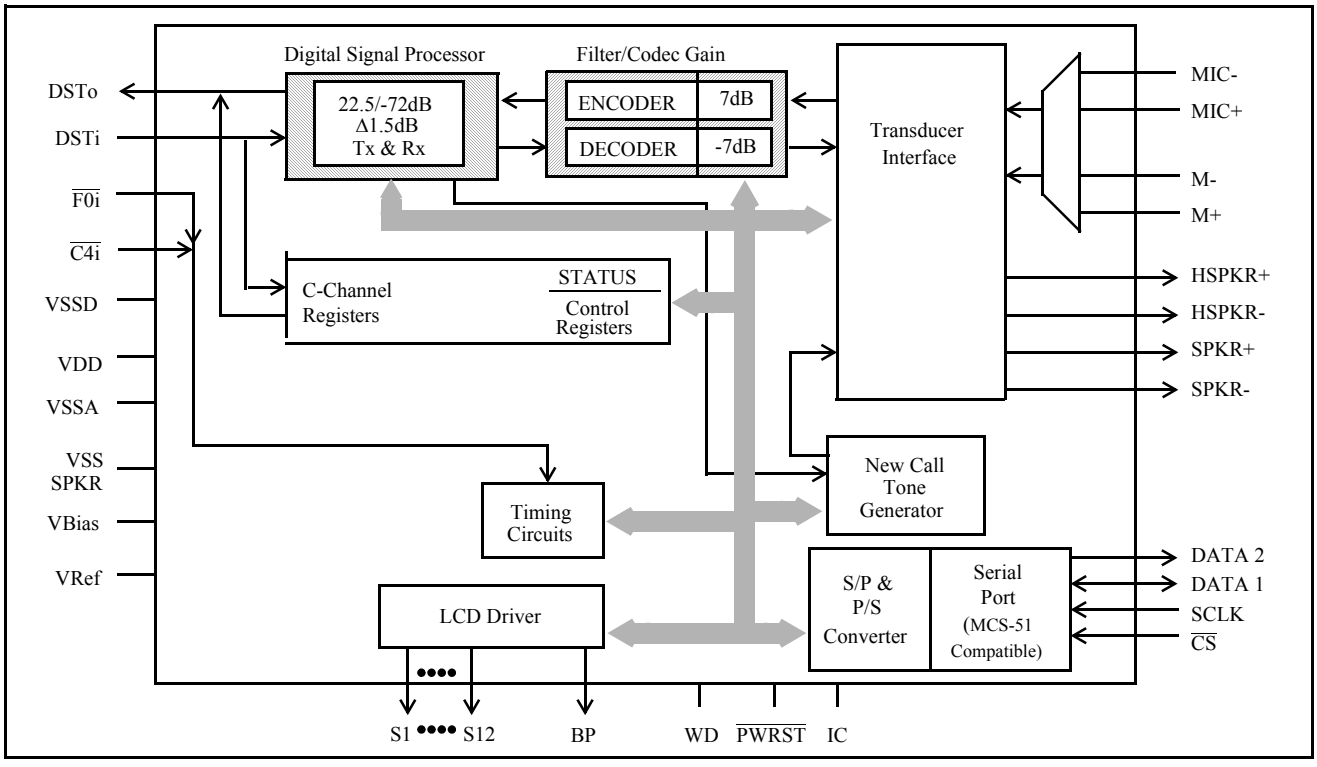

Figure 1 - Functional Block Diagram

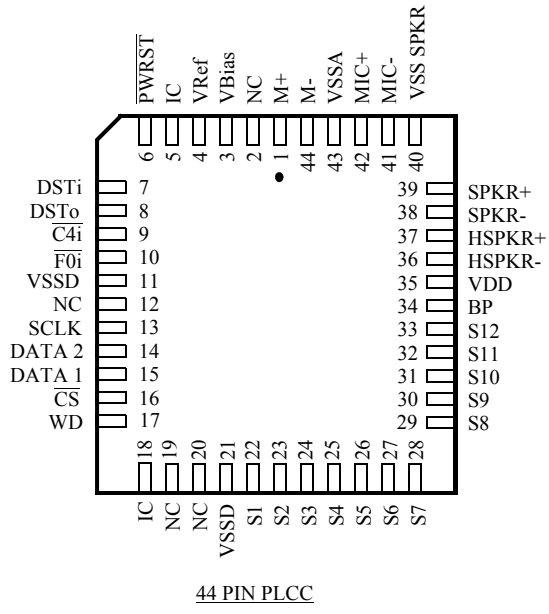

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	M+	**Non-Inverting Microphone (Input).** Non-inverting input to microphone amplifier from the handset microphone.
2	NC	**No Connect.** No internal connection to this pin.
3	V_{Bias}	**Bias Voltage (Output).** (V_{DD}/2) volts is available at this pin for biasing external amplifiers. Connect 0.1 µF capacitor to V_{SSA}.
4	V_{Ref}	**Reference voltage for codec (Output).** Nominally [(V_{DD}/2)-1.5] volts. Used internally. Connect 0.1 µF capacitor to V_{SSA}.
5	IC	**Internal Connection.** Tie externally to V_{SS} for normal operation.
6	$\overline{PWRST}$	**Power-up Reset (Input).** CMOS compatible input with Schmitt Trigger (active low).
7	DSTi	**ST-BUS Serial Stream (Input).** 2048 kbit/s input stream composed of 32 eight bit channels; the first four of which are used by the MT9094. Input level is TTL compatible.
8	DSTo	**ST-BUS Serial Stream (Output).** 2048 kbit/s output stream composed of 32 eight bit channels. The MT9094 sources digital signals during the appropriate channel, time coincident with the channels used for DSTi.
9	$\overline{C4i}$	**4096 kHz Clock (Input).** CMOS level compatible.
10	$\overline{F0i}$	**Frame Pulse (Input).** CMOS level compatible. This input is the frame synchronization pulse for the 2048 kbit/s ST-BUS stream.
11	V_{SSD}	**Digital Ground.** Nominally 0 volts.
12	NC	**No Connect.** No internal connection to this pin.

Pin Description (continued)

Pin #	Name	Description
13	SCLK	**Serial Port Synchronous Clock (Input).** Data clock for MCS-51 compatible microport. TTL level compatible.
14	DATA 2	**Serial Data Transmit.** In an alternate mode of operation, this pin is used for data transmit from MT9094. In the default mode, serial data transmit and receive are performed on the DATA 1 pin and DATA 2 is tri-stated.
15	DATA 1	**Bidirectional Serial Data.** Port for microprocessor serial data transfer compatible with MCS-51 standard (default mode). In an alternate mode of operation, this pin becomes the data receive pin only and data transmit is performed on the DATA 2 pin. Input level TTL compatible.
16	$\overline{CS}$	**Chip Select (Input).** This input signal is used to select the device for microport data transfers. Active low. (TTL level compatible.)
17	WD	**Watchdog (Output).** Watchdog timer output. Active high.
18	IC	**Internal Connection.** Tie externally to V_{SS} for normal operation.
19, 20	NC	**No Connection.** No internal connection to these pins.
21	V_{SSD}	**Digital Ground.** Nominally 0 volts.
22-33	S1-S12	**Segment Drivers (Output).** 12 independently controlled, two level, LCD segment drivers. An in-phase signal, with respect to the BP pin, produces a non-energized LCD segment. An out-of-phase signal, with respect to the BP pin, energizes its respective LCD segment.
34	BP	**Backplane Drive (Output).** A two-level output voltage for biasing an LCD backplane.
35	V_{DD}	**Positive Power Supply (Input).** Nominally 5 volts.
36	HSPKR-	**Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
37	HSPKR+	**Non-Inverting Handset Speaker (Output).** Output to the handset speaker (balanced).
38	SPKR-	**Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
39	SPKR+	**Non-Inverting Speaker (Output).** Output to the speakerphone speaker (balanced).
40	V_{SS} SPKR	**Power Supply Rail for Analog Output Drivers.** Nominally 0 Volts.
41	MIC-	**Inverting Handsfree Microphone (Input).** Handsfree microphone amplifier inverting input pin.
42	MIC+	**Non-inverting Handsfree Microphone (Input).** Handsfree microphone amplifier non-inverting input pin.
43	V_{SSA}	**Analog Ground.** Nominally 0 V.
44	M-	**Inverting Microphone (Input).** Inverting input to microphone amplifier from the handset microphone.

NOTES:
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Overview

The Functional Block Diagram of Figure 1 depicts the main operations performed within the DPhone-II. Each of these functional blocks will be described in the sections to follow. This overview will describe some of the end-user features which may be implemented as a direct result of the level of integration found within the DPhone-II.

The main feature required of a digital telephone is to convert the digital Pulse Code Modulated (PCM) information, being received by the telephone set, into an analog electrical signal. This signal is then applied to an appropriate audio transducer such that the information is finally converted into intelligible acoustic energy. The same is true of the reverse direction where acoustic energy is converted first into an electrical analog and then digitized (into PCM) before being transmitted from the set. Along the way if the signals can be manipulated, either in the analog or the digital domains, other features such as gain control, signal generation and filtering may be added. More complex processing of the digital signal is also possible and is limited only be the processing power available. One example of this processing power may be the inclusion of a complex handsfree switching algorithm. Finally, most electro-acoustic transducers (loudspeakers) require a large amount of power to develop an effective acoustic signal. The inclusion of audio amplifiers to provide this power is required.

The DPhone-II features Digital Signal Processing (DSP) of the voice encoded PCM, complete Analog/Digital and Digital/Analog conversion of audio signals (Filter/CODEC) and an analog interface to the external world of electro-acoustic devices (Transducer Interface). These three functional blocks combine to provide a standard full-duplex telephone conversation utilizing a common handset. Selecting transducers for handsfree operation, as well as allowing the DSP to perform its handsfree switching algorithm, is all that is required to convert the full-duplex handset conversation into a half-duplex speakerphone conversation. In each of these modes, full programmability of the receive path and side-tone gains is available to set comfortable listening levels for the user as well as transmit path gain control for setting nominal transmit levels into the network.

The ability to generate tones locally provides the designer with a familiar method of feedback to the telephone user as they proceed to set-up, and ultimately, dismantle a telephone conversation. Also, as the network slowly evolves from the dial pulse/DTMF methods to the D-Channel protocols it is essential that the older methods be available for backward compatibility. As an example; once a call has been established, say from your office to your home, using the D-Channel signalling protocol it may be necessary to use in-band DTMF signalling to manipulate your personal answering machine in order to retrieve messages. Thus the locally generated tones must be of network quality and not just a reasonable facsimile. The DPhone-II DSP can generate the required tone pairs as well as single tones to accommodate any in-band signalling requirement.

Each of the programmable parameters within the functional blocks is accessed through a serial microcontroller port compatible with Intel MCS-51 specifications.

Functional Description

In this section, each functional block within the DPhone-II is described along with all of the associated control/status bits. Each time a control/ status bit(s) is described it is followed by the address register where it will be found. The reader is referred to the section titled ‘Register Summary' for a complete listing of all address map registers, the control/status bits associated with each register and a definition of the function of each control/status bit. The Register Summary is useful for future reference of control/status bits without the need to locate them within the text of the functional descriptions.

Filter-CODEC

The Filter/CODEC block implements conversion of the analog 3.3kHz speech signals to/from the digital domain compatible with 64 kb/s PCM B-Channels. Selection of companding curves and digital code assignment are register programmable. These are CCITT G.711 A-law or μ-Law, with true-sign/ Alternate Digit Inversion or true-sign/Inverted Magnitude coding, respectively. Optionally, sign- magnitude coding may also be selected for proprietary applications.

The Filter/CODEC block also implements transmit and receive audio path gains in the analog domain. These gains are in addition to the digital gain pad provided in the DSP section and provide an overall path gain resolution of 0.5 dB. A programmable gain, voice side-tone path is also included to provide proportional transmit speech feedback to the handset receiver so that a dead sounding handset is not encountered. Figure 3 depicts the nominal half-channel and side-tone gains for the DPhone-II.

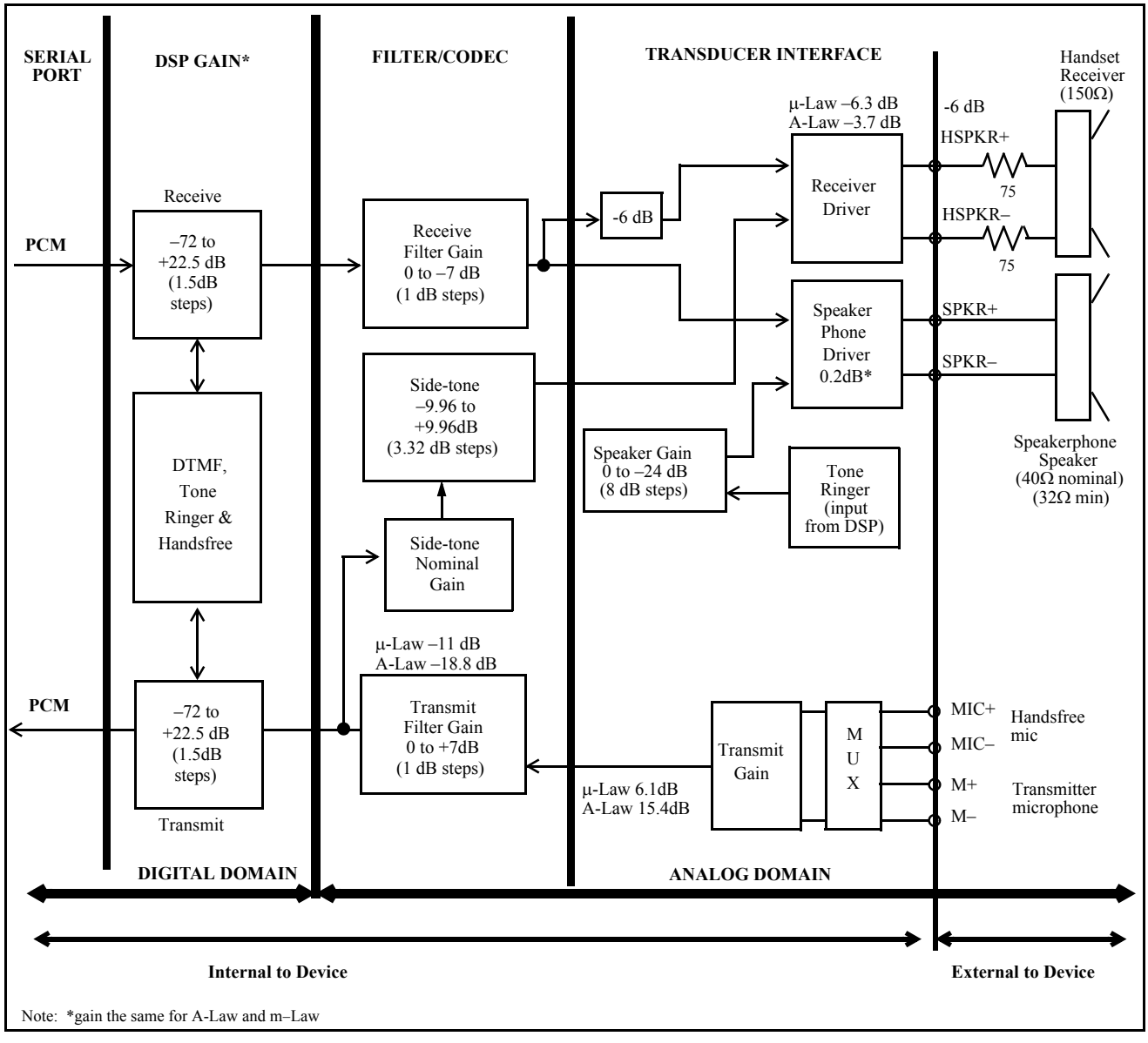


Figure 3 - Audio Gain Partitioning

On $\overline{\text{PWRST}}$ (pin 6) the Filter/CODEC defaults such that the side-tone path, dial tone filter and 400 Hz transmit filter are off, all programmable gains are set to 0 dB and μ-Law companding is selected. Further, the Filter/CODEC is powered down due to the PuFC bit (Transducer Control Register, address 0Eh) being reset. This bit must be set high to enable the Filter/CODEC.

The internal architecture is fully differential to provide the best possible noise rejection as well as to allow a wide dynamic range from a single 5 volt supply design. This fully differential architecture is continued into the Transducer Interface section to provide full chip realization of these capabilities.

A reference voltage (V_{Ref}), for the conversion requirements of the CODER section, and a bias voltage (V_{Bias}), for biasing the internal analog sections, are both generated on-chip. V_{Bias} is also brought to an external pin so that it may be used for biasing any external gain plan setting amplifiers. A 0.1 μF capacitor must be connected from V_{Bias} to analog ground at all times. Likewise, although V_{Ref} may only be used internally, a 0.1 μF capacitor from the V_{Ref}

pin to ground is required at all times. It is suggested that the analog ground reference point for these two capacitors be physically the same point. To facilitate this the V_{Ref} and V_{Bias} pins are situated on adjacent pins.

The transmit filter is designed to meet CCITT G.714 specifications. The nominal gain for this filter path is 0 dB (gain control = 0 dB). An anti-aliasing filter is included. This is a second order lowpass implementation with a corner frequency at 25 kHz. Attenuation is better than 32 dB at 256 kHz and less than 0.01 dB within the passband.

An optional 400 Hz high-pass function may be included into the transmit path by enabling the Tfhp bit in the Transducer Control Register (address 0Eh). This option allows the reduction of transmitted background noise such as motor and fan noise.

The receive filter is designed to meet CCITT G.714 specifications. The nominal gain for this filter path is 0 dB (gain control = 0 dB). Filter response is peaked to compensate for the sinx/x attenuation caused by the 8 kHz sampling rate.

The Rx filter function can be altered by enabling the DIAL EN control bit in the Transducer Control Register (address 0Eh). This causes another lowpass function to be added, with a 3 dB point at 1000 Hz. This function is intended to improve the sound quality of digitally generated dial tone received as PCM.

Transmit sidetone is derived from the Tx filter and is subject to the gain control of the Tx filter section. Sidetone is summed into the receive path after the Rx filter gain control section so that Rx gain adjustment will not affect sidetone levels. The side-tone path may be enabled/disabled with the SIDE EN bit located in the Transducer Control Register (address 0Eh). See also STG_0-STG_2 (address 0Bh).

Transmit and receive filter gains are controlled by the $TxFG_0$-$TxFG_2$ and $RxFG_0$-$RxFG_2$ control bits respectively. These are located in the FCODEC Gain Control Register 1 (address 0Ah). Transmit filter gain is adjustable from 0 dB to +7 dB and receive filter gain from 0 dB to -7 dB, both in 1 dB increments.

Side-tone filter gain is controlled by the STG_0-STG_2 control bits located in the FCODEC Gain Control Register 2 (address 0Bh). Side-tone gain is adjustable from -9.96 dB to +9.96 dB in 3.32 dB increments.

Law selection for the Filter/CODEC is provided by the A/μ companding control bit while the coding scheme is controlled by the sign-mag/$\overline{\text{CCITT}}$ bit. Both of these reside in the General Control Register (address 0Fh).

Digital Signal Processor

The DSP block is located, functionally, between the serial ST-BUS port and the Filter/CODEC block. Its main purpose is to provide both a digital gain control and a half-duplex handsfree switching function. The DSP will also generate the digital patterns required to produce standard DTMF signalling tones as well as single tones and a tone ringer output. A programmable (ON/OFF) offset null routine may also be performed on the transmit PCM data stream. The DSP can generate a ringer tone to be applied to the speakerphone speaker during normal handset operation so that the existing call is not interrupted.

The main functional control of the DSP is through two hardware registers which are accessible at any time via the microport. These are the Receive Gain Control Register at address 1Dh and the DSP Control Register at address 1Eh. In addition, other functional control is accomplished via multiple RAM-based registers which are accessible only while the DSP is held in a reset state. This is accomplished with the $\overline{\text{DRESET}}$ bit of the DSP Control Register. Ram-based registers are used to store transmit gain levels (20h for transmit PCM and 21h for transmit DTMF levels), the coefficients for tone and ringer generation (addresses 23h and 24h), and tone ringer warble rates (address 26h). All undefined addresses below 20h are reserved for the temporary storage of interim variables calculated during the execution of the DSP algorithms. These undefined addresses should not be written to via the microprocessor port. The DSP can be programmed to execute the following micro-programs which are stored in instruction ROM, (see PS0 to PS2, DSP Control Register, address 1Eh). All program execution begins at the frame pulse boundary.

PS2	PS1	PS0	Micro-program
0	0	0	Power up reset program

0	0	1	Transmit and receive gain control program; with autonulling of the transmit PCM, if the AUTO bit is set (see address 1Dh)
0	1	0	DTMF generation plus transmit and receive gain control program (autonull available via the AUTO control bit)
0	1	1	Tone ringer plus transmit and receive gain control program (autonull available via the AUTO control bit)
1	0	0	handsfree switching program
1	0	1	
1	1	0	Last three selections reserved
1	1	1	

Note: For the DSP to function it must be selected to operate, in conjunction with the Filter/Codec, in one of the B-Channels. Therefore, one of the B-Channel enable bits must be set (see Timing Control, address 15h: bits CH_2EN and CH_3EN).

Power Up Reset Program

A hardware power-up reset (pin 6, $\overline{\text{PWRST}}$) will initialize the DSP hardware registers to the default values (all zeros) and will reset the DSP program counter. The DSP will then be disabled and the PCM streams will pass transparently through the DSP. The RAM-based registers are not reset by the $\overline{\text{PWRST}}$ pin but may be initialized to their default settings by programming the DSP to execute the power up reset program. None of the micro-programs actually require the execution of the power up reset program but it is useful for pre-setting the variables to a known condition. Note that the reset program requires one full frame (125μSec) for execution.

Gain Control Program

Gain control is performed on converted linear code for both the receive and the transmit PCM. Receive gain control is set via the hardware register at address 1Dh (see bits B0 - B5) and may be changed at any time. Gain in 1.5 dB increments is available within a range of +22.5 dB to -72 dB. Normal operation usually requires no more than a +20 to -20 dB range of control. However, the handsfree switching algorithm requires a large attenuation depth to maintain stability in worst case environments, hence the large (-72 dB) negative limit. Transmit gain control is divided into two RAM registers, one for setting the network level of transmit speech (address 20h) and the other for setting the transmit level of DTMF tones into the network (address 21h). Both registers provide gain control in 1.5 dB increments and are encoded in the same manner as the receive gain control register (see address 1Dh, bits B0 - B5). The power up reset program sets the default values such that the receive gain is set to -72.0 dB, the transmit audio gain is set to 0.0dB and the transmit DTMF gain is set to -3.0 dB (equivalent to a DTMF output level of -4 dBm0 into the network).

Optional Offset Nulling

Transmit PCM may contain residual offset in the form of a DC component. An offset of up to ±fifteen linear bits is acceptable with no degradation of the parameters defined in CCITT G.714. The DPhone-II filter/CODEC guarantees no more than ±ten linear bits of offset in the transmit PCM when the autonull routine is not enabled. By enabling autonulling (see AUTO in the Receive Gain Control Register, address 1Dh) offsets are reduced to within ±one bit of zero. Autonulling circuitry was essential in the first generations of Filter/Codecs to remove the large DC offsets found in the linear technology. Newer technology has made nulling circuitry optional as offered in the DPhone-II.

DTMF and Gain Control Program

The DTMF program generates a dual cosine wave pattern which may be routed into the receive path as comfort tones or into the transmit path as network signalling. In both cases, the digitally generated signal will undergo gain adjustment as programmed into the Receive Gain Control and the Transmit DTMF Gain Control registers. The composite signal output level in both directions is -4 dBm0 when the gain controls are set to 2Eh (-3.0 dB). Adjustments to these levels may be made by altering the settings of the gain control registers. Pre-twist of 2.0 dB is incorporated into the composite signal. The frequency of the low group tone is programmed by writing an 8-bit coefficient into Tone Coefficient Register 1 (address 23h), while the high group tone frequency uses the 8-bit coefficient programmed into Tone Coefficient Register 2 (address 24h). Both coefficients are determined by the following equation:

$$COEFF = 0.128 \times Frequency\ (in\ Hz)$$

where COEFF is a rounded off 8 bit binary integer

A single frequency tone may be generated instead of a dual tone by programming the coefficient at address 23h to a value of zero. In this case the frequency of the single output tone is governed by the coefficient stored at address 24h.

Frequency (Hz)	COEF	Actual Frequency	% Deviation
697	59h	695.3	-.20%
770	63h	773.4	+.40%
852	6Dh	851.6	-.05%
941	79h	945.3	+.46%
1209	9Bh	1210.9	+.20%
1336	ABh	1335.9	.00%
1477	BDh	1476.6	-.03%
1633	D1h	1632.8	-.01%

Table 1

DTMF Signal to distortion:
The sum of harmonic and noise power in the frequency band from 50 Hz to 3500 Hz is typically more than 30dB below the power in the tone pair. All individual harmonics are typically more than 40 dB below the level of the low group tone.

Table 1 gives the standard DTMF frequencies, the coefficient required to generate the closest frequency, the actual frequency generated and the percent deviation of the generated tone from the nominal.

Tone Ringer and Gain Control Program

A locally generated alerting (ringing) signal is used to prompt the user when an incoming call must be answered. The DSP uses the values programmed into Tone Coefficient Registers 1 and 2 (addresses 23h and 24h) to generate two different squarewave frequencies in PCM code. The amplitude of the squarewave frequencies is set to a mid level before being sent to the receive gain control block. From there the PCM passes through the decoder and receive filter, replacing the normal receive PCM data, on its way to the loudspeaker driver. Both coefficients are determined by the following equation:

$$COEFF = 8000/Frequency\ (Hz)$$

where COEFF is a rounded off 8 bit binary integer

The ringer program switches between these two frequencies at a rate defined by the 8-bit coefficient programmed into the Tone Ringer Warble Rate Register (address 26h). The warble rate is defined by the equation:

$$\textit{Tone duration (warble frequency in Hz)} = 500/COEFF$$

where 0 < COEFF < 256, a warble rate of 5-20 Hz is suggested.

An alternate method of generating ringer tones to the speakerphone speaker is available. With this method the normal receive speech path through the decoder and receive filter is uninterrupted to the handset, allowing an existing conversation to continue. The normal DSP and Filter/CODEC receive gain control is also retained by the speech path. When the OPT bit (DSP Control Register address 1Eh) is set high the DSP will generate the new call tone according to the coefficients programmed into registers 23h, 24h and 26h as before. In this mode the DSP output is no longer a PCM code but a toggling signal which is routed directly through the New Call Tone gain control section to the loudspeaker driver. Refer to the section titled 'New Call Tone'.

Handsfree Program

A half-duplex speakerphone program, fully contained on chip, provides high quality gain switching of the transmit and receive speech PCM to maintain loop stability under most network and local acoustic environments. Gain switching is performed in continuous 1.5 dB increments and operates in a complimentary fashion. That is, with the transmit path at maximum gain the receive path is fully attenuated and vice versa. This implies that there is a mid position where both transmit and receive paths are attenuated equally during transition. This is known as the idle state.

Of the 64 possible attenuator states, the algorithm may rest in only one of three stable states; full receive, full transmit and idle. The maximum gain values for full transmit and full receive are programmable through the microport at addresses 20h and 1Dh respectively, as is done for normal handset operation. This allows the user to set the maximum volumes to which the algorithm will adhere. The algorithm determines which path should maintain control of the loop based upon the relative levels of the transmit and receive audio signals after the detection and removal of background noise energy. If the algorithm determines that neither the transmit or the receive path has valid speech energy then the idle state will be sought. The present state of the algorithm plus the result of the Tx vs. Rx decision will determine which transition the algorithm will take toward its next stable state. The time durations required to move from one stable state to the next are parameters defined in CCITT Recommendation P.34 and are used by default by this algorithm (i.e., build-up time, hang-over time and switching time).

Quiet Code

The DSP can be made to send quiet code to the decoder and receive filter path by setting the RxMUTE bit high. Likewise, the DSP will send quiet code in the transmit (DSTo) path when the TxMUTE bit is high. Both of these control bits reside in the DSP Control Register at address 1Eh. When either of these bits are low, their respective paths function normally.

Transducer Interfaces

Four standard telephony transducer interfaces are provided by the DPhone-II. These are:

- The handset microphone inputs (transmitter), pins M+/M- and the speakerphone microphone inputs, pins MIC+/MIC-. The transmit path is muted/not-muted by the MIC EN control bit. Selection of which input pair is to be routed to the transmit filter amplifier is accomplished by the MIC/HNSTMIC control bit. Both of these reside in the Transducer Control Register (address 0Eh). The nominal transmit path gain may be adjusted to either 6.1 dB (suggested for μ-Law) or 15.4 dB (suggested for A-Law). Control of this gain is provided by the MICA/u control bit (General Control Register, address 0Fh). This gain adjustment is in addition to the programmable gain provided by the transmit filter and DSP.

- The handset speaker outputs (receiver), pins HSPKR+/HSPKR-. This internally compensated, fully differential output driver is capable of driving the load shown in Figure 4. This output is enabled/disabled by the HSSPKR EN bit residing in the Transducer Control Register (address 0Eh). The nominal handset receive path gain may be adjusted to either -12.3 dB (suggested for μ-Law) or - 9.7 dB (suggested for A-Law). Control of this gain is provided by the RxA/u control bit (General Control Register, address 0Fh). This gain adjustment is in addition to the programmable gain provided by the receive filter and DSP.
- The loudspeaker outputs, pins SPKR+/SPKR-. This internally compensated, fully differential output driver is capable of directly driving 6.5vpp into a 40 ohm load. This output is enabled/disabled by the SPKR EN bit residing in the Transducer Control Register (address 0Eh). The nominal gain for this amplifier is 0.2 dB.

C-Channel

Access to the internal control and status registers of Zarlink basic rate, layer 1, transceivers is through the ST-BUS Control Channel (C-Channel), since direct microport access is not usually provided, except in the case of the SNIC (MT8930). The DPhone-II provides asynchronous microport access to the ST-BUS C-Channel information on both DSTo and DSTi via a double-buffered read/write register (address 14h). Data written to this address is transmitted on the C-Channel every frame when enabled by CH_1EN (see ST-BUS/Timing Control).

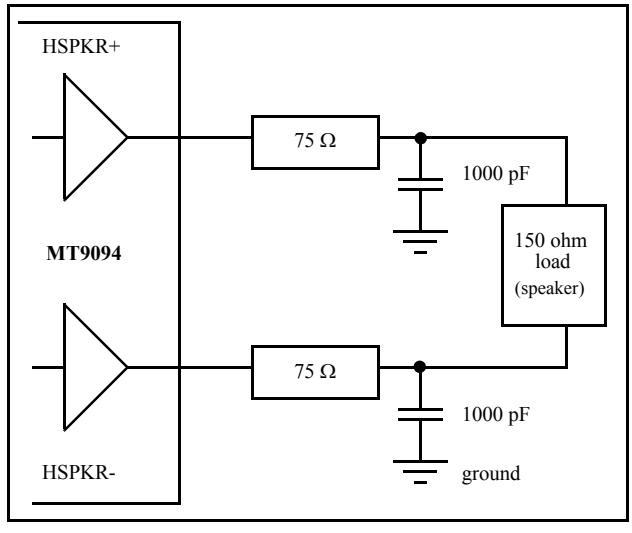


Figure 4 - Handset Speaker Driver

LCD

A twelve segment, non-multiplexed, LCD display controller is provided for easy implementation of various set status and call progress indicators. The twelve output pins (S_n) are used in conjunction with 12 segment control bits, located in LCD Segment Enable Registers 1&2 (addresses 12h and 13h), and the BackPlane output pin (BP) to control the on/off state of each segment individually.

The BP pin drives a continuous 62.5 Hz, 50% duty cycle squarewave output signal. An individual segment is controlled via the phase relationship of its segment driver output pin with respect to the backplane, or common, driver output. Each of the twelve Segment Enable bits corresponds to a segment output pin. The waveform at each segment pin is in-phase with the BP waveform when its control bit is set to logic zero (segment off) and is out-of-phase with the BP waveform when its control bit is set to a logic high (segment on). Refer to the LCD Driver Characteristics for pin loading information.

Microport

A serial microport, compatible with Intel MCS-51 (mode 0) specifications, provides access to all DPhone-II internal read and write registers. This microport consists of three pins; a half-duplex transmit/receive data pin (DATA1), a chip select pin ($\overline{CS}$) and a synchronous data clock pin (SCLK).

On power-up reset ($\overline{PWRST}$) or with a software reset (RST), the DATA1 pin becomes a bidirectional (transmit/receive) serial port while the DATA2 pin is internally disconnected and tri-stated.

All data transfers through the microport are two-byte transfers requiring the transmission of a Command/Address byte followed by the data byte written or read from the addressed register. $\overline{CS}$ must remain asserted for the duration of this two-byte transfer. As shown in Figure 5, the falling edge of $\overline{CS}$ indicates to the DPhone-II that a microport transfer is about to begin. The first 8 clock cycles of SCLK after the falling edge of $\overline{CS}$ are always used to receive the Command/Address byte from the microcontroller. The Command/Address byte contains information detailing whether the second byte transfer will be a read or a write operation and of what address. The next 8 clock cycles are used to transfer the data byte between the DPhone-II and the microcontroller. At the end of the two-byte transfer $\overline{CS}$ is brought high again to terminate the session. The rising edge of $\overline{CS}$ will tri-state the output driver of DATA1 which will remain tri-stated as long as $\overline{CS}$ is high.

Receive data is sampled and transmit data is made available on DATA1 concurrent with the falling edge of SCLK.

Lastly, provision is made to separate the transmit and receive data streams onto two individual pins. This control is given by the DATASEL pin in the General Control Register (address 0Fh). Setting DATASEL logic high will cause DATA1 to become the data receive pin and DATA2 to become the data transmit pin. Only the signal paths are altered by DATASEL; internal timing remains the same in both cases. Tri-stating on DATA2 follows $\overline{CS}$ as it does on DATA1 when DATASEL is logic low. Use of the DATASEL bit is intended to help in adapting Motorola (SPI) and National Semiconductor (Micro-wire) microcontrollers to the DPhone-II. Note that whereas Intel processor serial ports transmit data LSB first other processor serial ports, including Motorola, transmit data MSB first. It is the responsibility of the microcontroller to provide LSB first data to the DPhone-II.

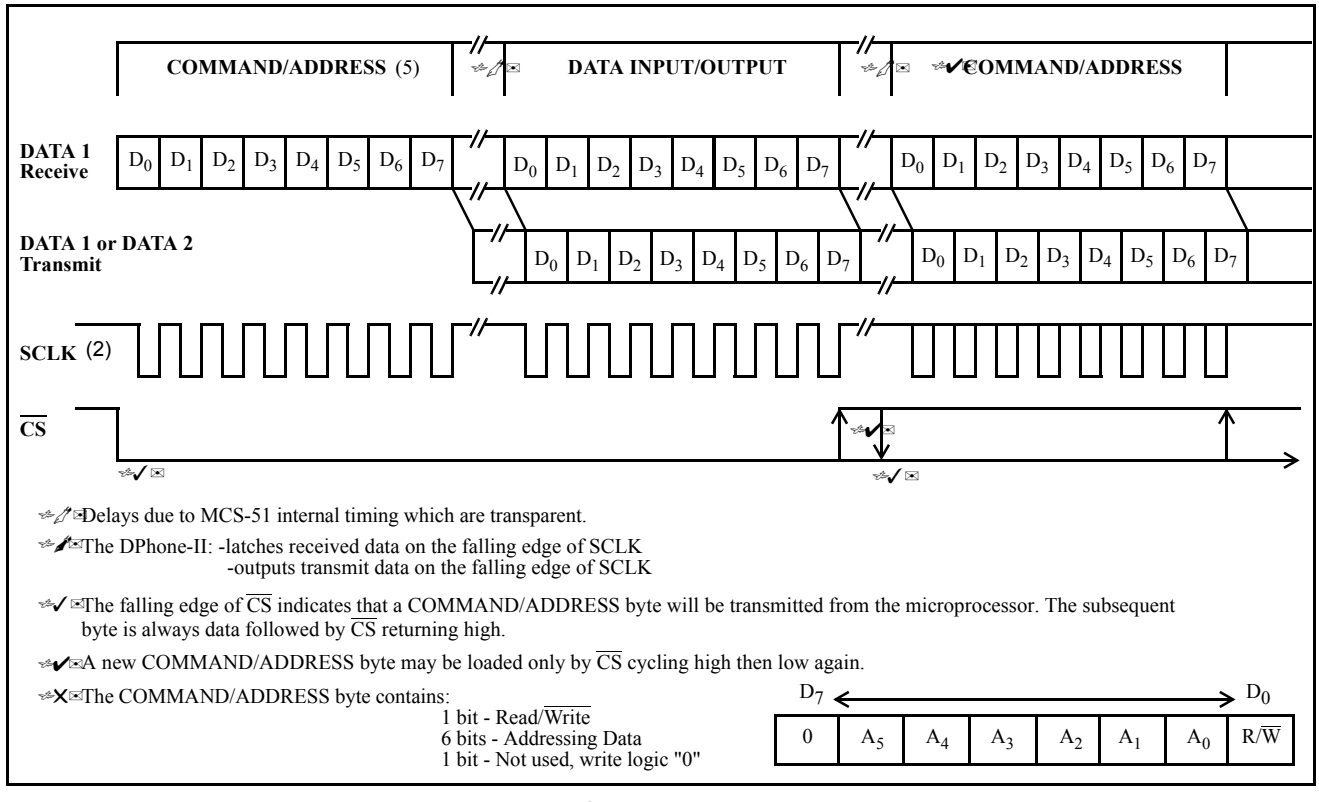


Figure 5 - Serial Port Relative Timing

ST-BUS/Timing Control

A serial link is required for the transport of data between the DPhone-II and the external digital transmission device. The DPhone-II utilizes the ST-BUS architecture defined by Zarlink Semiconductor. Refer to Zarlink Application Note

MSAN-126. The DPhone-II ST-BUS consists of output and input serial data streams, DSTo and DSTi respectively, a synchronous clock signal C4i, and a framing pulse F0i.

The data streams operate at 2048 kb/s and are Time Division Multiplexed into 32 identical channels of 64 kb/s bandwidth. Frame Pulse (a 244 nSec low going pulse) is used to parse the continuous serial data streams into the 32 channel TDM frames. Each frame has a 125 μSecond period translating into an 8 kHz frame rate. Valid frame pulse occurs when F0i is logic low coincident with a falling edge of C4i. C4i has a frequency (4096 MHz) which is twice the data rate. This clock is used to sample the data at the _ bit-cell position on DSTi and to make data available on DSTo at the start of the bit-cell. C4i is also used to clock the DPhone-II internal functions (i.e., DSP, Filter/CODEC, HDLC) and to provide the channel timing requirements.

The DPhone-II uses channels 1, 2 & 3 of the 32 channel frame. These channels are always defined, beginning with the first channel after frame pulse, as shown in Figure 6 (DSTi and DSTo channel assignments). Channels are enabled independently by the three control bits Ch_1En -Ch_3En residing in the Timing Control Register (address15h).

Ch_1EN - C-Channel

Channel 1 conveys the control/status information for Zarlink's layer 1 transceiver. The full 64 kb/s bandwidth is available and is assigned according to which transceiver is being used. Consult the data sheet for the selected transceiver for its bit definitions and order of bit transfer. When this bit is high register data is transmitted on DSTo. When low, this timeslot is tri-stated on DSTo. Receive C-Channel data (DSTi) is always routed to the register regardless of this control bit's logic state. C-channel data is transferred on the ST-BUS MSB first by the DPhone-II.

Ch_2EN and Ch_3EN - B1-Channel and B2-Channel

Channels 2 and 3 are the B1 and B2 channels, respectively. These bits (Ch_2EN and Ch_3EN) are used to enable the PCM channels from/to the DPhone-II as required.

Transmit PCM on DSTo

When high, PCM from the Filter/CODEC and DSP is transmitted on DSTo in the selected ST-BUS channel. When low, DSTo is forced to logic 0 for the corresponding timeslot. If both Ch_2EN and Ch_3EN are enabled, default is to channel 2.

Receive PCM from DSTi

When high, PCM from DSTi is routed to the DSP and Filter/CODEC in the associated channel. If both Ch_2EN and Ch_3EN are enabled the default is to channel 2.

New Call Tone

The New Call Tone Generator produces a frequency shifted square-wave used to toggle the speaker driver outputs. This is intended for use where a ringing signal is required concurrently with an already established voice conversation in the handset.

Programming of the DSP for New Call generator is exactly as is done for the tone ringer micro-program except that the OPT bit (DSP Control Register, address 1Eh) is set high. In this mode the DSP does not produce a frequency shifted squarewave output to the filter CODEC section. Instead the DSP uses the contents of the tone coefficient registers, along with the tone warble rate register, to produce a gated squarewave control signal output which toggles between the programmed frequencies. This control signal is routed to the New Call Tone block when the NCT EN control bit is set (General Control Register, address 0Fh). NCT EN also enables a separate gain control block, for controlling the loudness of the generated ringing signal. With the gain control block set to 0 dB the output is at maximum or 6 volts p-p. Attenuation of the applied signal, in three steps of 8 dB, provide the four settings for New Call tone (0, -8, -16, -24 dB). The NCT gain bits ($NCTG_0$-$NCTG_1$) reside in the FCODEC Gain Control Register 2 (address 0Bh).

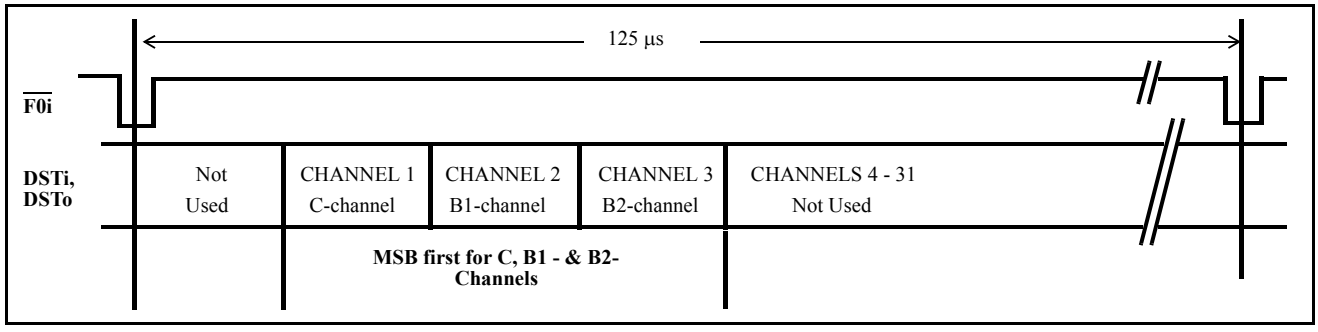


Figure 6 - ST-BUS Channel Assignment

Watchdog

To maintain program integrity an on-chip watchdog timer is provided for connection to the microcontroller reset pin. The watchdog output WD (pin 17) goes high while the DPhone-II is held in reset via the $\overline{PWRST}$ (pin 6). Release of $\overline{PWRST}$ will cause WD to return low immediately and will also start the watchdog timer. The watchdog timer is clocked on the falling edge of $\overline{F0i}$ and requires only this input, along with V_{DD}, for operation.

If the watchdog reset word is written to the watchdog register (address 11h) after $\overline{PWRST}$ is released, but before the timeout period (T=512mSec) expires, a reset of the timer results and WD will remain low. Thereafter, if the reset word is loaded correctly at intervals less than 'T' then WD will continue low. The first break from this routine, in which the watchdog register is not written to within the correct interval or it is written to with incorrect data, will result in a high going WD output after the current interval 'T' expires. WD will then toggle at this rate until the watchdog register is again written to correctly.

5-BIT WATCHDOG RESET WORD

			W4	W3	W2	W1	W0
X	X	X	0	1	0	1	0

x=don't care

DPhone-II Register Map

Address (Hex)	WRITE	READ
00-09	RESERVED	RESERVED
0A	FCODEC GAIN CONTROL REGISTER 1	VERIFY
0B	FCODEC GAIN CONTROL REGISTER 2	VERIFY
0C	RESERVED	RESERVED
0D	RESERVED	RESERVED
0E	TRANSDUCER CONTROL REGISTER	VERIFY
0F	GENERAL CONTROL REGISTER	VERIFY
10	RESERVED	RESERVED
11	WATCHDOG REGISTER	NOT USED
12	LCD SEGMENT ENABLE REGISTER 1	VERIFY
13	LCD SEGMENT ENABLE REGISTER 2	VERIFY
14	C-CHANNEL REGISTER (to DSTo)	C-CHANNEL REGISTER (from DSTi)
15	TIMING CONTROL REGISTER	VERIFY
16	LOOP-BACK REGISTER	VERIFY
17-1C	RESERVED	RESERVED

DPhone-II Register Map

Address (Hex)	WRITE	READ
1D	RECEIVE GAIN CONTROL REGISTER	VERIFY
1E	DSP CONTROL REGISTER	VERIFY
1F	RESERVED	RESERVED
20	TRANSMIT AUDIO GAIN REGISTER	VERIFY
21	TRANSMIT DTMF GAIN REGISTER	VERIFY
22	RESERVED	RESERVED
23	TONE COEFFICIENT REGISTER 1	VERIFY
24	TONE COEFFICIENT REGISTER 2	VERIFY
25	RESERVED	RESERVED
26	TONE RINGER WARBLE RATE REGISTER	VERIFY
27-3F	RESERVED	RESERVED

Test Loops

Detail LBio and LBoi Loopback Register (address 16h)

LBio Setting this bit causes data on DSTi to be looped back to DSTo directly at the pins. The appropriate channel enables Ch_1EN -Ch_3EN must also be set.

LBoi Setting this bit causes data on DSTo to be looped back to DSTi directly at the pins.

Register Summary

This section contains a complete listing of the DPhone-II register addresses, the control/status bit mapping associated with each register and a definition of the function of each control/status bit.

The Register Summary may be used for future reference to review each of the control/status bit definitions without the need to locate them in the text of the functional block descriptions.

ADDRESSES 00h and 09h are RESERVED

FCODEC Gain Control Register 1 ADDRESS = 0Ah WRITE/READ VERIFY

Power Reset Value
X000 X000

-	$RxFG_2$	$RxFG_1$	$RxFG_0$	-	$TxFG_2$	$TxFG_1$	$TxFG_0$
7	6	5	4	3	2	1	0

Receive Gain Setting (dB)	$RxFG_2$	$RxFG_1$	$RxFG_0$
(default) 0	0	0	0
-1	0	0	1
-2	0	1	0
-3	0	1	1
-4	1	0	0
-5	1	0	1
-6	1	1	0
-7	1	1	1

$RxFG_n$ = Receive Filter Gain n

Transmit Gain Setting (dB)	$TxFG_2$	$TxFG_1$	$TxFG_0$
(default) 0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

$TxFG_n$ = Transmit Filter Gain n

FCODEC Gain Control Register 2 ADDRESS = 0Bh WRITE/READ VERIFY

Power Reset Value
0X00 X000

-	-	$NCTG_1$	$NCTG_0$	-	STG_2	STG_1	STG_0
7	6	5	4	3	2	1	0

Gain (dB)	$NCTG_1$	$NCTG_0$
0 (default)	0	0
-8	0	1
-16	1	0
-24	1	1

NCTGn = New Call Tone Gain n

Side-tone Gain Setting (dB)	STG_2	STG_1	STG_0
(default) OFF	0	0	0
-9.96	0	0	1
-6.64	0	1	0
-3.32	0	1	1
0	1	0	0
3.32	1	0	1
6.64	1	1	0
9.96	1	1	1

STG_n= Side-tone Gain n

ADDRESSES 0Ch and 0Dh are RESERVED

Note: Bits marked "-" are reserved bits and should be written with logic "0".

Transducer Control Register ADDRESS = 0Eh WRITE/READ VERIFY

Power Reset Value
0000 0000

PuFC	Tfhp	DIAL EN	SIDE EN	MIC EN	MIC/ HNSTMIC	SPKR EN	HSSPKR EN
7	6	5	4	3	2	1	0

PuFC	When high, the Filter/CODEC is powered up. When low, the Filter/CODEC is powered down. If PuFC, SPKR EN and HSSPKR EN are all low then the VRef/VBias circuit is also powered down.
Tfhp	When high, an additional high pass function (passband beginning at 400 Hz) is inserted into the transmit path. When low, this highpass filter is disabled.
DIAL EN	When high, a first order lowpass filter is inserted into the receive path (3 dB = 1 kHz). When low, this lowpass filter is disabled.
SIDE EN	When high, the sidetone path is enabled (assuming STG_{2-0} are not all low). When low, the sidetone path is disabled.
MIC EN	When high, the selected transmit microphone is enabled to the transmit filter section. When low, the microphone path is muted.
MIC/$\overline{\text{HNSTMIC}}$	When high, the handsfree microphone (pins MIC±) is muxed into the transmit path. When low, the handset microphone (pins M±) is muxed into the transmit path. Both are contingent on "MIC EN".
SPKR EN	When high, the handsfree loudspeaker driver is powered up. When low, this driver is powered down.
HSSPKR EN	When high, the handset speaker driver is powered up. When low, this driver is powered down.

General Control Register ADDRESS = 0Fh WRITE/READ VERIFY

Power Reset Value
0000 0000

RST	DATA SEL	A/$\overline{\mu}$	Sign-Mag/ $\overline{\text{CCITT}}$	Rx A/$\overline{\mu}$	MIC A/$\overline{\mu}$	Side A/$\overline{\mu}$	NCT EN
7	6	5	4	3	2	1	0

RST	Active high reset. Performs the same function as $\overline{\text{PWRST}}$ but does not affect the microport or the watchdog circuits. To remove this reset a $\overline{\text{PWRST}}$ must occur or this bit must be written low.
DATASEL	When high, the microport transmit and receive are performed on separate pins. DATA1 is receive while DATA2 is transmit. When low, the microport conforms to Intel MCS-51 mode 0 specifications; DATA1 is a bi-directional (transmit/receive) serial data pin while DATA2 is internally disconnected and tri-stated.
A/$\overline{u}$	When high, A-Law (de)coding is selected. When low, μ-Law (de)coding is selected.
Sign-mag/$\overline{\text{CCITT}}$	When high, sign-magnitude bit coding is selected, When low, true CCITT PCM coding is selected.
RxA/$\overline{u}$	When high, the receiver driver nominal gain is set at -9.7 dB. When low this driver nominal gain is set at -12.3 dB.
MICA/$\overline{u}$	When high, the transmit amplifier nominal gain is set at 15.4 dB. When low this amplifier nominal gain is set at 6.1 dB.
SIDEA/$\overline{u}$	When high, the side-tone nominal gain is set at -18.8 dB. When low this nominal gain is set at -11 dB.
NCT EN	When high, the new call tone generator output from the DSP is selected as the source for the loudspeaker path. When low, the CODEC output is selected for the loudspeaker path. Note that SPKR EN must also be set high for new call tone to function.

ADDRESS 10h is RESERVED

Note: Bits marked "-" are reserved bits and should be written with logic "0".

Watchdog Register ADDRESS = 11h WRITE

Power Reset Value
XXX0 1010

-	-	-	W_4	W_3	W_2	W_1	W_0
7	6	5	4	3	2	1	0

WATCHDOG RESET WORD - XXX01010

LCD Segment Enable Register 1 ADDRESS = 12h WRITE/READ VERIFY

Power Reset Value
0000 0000

SC_8	SC_7	SC_6	SC_5	SC_4	SC_3	SC_2	SC_1
7	6	5	4	3	2	1	0

Twelve segment control bits used for the LCD outputs. When high the respective segment is on. When low the respective segment is off.

LCD Segment Enable Register 2 ADDRESS = 13h WRITE/READ VERIFY

Power Reset Value
XXXX 0000

-	-	-	-	SC_{12}	SC_{11}	SC_{10}	SC_9
7	6	5	4	3	2	1	0

Twelve segment control bits used for the LCD outputs. When high the respective segment is on. When low the respective segment is off.

C-Channel Register ADDRESS = 14h WRITE/READ

Power Reset Value
Write = 1111 1111
Read = Not Applicable

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
7	6	5	4	3	2	1	0

Micro-port access to the ST-BUS C-Channel information.

Note: Bits marked "-" are reserved bits and should be written with logic "0".

Timing Control Register ADDRESS = 15h WRITE/READ VERIFY

Power Reset Value
XX0X 0000

7	6	5	4	3	2	1	0
-	-	-	-	CH_3EN	CH_2EN	CH_1EN	-

All bits active high:

Ch_2EN and Ch_3EN

Channels 2 and 3 are the B1 and B2 channels, respectively. PCM associated with the DSP, Filter/CODEC and transducer audio paths is conveyed in one of these channels as selected in the timing control register.

Transmit B1 and B2 data on DSTo

When high PCM from the Filter/CODEC and DSP is transmitted on DSTo in the associated channel. When low DSTo is forced to logic 0 for the corresponding timeslot. If both Ch_2EN and Ch_3EN are enabled, data defaults to channel 2.

Receive B1 and B2 data on DSTi

When enabled PCM from DSTi is routed to the DSP and Filter/CODEC in the associated channel. If both Ch_2EN and Ch_3EN are enabled, data input defaults to channel 2.

Ch_1EN Channel 1 conveys the control/status information for the layer 1 transceiver. The full 64kb/s bandwidth is available and is assigned according to which transceiver is being used. Consult the data sheets for the transceiver selected. When high register data is transmitted on DSTo. When low this timeslot is tri-stated on DSTo. Receive C-Channel data (DSTi) is always routed to the register regardless of this control bit's logic state.

Loop-back Register ADDRESS = 16h WRITE/READ VERIFY

Power Reset Value
X00X XXXX

7	6	5	4	3	2	1	0
-	LBio	LBoi	-	-	-	-	-

LB_{io} Active high enables data from the ST-BUS input to be looped back to the ST-BUS output directly at the pins. The DSTo tri-state driver must also be enabled using one of the channel enable signals.

LB_{oi} Active high enables data from ST-BUS output to be looped back to the ST-BUS input directly at the pins.

ADDRESSES 17h - 1Ch are RESERVED

Note: Bits marked "-" are reserved bits and should be written with logic "0".

Receive Gain Control Register ADDRESS = 1Dh WRITE/READ VERIFY

Power Reset Value
0000 0000

-	AUTO	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

AUTO When high autonulling of the transmit PCM is enabled. When low, autonulling is disabled. This bit is used in conjunction with the PS2 - PS0 bits of the DSP Control Register at address 1Eh.

B5-B0 These 6 bits (indicated below in hexadecimal) are decoded to control Rx PCM gain:

B5-B0	Gain Setting (dB)	B5-B0	Gain Setting (dB)
3F	+22.5	1F	-25.5
3E	+21.0	1E	-27.0
3D	+19.5	1D	-28.5
3C	+18.0	1C	-30.0
3B	+16.5	1B	-31.5
3A	+15.0	1A	-33.0
39	+13.5	19	-34.5
38	+12.0	18	-36.0
37	+10.5	17	-37.5
36	+9.0	16	-39.0
35	+7.5	15	-40.5
34	+6.0	14	-42.0
33	+4.5	13	-43.5
32	+3.0	12	-45.0
31	+1.5	11	-46.5
30	+0.0	10	-48.0
2F	-1.5	0F	-49.5
2E	-3.0	0E	-51.0
2D	-4.5	0D	-52.5
2C	-6.0	0C	-54.0
2B	-7.5	0B	-55.5
2A	-9.0	0A	-57.0
29	-10.5	09	-58.5
28	-12.0	08	-60.0
27	-13.5	07	-61.5
26	-15.0	06	-63.0
25	-16.5	05	-64.5
24	-18.0	04	-66.0
23	-19.5	03	-67.5
22	-21.0	02	-69.0
21	-22.5	01	-70.5
20	-24.0	00	-72.0

Note: B0-B5 of addresses 20h and 21h are encoded in the same manner

Note: Bits marked "-" are reserved bits and should be written with logic "0".

DSP Control Register ADDRESS = 1Eh WRITE/READ VERIFY

PS2	PS1	PS0	OPT	RxMUTE	TxMUTE	-	$\overline{\text{DRESET}}$
7	6	5	4	3	2	1	0

Power Reset Value
0000 0000

OPT: When high, the tone ringer is in New Call tone mode. When low the normal tone ringer program is executed.

RxMUTE: This bit when high turns off the receive PCM channel, substituting quiet code.

TxMUTE: This bit when high turns off the transmit PCM channel, substituting quiet code.

$\overline{\text{DRESET}}$: This bit (when high) enables the DSP. If low, no programs are executed, the master clock is disabled and the program counter is reset to zero.

PS2-PS0: These bits are program select bits for the DSP Rom programs.

PS2	PS1	PS0	MICRO-PROGRAM
0	0	0	Power up reset program
0	0	1	Gain control program
0	1	0	DTMF & Gain control program
0	1	1	Tone Ringer & Gain control program
1	0	0	Handsfree program
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

ADDRESS 1Fh is RESERVED

Transmit Audio Gain Register ADDRESS = 20h WRITE/READ VERIFY

-	-	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Power Reset Value
XX11 0000

This register controls the transmit speech path gain in 1.5dB steps as in Receive Gain Register (address 1Dh).

Transmit DTMF Gain Register ADDRESS = 21h WRITE/READ VERIFY

-	-	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Power Reset Value
XX10 1110

This register controls the transmit DTMF level in 1.5dB steps as in Receive Gain Register (address 1Dh).

ADDRESS 22h is RESERVED

Note: Bits marked "-" are reserved bits and should be written with logic "0".

Tone Coeff Register 1-DTMF or Tone Ringer ADDRESS = 23h WRITE/READ VERIFY

B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Power Reset Value
0000 0000

This register is used to program the low-group frequency of the DTMF program. The tone coefficient is calculated as follows:

COEF = 0.128 x Frequency
where: Frequency is in Hz (note: COEF must be converted to an 8 bit binary integer)
Highest frequency possible: *1992.2 Hz*
Lowest frequency possible: *7.8 Hz*
Frequency resolution: *7.8 Hz*
Pre-twist: *-2.1 dB ± 0.2 dB*

This register is used to program the first frequency of the squarewave ringer program. The tone coefficient is calculated as follows:

COEF = 8000 / Frequency
where: Frequency is in Hz (note: COEF must be rounded off and converted to an 8 bit binary integer)
Highest frequency possible: *4000 Hz*
Lowest frequency possible: *31.4 Hz*
Frequency resolution: *non-linear*

This tone can be disabled by writing zero to this register for single tone generation.

Tone Coeff Register 2-DTMF or Tone Ringer ADDRESS = 24h WRITE/READ VERIFY

B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Power Reset Value
0000 0000

This register is used to program the high-group frequency of the DTMF program. The tone coefficient is calculated as follows:

COEF = 0.128 x Frequency
where: Frequency is in Hz (note: COEF must be converted to an 8 bit binary integer)
Highest frequency possible: *1992.2 Hz*
Lowest frequency possible: *7.8 Hz*
Frequency resolution: *7.8 Hz*
Pre-twist: *0 dB*

This register is used to program the second frequency of the squarewave program. The tone coefficient is calculated similarly to tone coefficient register 1.

ADDRESS 25h is RESERVED

Tone Ringer Warble Rate-Tone Ringer ADDRESS = 26h WRITE/READ VERIFY

B7	B6	B5	B4	B3	B2	B1	B0
7	6	5	4	3	2	1	0

Power Reset Value
0000 0000

The tone ringer will switch between squarewave frequencies at a warble frequency defined by this register. The relationship between the duration period of each tone and the 8 bit warble coefficient is as follows:

Tone duration (warble frequency) = 500 / COEF

where: Frequency is in Hz, and 0≤COEF <256

Highest frequency possible: *500 Hz*

Lowest frequency possible: *2.0 Hz*

Frequency resolution: *non-linear*

Addresses: 27h to 2Dh are transmit and receive gains and coefficients used by the filters in the handsfree decision circuit.

2Eh to 3Fh are scratch-pad ram locations used by the DSP algorithms as temporary storage during calculations.

Applications

To maintain a fully differential topology in the transmit path the suggested connection scheme for the transmit microphones is shown in Figure 7. However, it is possible to use a single-ended arrangement as shown in Figure 8 for the transmit interface. In this case the dynamic range of the MT9094 is reduced by half. In both figures the output drivers are connected in a fully differential manner.

The MT9094 is a member of the Zarlink family of digital terminal equipment components. There are two transmission devices which connect directly with the MT9094 to complete an application; the MT8930 (SNIC) and the MT8971/72 (DSIC/DNIC). An ISDN 4-wire "TE" function is implemented with the MT8930/MT9094 combination. A 2-wire digital phone for PABX, key-systems and other proprietary applications is implemented with the MT8971/72/MT9094 combination.

Figures 9 and 10 show the 4-wire and 2-wire applications, respectively.

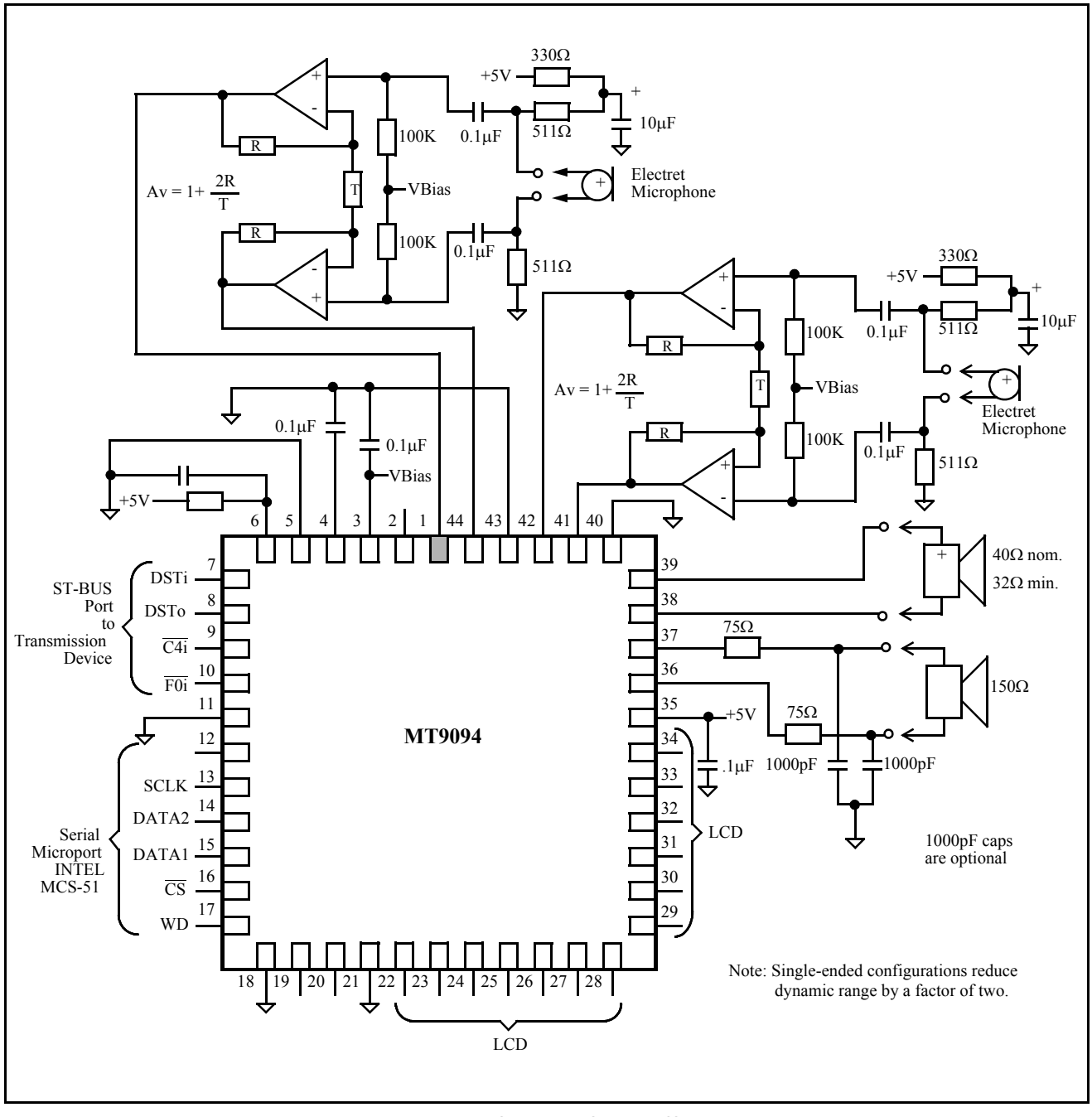


Figure 7 - Application Circuit - fully differential audio input

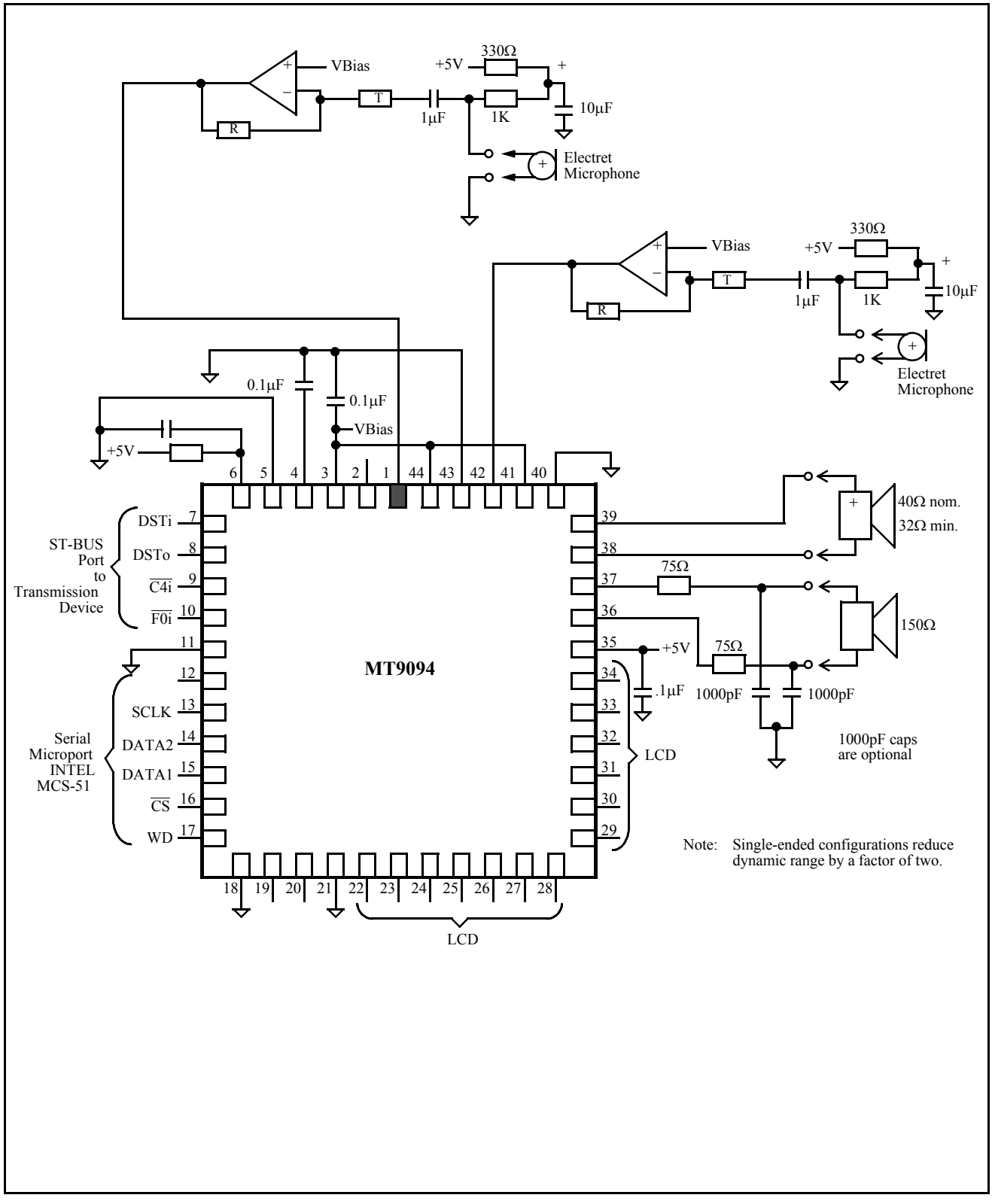


Figure 8 - Application Circuit - single-ended audio input

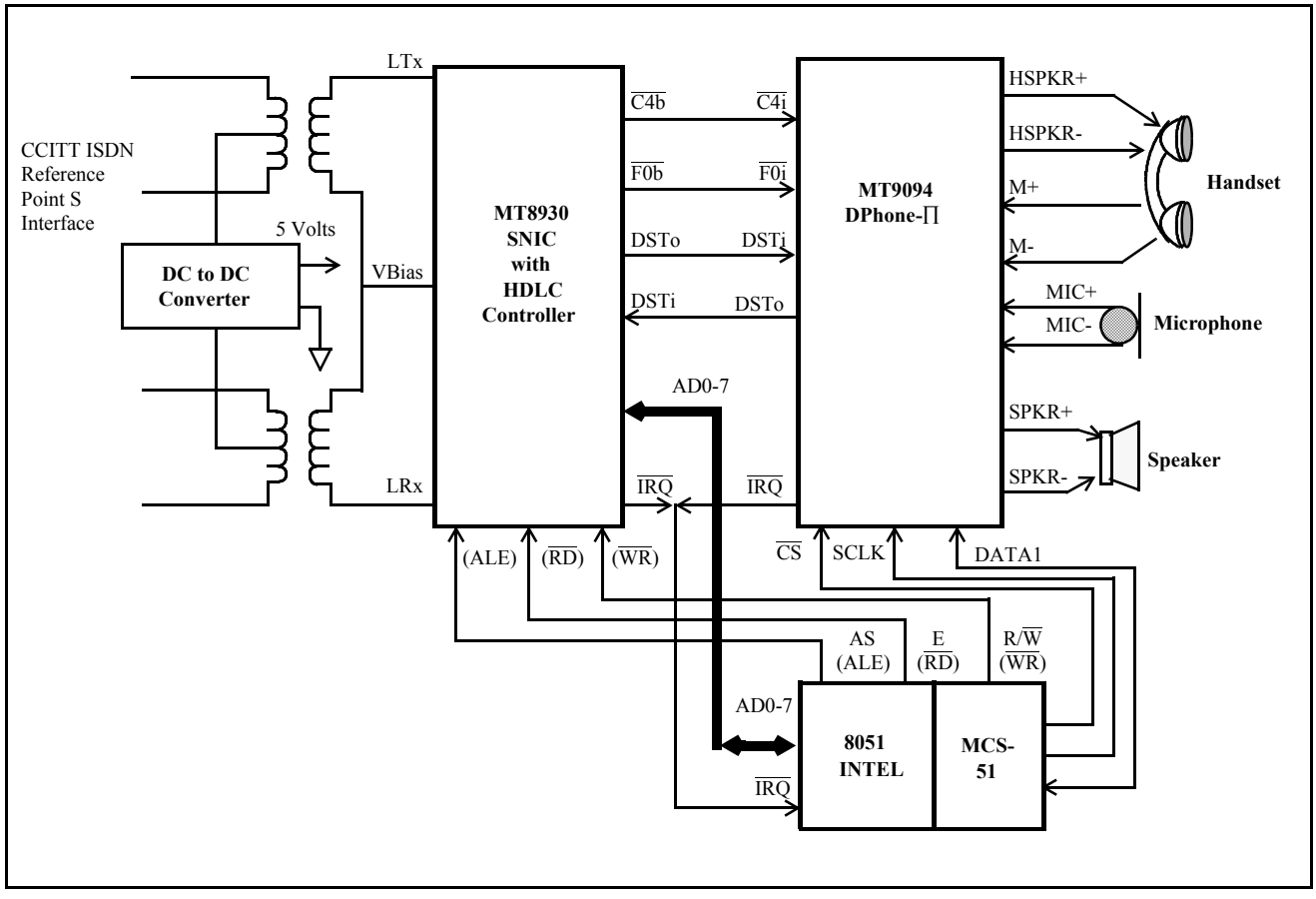


Figure 9 - CCITT ISDN Voice/Data Terminal Equipment - TE1

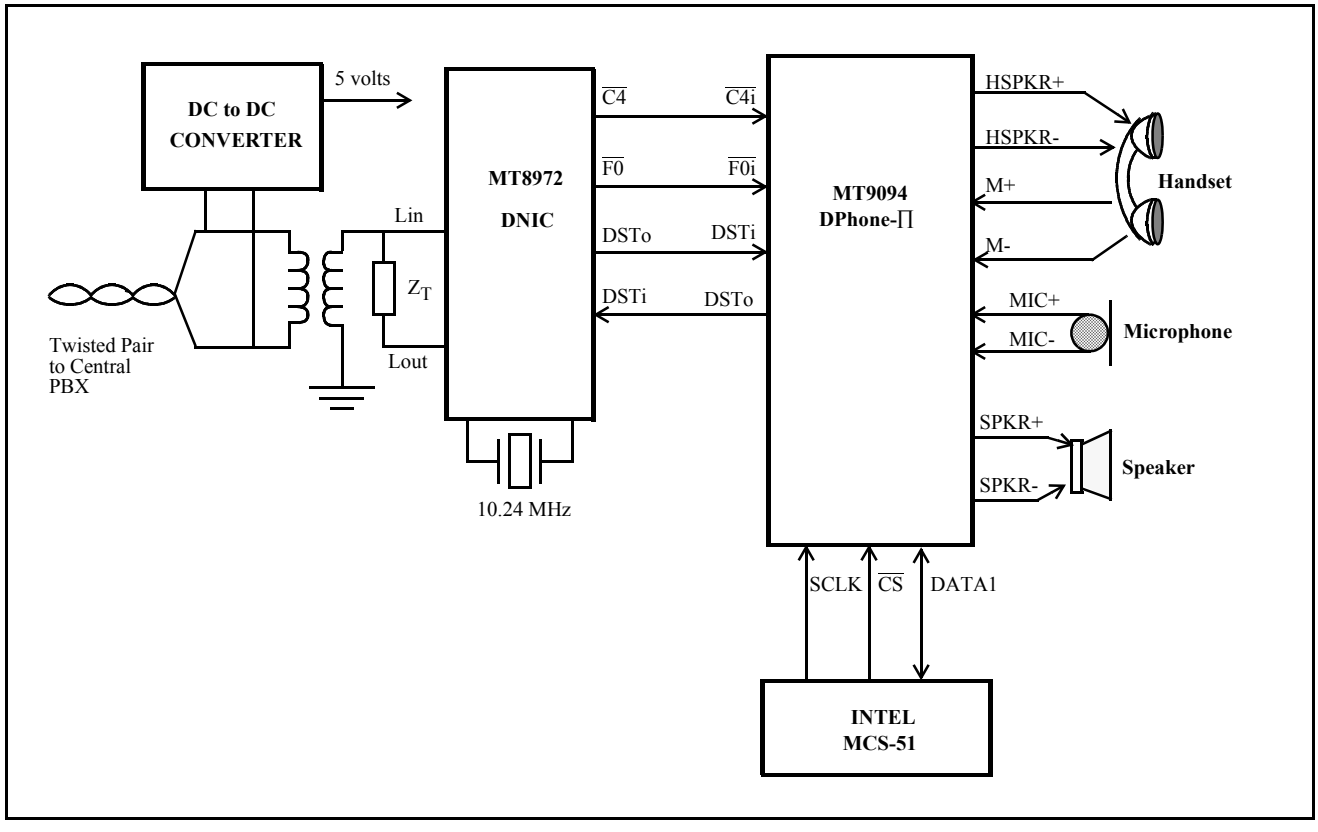


Figure 10 - Voice/Data Digital Telephone Set Circuit

Programming Examples

Some examples of the programming steps required to set-up various telephony functions are given. Note that these steps are from the power-up reset default definition. If some other state is currently true then some programming steps may be omitted while new ones may be required.

Standard Full-duplex handset call

Description	Address	DATA
select B-Channel of operation	15h	bits 2 or 3 (as required)
reset DSP	1Eh	00h
set Rx gain (ie 0dB with Tx autonull)	1Dh	70h (or as required)
set Tx gain (ie 0dB)	20h	30h (or as required)
start Rx gain program	1Eh	21h
select transducers and turn on sidetone and filter/CODEC	0Eh	99h
set sidetone gain	0Bh	04h (for 0dB or as required)
optional:		
set CODEC Rx and Tx gain	0Ah	as required (0dB default)
select A-Law versus μ-Law	0Fh	bits 1-5 (as required)

Half-Duplex handsfree operation

Description	Address	DATA
select B-Channel of operation	15h	bits 2 or 3 (as required)
reset DSP	1Eh	00h
set Rx gain (ie 12 dB)	1Dh	38h (or as required)
set Tx gain (ie 0dB)	20h	30 h (or as required)
start handsfree program	1Eh	81h
select transducers and filter/CODEC and turn off sidetone	0Eh	1Eh
optional:		
set CODEC Rx and Tx gain	0Ah	as required (0dB default)
select A-Law versus μ-Law	0Fh	bits 1-5 (as required)

Generate tone ringer

Description	Address	DATA
select B-Channel of operation	15h	bits 2 or 3 (as required)
reset DSP	1Eh	00h
set Rx gain (ie 0 dB with Tx autonull)	1Dh	70h (or as required)
set Tx gain (ie 0dB)	20h	30h (or as required)
write tone coefficient 1	23h	as required
write tone coefficient 2	24h	as required
write warble tone rate coefficient	26h	as required
start tone ringer program	1Eh	61h
select speaker and filter/CODEC and turn off sidetone	0Eh	82h
control ringer cadence by toggling RxMUTE	1Eh	61 (on) 69 (off) 61 (on) 69 (off) etc...

Generate DTMF tones

Description	Address	DATA
select B-Channel of operation	15h	bits 2 or 3 (as required)
reset DSP	1Eh	00h
set Rx DTMF gain (ie -20 dBm0)	1Dh	22h (or as required)
set Tx audio gain (ie 0dB)	20h	30h (or as required)
set Tx DTMF gain (ie -4dBm0)	21h	2Eh (or as required)
write tone coefficient 1	23h	as required
write tone coefficient 2	24h	as required
start DTMF program	1Eh	41h
select transducers and filter/CODEC (PuFC) and turn off sidetone	0Eh	as required
optional: set CODEC Rx gain	0Ah	as required (0dB default)
send tones in only Rx or Tx by disabling RxMUTE or TxMUTE appropriately	1Eh	as required

New Call Tone

Description	Address	DATA
Assume that a B-Channel of operation has already been selected for the concurrent handset conversation. If this is not true select one.		
select B-Channel of operation	15h	bits 2 or 3 (as required)
reset DSP	1Eh	00h
**********		
set Rx gain (ie 0 dB with Tx autonull)	1Dh	70h (or as required)
set Tx gain (ie 0dB)	20h	30h (or as required)
Note: these two steps a required for the concurrent conversation only and do not affect new call tone generation. See Standard Full-duplex handset call for required programming.		
**********		
write tone coefficient 1	23h	as required
write tone coefficient 2	24h	as required
write warble rate coefficient	26h	as required
start new call tone ringer program	1Eh	71h
set new call tone gain	0Bh	NCTG2-1 (as required)
select speaker	0Eh	02h 9Bh (assuming a concurrent handset call)
enable new call tone	0Fh	01h (assuming all other bits are μ-Law
control ringer cadence by toggling between gain control and tone ringer with gain control programs	1Eh	71h (on) 31h (off) 71h (on) etc...

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	7	V
2	Voltage on any I/O pin	V_I/V_O	V_{SS}-0.3	V_{DD}+0.3	V
3	Current on any I/O pin (transducers excluded)	I_I/I_O		±20	mA
4	Storage Temperature	T_S	-65	+150	°C
5	Power Dissipation (package) Plastic	P_D		750	mW
6	Static Discharge	ESD		±2.0	KV
7	Latch-up Current	I_{LU}	±100		mA

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5	5.25	V	
2	Input Voltage (high) *	V_{IH}	2.4		V_{DD}	V	Noise margin = 400 mV
3	Input Voltage (low) *	V_{IL}	V_{SS}		0.4	V	Noise margin = 400 mV
4	Operating Temperature	T_A	-40		+85	°C	
5	Clock Frequency ($\overline{C4i}$)	f_{CLK}	4092	4096	4100	kHz	

* Excluding $\overline{PWRST}$ which is a Schmitt Trigger Input.

Power Characteristics

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Supply Current (clock enabled, all functions off	I_{DDC1}			6	mA	
2	Supply Current by function						
	Filter/Codec	I_{DDF1}		1.5		mA	
	DSP	I_{DDF3}		1.5		mA	
	Handset Driver (bias only, no signal)	I_{DDF4}		1.5		mA	See Note 1.
	Speaker Driver (bias only, no signal)	I_{DDF5}		1.5		mA	See Note 1.
	Timing Control, C-Channel, ST-BUS, etc.	I_{DDF6}		1.0		mA	
	Total all functions enabled	I_{DDFT}		7.0	14	mA	See Note 2.

Note 1: Power delivered to the load is in addition to the bias current requirements.
Note 2: I_{DDFT} is not additive to I_{DDC1}.

DC Electrical Characteristics† (except LCD Drive Pins) - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input HIGH Voltage TTL inputs	V_{IN}	2.0			V	
2	Input LOW Voltage TTL inputs	V_{IL}			0.8	V	
3	VBias Voltage Output	V_{Bias}		$V_{DD}/2$		V	Max. Load = 100 µA
4	Input Leakage Current [1]	I_{IZ}		0.1	10	µA	$V_{IN} = V_{DD}$ to V_{SS}
5	Positive Going Threshold Voltage ($\overline{PWRST}$ only) Negative Going Threshold Voltage ($\overline{PWRST}$ only)	V_{T+} V_{T-}	3.3		1.5		
6	Output HIGH Current TTL O/P	I_{OH}	-10	-16		mA	V_{OH} = 2.4V DSTo, $\overline{WD}$, DATA1, DATA2
7	Output LOW Current TTL O/P	I_{OL}	5	10		mA	V_{OL} = 0.4V DSTo, $\overline{WD}$, DATA1, DATA2
8	Output Voltage	V_{Ref}		$(V_{DD}/2)$-1.5		V	No load
9	Output Leakage Current [1]	I_{OZ}		0.01	10	µA	$V_{OUT} = V_{DD}$ and V_{SS}
10	Output Capacitance	C_o		15		pF	
11	Input Capacitance	C_i		10		pF	

† DC Electrical Characteristics are over recommended temperature and range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1 TTL compatible pins only.

DC Electrical Characteristics† - LCD Drive Pins - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Output High Voltage Both Segment and Backplane	V_{OH}	4.8	---	---	Volts	Io = 1 mA, V_{DD} = 5 V
2	Output Low Voltage Both Segment and Backplane	V_{OL}	---	---	0.2	Volts	Io = 1 mA, V_{DD} = 5 V
3	Segment Output Load		---	---	1200	pF	
4	Backplane Output Load		---	---	7200	pF	
5	Frequency		62	62.5	63	Hz	

AC Characteristics† for A/D (Transmit) Path - 0dBm0 = 1.421V_{rms} for μ-Law and 1.477V_{rms} for A-Law, at the CODEC. (V_{Ref} = 0.5 volts and V_{Bias} = 2.5 volts). All parameters pertain exclusively to the Filter/CODEC except absolute half-channel gain and transmit idle channel noise.

	Characteristics	Sym.	Min.	Typ.‡	Max	Units	Test Conditions
1	Analog input equivalent to overload decision	$A_{Li3.17}$ $A_{Li3.14}$		5.79 6.0		Vp-p Vp-p	μ-Law A-Law Both at CODEC
2	Absolute half-channel gain. Transmit filter gain = 0 dB setting	G_{AX1} G_{AX2}	5.4 14.7	6.1 15.4	6.8 16.1	dB dB	MICA/$\overline{u}$=0* MICA/$\overline{u}$=1* MIC± or M± to PCM 1020Hz
	All other transmit filter settings (1 to 7 dB) are in addition to 0 dB setting	G_{AX1} G_{AX2}	-0.15 -0.15		+0.15 +0.15	dB dB	MICA/$\overline{u}$=0* MICA/$\overline{u}$=1* from nominal MIC± or M± to PCM 1020 Hz
3	Gain tracking vs. input level CCITT G.714 Method 2	G_{TX}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total Distortion vs. input level CCITT G.714 Method 2	D_{QX}	35 29 24			dB dB dB	0 to -30dBm0 -40 dBm0 -45 dBm0
5	Transmit Idle Channel Noise	N_{CX} N_{PX}		15 -72	17.5 -66	dBrnC0 dBrn0p	μ-Law A-Law
6	Gain relative to gain at 1020 Hz <50 Hz 60 Hz 200 Hz 300-3000 Hz 3000-3400 Hz 4000 Hz >4600 Hz	G_{RX}	 -0.25 -0.9		 -25 -30 0.0 0.25 0.25 -12.5 -25	 dB dB dB dB dB dB dB	
7	Absolute Delay	D_{AX}		360		μs	at frequency of minimum delay
8	Group Delay relative to D_{AX}	D_{DX}		750 380 130 750		μs μs μs μs	500-600 Hz 600-1000 Hz 1000-2600 Hz 2600 - 2800 Hz
9	Power Supply Rejection f=1020 Hz f=0.3 to 3 kHz f=3 to 4 kHz f=4 to 50 kHz	 PSSR PSSR1 PSSR2 PSSR3	 37 40 35 40			 dB dB dB dB	100mV_{rms} signal μ-Law PSSR1-3 not production tested

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note: MICA/$\overline{u}$, refer to General Control Register, address 0Fh.

AC Characteristics† for D/A (Receive) Path - 0dBm0 = 1.421V_{rms} for μ-Law and 1.477V_{rms} for A-Law, at the CODEC. (V_{Ref} = 0.5 volts and V_{Bias} = 2.5 volts). All parameters pertain exclusively to the Filter/CODEC except absolute gain and receive idle channel noise.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Analog output at the CODEC full scale	$A_{Lo3.17}$ $A_{Lo3.14}$		5.704 5.906		Vp-p Vp-p	μ-Law A-Law
2	Absolute half-channel gain. Receive filter gain = 0 dB setting	G_{AR1} G_{AR2} G_{AR3}	-0.6 -12.9 -10.3	0.2 -12.3 -9.7	0.95 -11.8 -9.1	dB dB dB	PCM to SPKR± PCM to HSPKR±, RxA/$\overline{u}$=0* PCM to HSPKR±, RxA/$\overline{u}$=1* 1020Hz
	All other receive filter settings (-1 to -7 dB) are in addition to 0 dB setting	G_{AR1} G_{AR2} G_{AR3}	-0.15 -0.15 -0.15		+0.15 +0.15 +0.15	dB dB dB	PCM to SPKR± PCM to HSPKR±, RxA/$\overline{u}$=0* PCM to HSPKR±, RxA/$\overline{u}$=1* from nominal 1020Hz
3	Gain tracking vs. input level CCITT G.714 Method 2	G_{TR}	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB	3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
4	Signal to total distortion vs. input level CCITT G.714 Method 2	G_{QR}	35 29 24			dB dB dB	0 to -30dBm0 -40 dBm0 -45 dBm0
5	Receive Idle Channel Noise	N_{CR} N_{PR}			15.5 -75	dBrnC0 dBrn0p	μ-Law A-Law
6	Gain relative to gain at 1020 Hz 200 Hz 300-3000 Hz 3000-3400 Hz 4000 Hz >4600 Hz	G_{RR}	 -0.25 -0.90		 0.25 0.25 0.25 -12.5 -25	 dB dB dB dB dB	
7	Absolute Delay	D_{AR}		240		μs	at frequency of min. delay
8	Group Delay relative to D_{AR}	D_{DR}		750 380 130 750		μs μs μs μs	500-600 Hz 600-1000 Hz 1000-2600 Hz 2600 - 2800 Hz
9	Crosstalk D/A to A/D A/D to D/A	CT_{RT} CT_{TR}			-74 -80	dB dB	G.714.16

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Note: RxA/$\overline{u}$, refer to General Control Register, address 0Fh.

AC Electrical Characteristics† for Side-tone Path

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Absolute path gain Gain adjust = 0 dB	G_{AS1} G_{AS2}	-17.2- 13.1	-16.7 -12.6	16.2 -12.1	dB dB	SIDEA/$\overline{u}$, MICA/$\overline{u}$, RxA/$\overline{u}$ all 0 SIDEA/$\overline{u}$, MICA/$\overline{u}$, RxA/$\overline{u}$ all 1 M± inputs to HSPKR± outputs 1000Hz
	All other settings (-9.96 to +9.96 dB)	G_{AS} G_{AS}	-0.3 -0.3		+0.3 +0.3	dB dB	SIDEA/$\overline{u}$=0 SIDEA/$\overline{u}$=1 from nominal relative measurements w.r.t. G_{AS1} & G_{AS2}

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† for New Call Tone

	Characteristics	Sym.	Typ.‡	Units	Test Conditions
1	New Call Tone Output voltage (SPKR+ to SPKR-)	V_{NCT1} V_{NCT2} V_{NCT3} V_{NCT4}	6.0 2.390 0.950 0.380	Vp-p Vp-p Vp-p Vp-p	NCTG0=0, NCTG1=0 NCTG0=1, NCTG1=0 NCTG0=0, NCTG1=1 NCTG0=1, NCTG1=1 load > 34 ohms across SPKR±

† AC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics† for Analog Outputs

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Earpiece load impedance	E_{ZL}	260	300		ohms	across HSPKR±
2	Allowable Earpiece capacitive load	E_{CL}		300		pF	each pin: HSPKR+ HSPKR-
3	Earpiece harmonic distortion	E_D			0.5	%	300 ohms load across HSPKR± (tol-15%),RxA/$\overline{u}$=1, $V_O \leq 693V_{rms}$, Rx gain=0dB
4	Speaker load impedance	S_{ZL}	34	40		ohms	across SPKR±
5	Allowable Speaker capacitive load	S_{CL}		300		pF	each pin SPKR+ SPKR-
6	Speaker harmonic distortion	S_D			0.5	%	40 ohms load across SPKR± (tol-15%), $V_O \leq 6.2$Vp-p, Rx gain=0 dB

† Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Electrical Characteristics† for Analog Inputs

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Differential input voltage without overloading CODEC	V_{ID}			2.87 1.02	Vp-p Vp-p	MICA/$\overline{u}$=0, A/$\overline{u}$=0 MICA/$\overline{u}$=0, A/$\overline{u}$=1 across MIC± or M± inputs, Tx filter gain = 0 dB setting
2	Input impedance	Z_I	50			kΩ	MIC+, MIC-, M+ or M- to V_{SS}.

† Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - ST-BUS Timing (See Figure 11)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{C4i}$ Clock Period	t_{C4P}	243	244	245	ns	
2	$\overline{C4i}$ Clock High Period	t_{C4H}	121	122	123	ns	
3	$\overline{C4i}$ Clock Low Period	t_{C4L}	121	122	123	ns	
4	$\overline{C4i}$ Clock Transition Time	t_T		20	50	ns	
5	$\overline{F0i}$ Frame Pulse Setup Time	t_{F0iS}	50			ns	
6	$\overline{F0i}$ Frame Pulse Hold Time	t_{F0iH}	50			ns	
7	$\overline{F0i}$ Frame Pulse Width Low	t_{F0iW}	150			ns	
8	DSTo Delay	t_{DSToD}		100	125	ns	C_L=50 pF
9	DSTi Setup Time	t_{DSTiS}	30			ns	
10	DSTi Hold Time	t_{DSTiH}	50			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

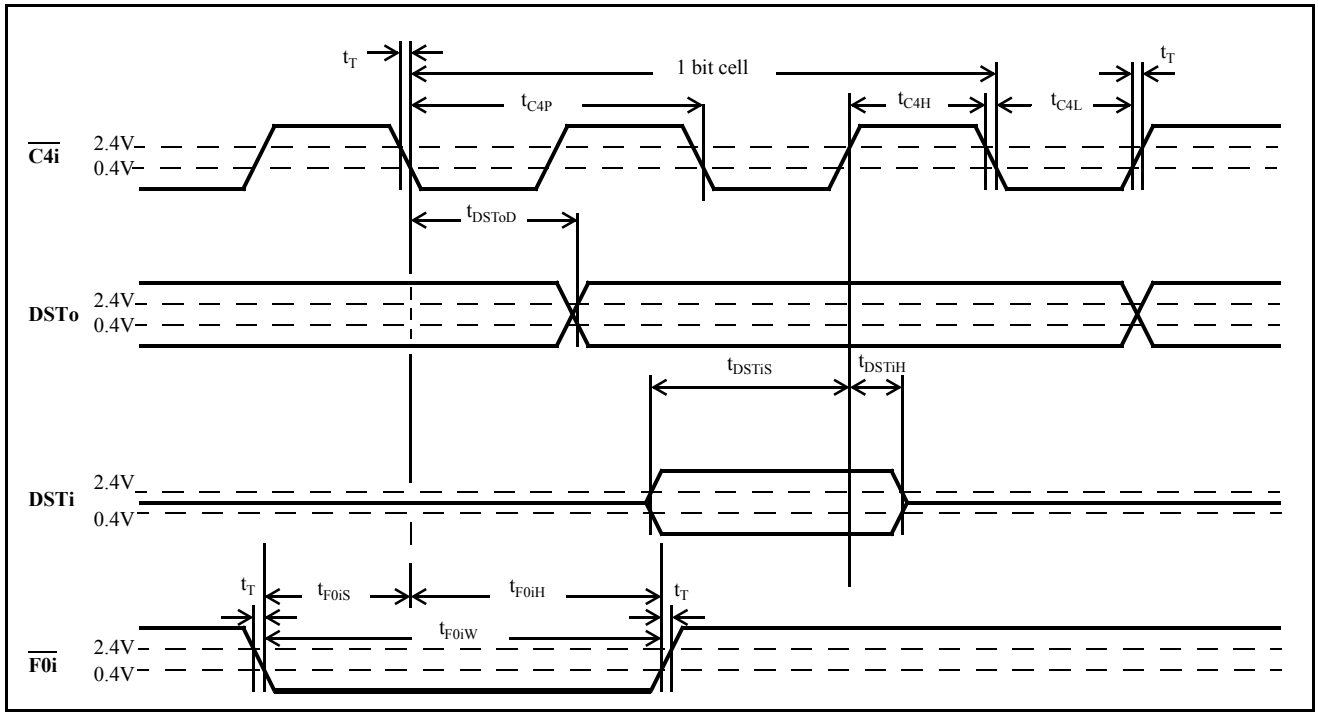


Figure 11 - ST-BUS Timing Diagram

AC Electrical Characteristics† - Microport Timing (see Figure 12)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Receive data setup	A	10			ns	
2	Receive data hold	B	10			ns	
3	Transmit data delay from clock falling edge	C			80	ns	50 pF
4	High Z to valid data from SCLK falling edge	D			80	ns	50 pF
5	Valid data to high Z from $\overline{CS}$ rising edge	E			80	ns	50 pF
6	Current transmit data hold from clock falling edge	F			0	ns	
7	Chip Select to SCLK setup and hold times	G	0			ns	
8	SCLK clock period (3 MHz)	H	333			ns	

† Timing is over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

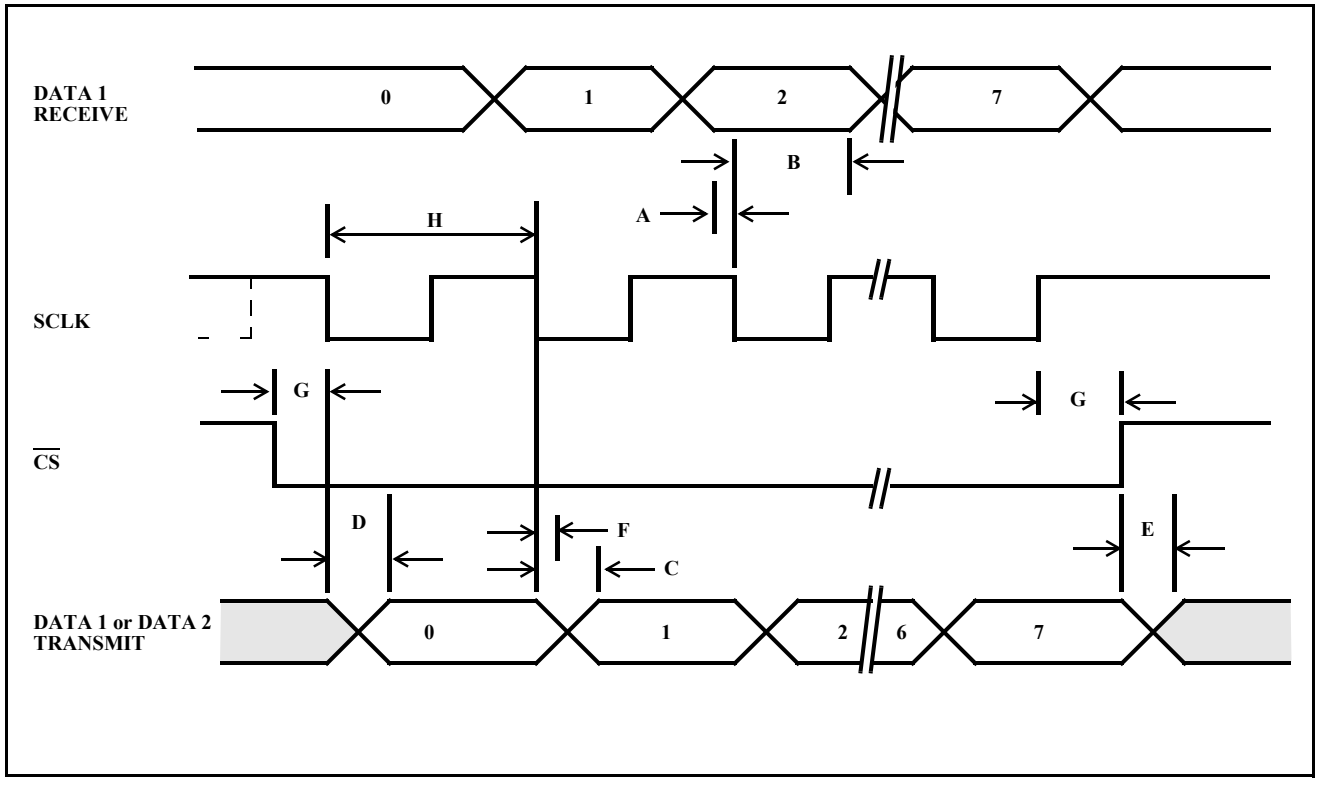
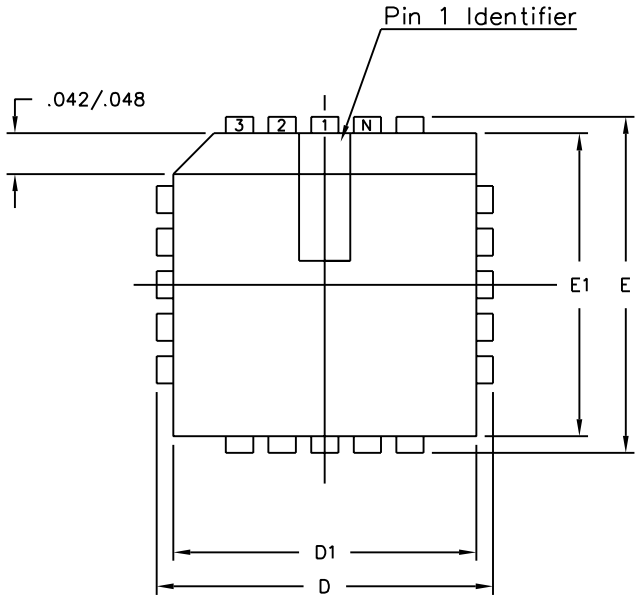
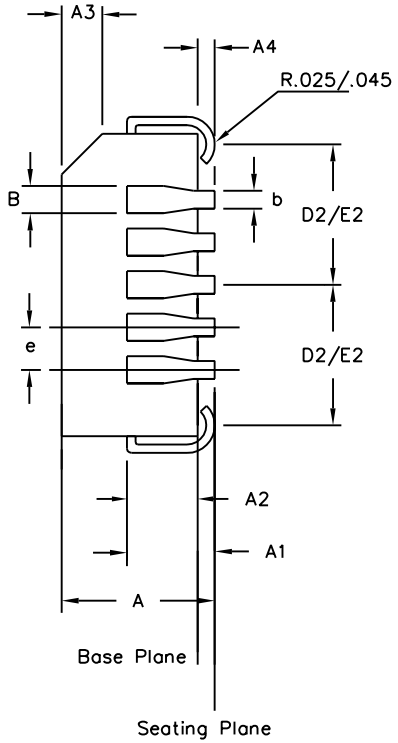


Figure 12 - Serial Microport Timing Diagram





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

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GPD00003

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