PAM8408

2x3W STEREO DIFFERENTIAL INPUT CLASS D AUDIO AMPLIFIER WITH MEMORY UP/DOWN VOLUME

NEW PRODUCT

Description

The PAM8408 is a filter-less Class-D amplifier with high SNR and differential input that helps eliminate noise. Advanced 32-step Up/Down volume control minimizes external components and allows speaker volume control. The gain will held when the chip is in shutdown mode.

The PAM8408 supports 2.5V to 6V operation make it idea for up to 4 cells alkaline battery applications.

Features like greater than 87% efficiency and small PCB area make the PAM8408 Class-D amplifier ideal for portable applications. The output uses a filter-less architecture minimizing the number of external components and PCB area whilst providing a high performance, simple and lower cost system.

The PAM8408 built in auto recovery SCP (short circuit protection) and thermal shutdown.

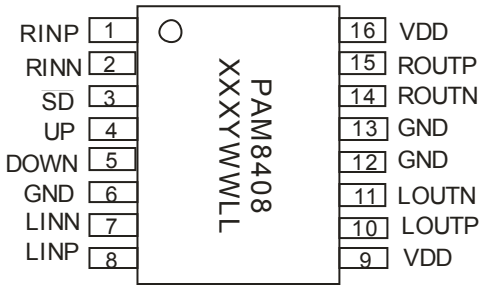
The PAM8408 is available in SO-16L package.

Features

- 3W Output at 10% THD with a 4Ω Load and 5V Supply
- 2.4W Output at 1% THD with a 4Ω Load and 5V Supply
- 2.5V to 6.0V VDD Operating
- Fully Differential Input
- Filter-less, Low Quiescent Current and Low EMI
- Low THD+N
- 32-Step Memory Up/Down Volume Control from -80dB to 24dB
- Superior Low Noise: 60uV
- Minimize Pop/Clip Noise
- Auto Recovery Short Circuit Protection
- Thermal Shutdown
- Pb-Free SO-16L Package

Pin Assignments

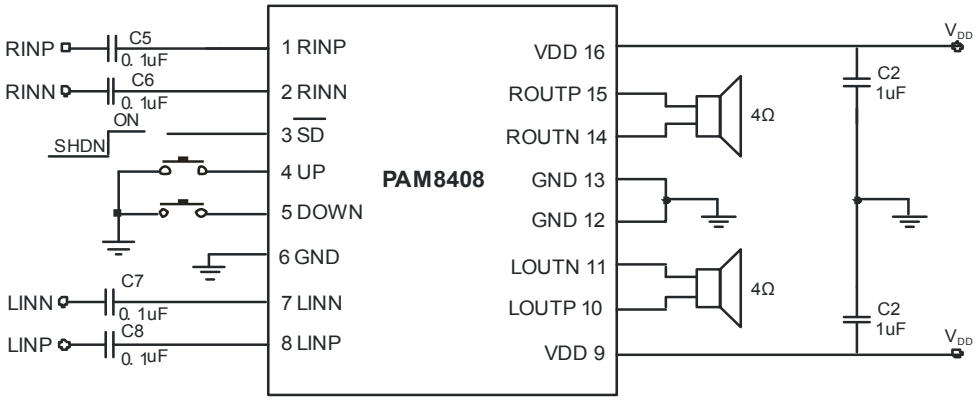
SO-16L



Applications

- PC Speaker
- Wireless Speaker
- Home Sound Systems
- Active Speakers
- Docking Stations

Typical Applications Circuit



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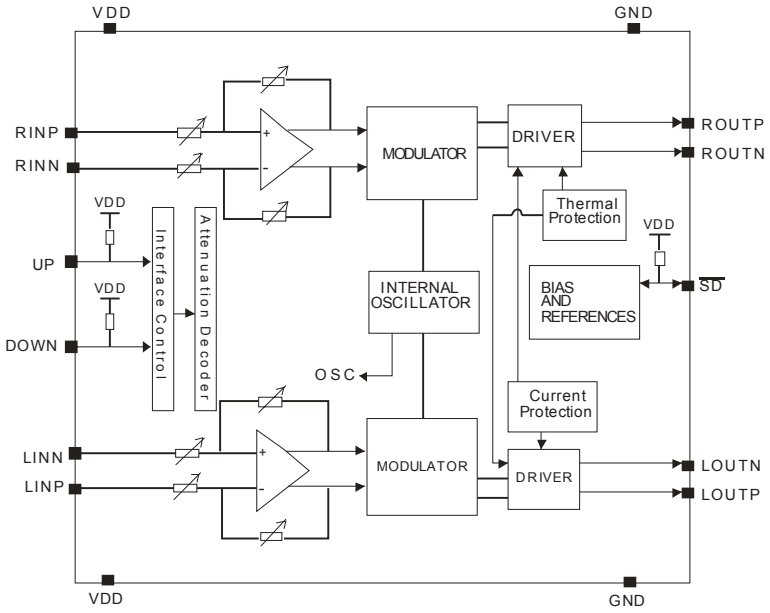
Pin Descriptions

Pin Number	Pin Name	Function
1	RINP	Positive Input of Right Channel Power Amplifier
2	RINN	Negative Input of Right Channel Power Amplifier
3	SD	Full Chip Shutdown Control Input (active low)
4	UP	Volume UP Control (active low)Ground Connection
5	DOWN	Volume down Control (active low)
6,12,13	GND	Ground
7	LINN	Negative Input of Left Channel Power Amplifier
8	LINP	Positive Input of Left Channel Power Amplifier
9,16	VDD	Power Supply
10	LOUTP	Positive Output of Left Channel Power Amplifier
11	LOUTN	Negative Output of Left Channel Power Amplifier
14	ROUTN	Negative Output of Right Channel Power Amplifier
15	ROUTP	Positive Output of Right Channel Power Amplifier

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage (VDD)	6.5	V
Pins Input Voltage (SD, UP, Down, IN)	-0.3 to V_{DD}+0.3	V
Storage Temperature	-65 to 150	°C
Maximum Junction Temperature	150	°C
Junction to ambient thermal resistance	40	°C/W

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Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	2.5	6.0	V
T_A	Operating Ambient Temperature Range	-40	85	°C
T_J	Junction Temperature Range	-40	125	°C

Electrical Characteristics (@T_A = +25°C, V_{DD} = 5V, Gain = 24dB, R_L = 8Ω (33μH)+R+L(33μH), unless otherwise noted.)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Voltage Range	V_{DD}			2.5		6.0	V
Quiescent Current	I_Q	No Load			8		mA
Output Offset Voltage	V_{OS}	No Load			10		mV
Drain-Source On-State Resistance	$R_{DS(ON)}$	I_{DS} = 0.5A	P MOSFET		0.3		Ω
			N MOSFET		0.2		
Output Power	P_O	THD+N = 1%, f = 1kHz	R_L= 8Ω		1.4		W
			R_L= 4Ω		2.4		
Total Harmonic Distortion Plus Noise	THD+N	R_L = 8Ω， P_O=0.85W,f=1KHz			0.08		%
		R_L = 4Ω， P_O=1.75W,f=1KHz			0.08		
Power Supply Ripple Rejection	PSRR	Input AC-GND, f=1KHz, Vpp=200mV			70		dB
Channel Separation	CS	P_O=1W, f=1KHz			-95		dB
Oscillator Frequency	f_{OSC}			200	250	300	kHz
Efficiency	η	P_O = 1.1W, f = 1kHz, R_L = 8Ω			87		%
		P_O = 2.4W, f = 1kHz, R_L = 4Ω			83		%
Noise	Vn	Input AC-GND	A-weighting		60		uV
			No A-weighting		80		
Signal Noise Ratio	SNR	F = 20 - 20kHz, THD = 1%			95		dB
Turn-on Time	Ton	VDD = 5V			0.65		S
Mute Current	I_{MUTE}	MUTE = VDD			4	10	mA
Shutdown Current	I_{SD}	V_{SD} = 0V				5	μA
Logic Input High	V_{IH}	Include SD,UP,DOWN		1.4			V
Logic Input Low	V_{IL}	Include SD,UP,DOWN				0.6	V
Over Temperature Protection	OTP				150		°C
Over Temperature Hysteresis	OTH				40		°C

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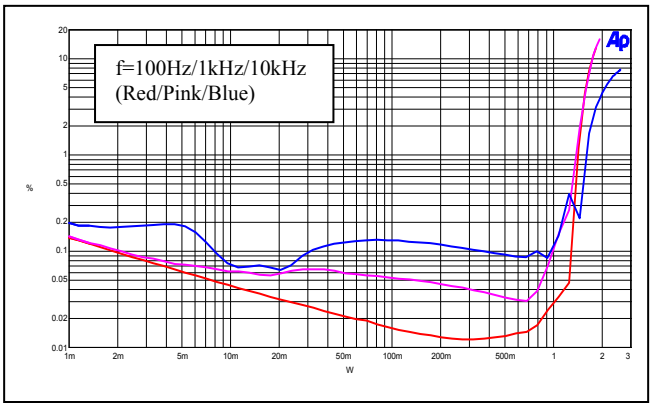
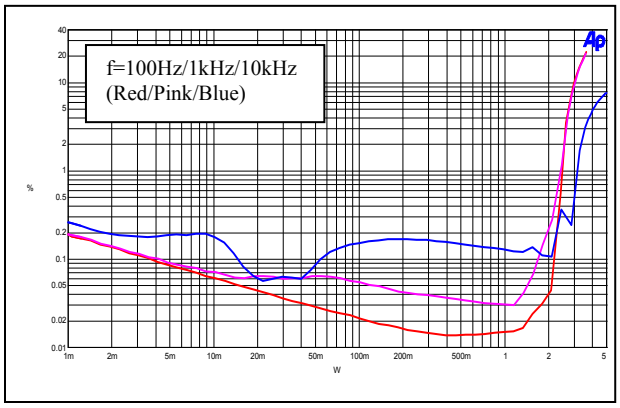
Performance Characteristics (@T_A = +25°C, V_{DD} = 5V, Gain = 24dB, R_L = 8Ω (33μH)+R+L(33μH), unless otherwise noted.)

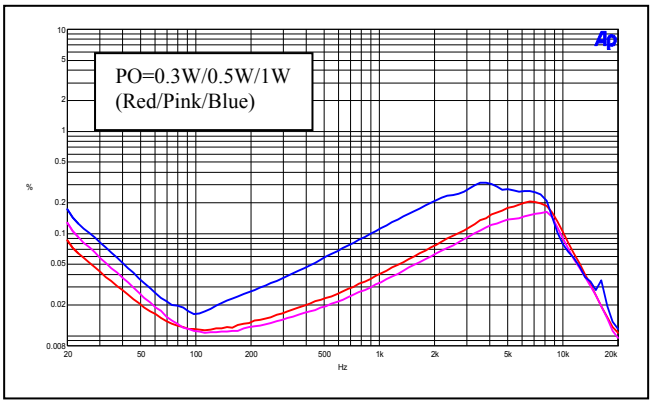
THD+N Vs. Output Power (RL=8Ω)



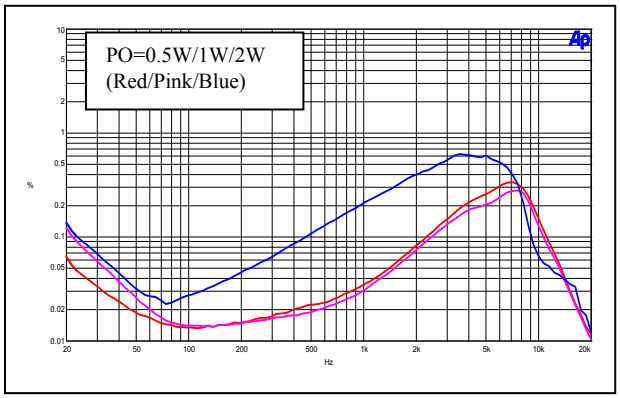
THD+N Vs. Output Power (RL=4Ω)



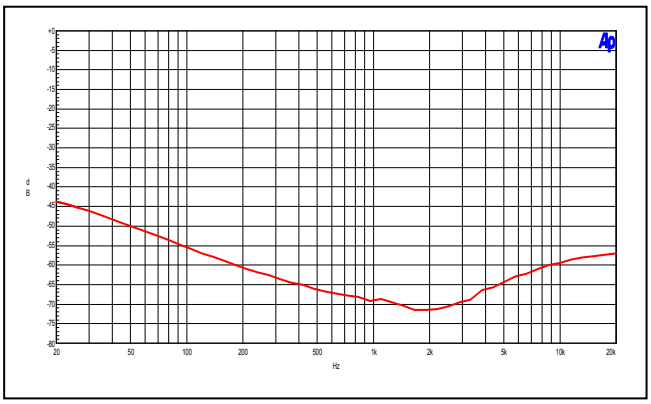
THD+N Vs. Frequency (RL=8Ω)



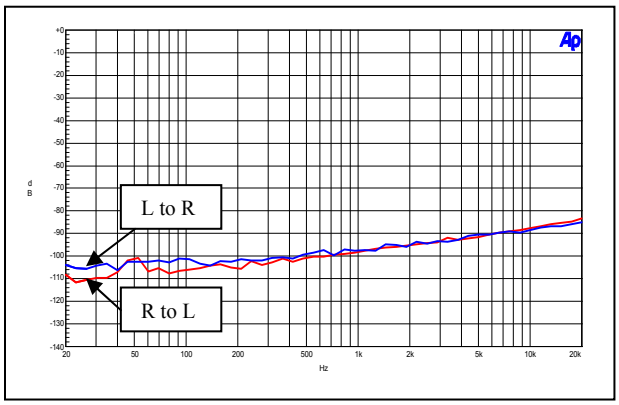
THD+N Vs. Frequency (RL=4Ω)



PSRR Vs. Frequency



Crosstalk Vs Frequency



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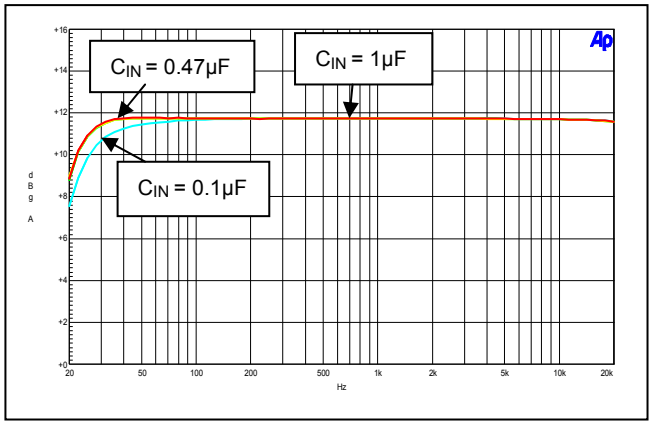
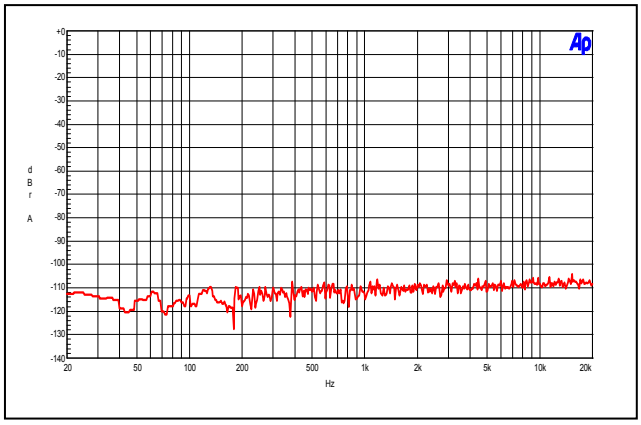
Performance Characteristics (cont.)

(@T_A = +25°C, V_{DD} = 5V, Gain = 24dB, R_L = 8Ω (33μH)+R+L(33μH), unless otherwise noted.)

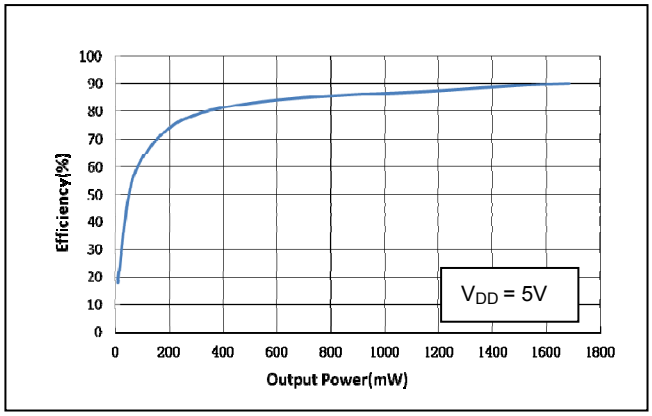
Frequency Response



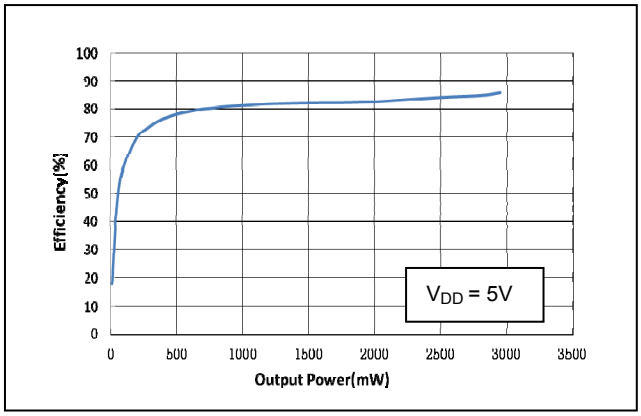
Noise Floor



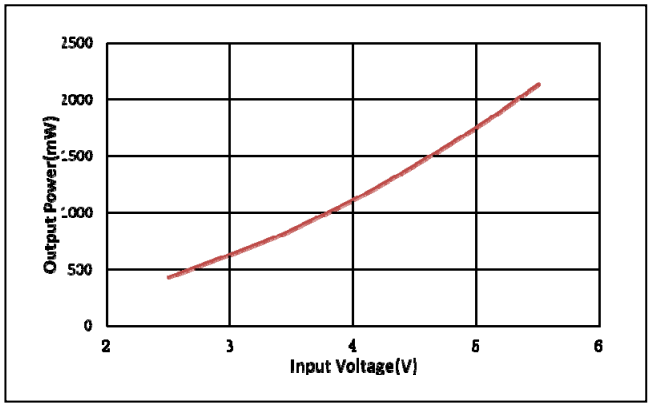
Efficiency vs. Output Power (RL = 8Ω)



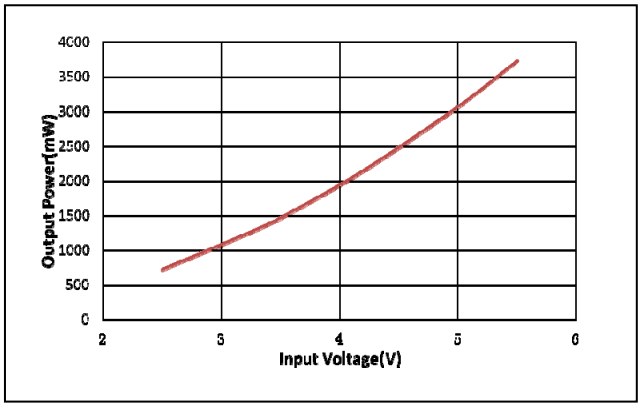
Efficiency vs. Output Power (RL = 4Ω)



Output Power vs. Supply Voltage (RL = 8Ω, THD = 10%)



Output Power vs. Supply Voltage (RL = 4Ω,THD = 10%)



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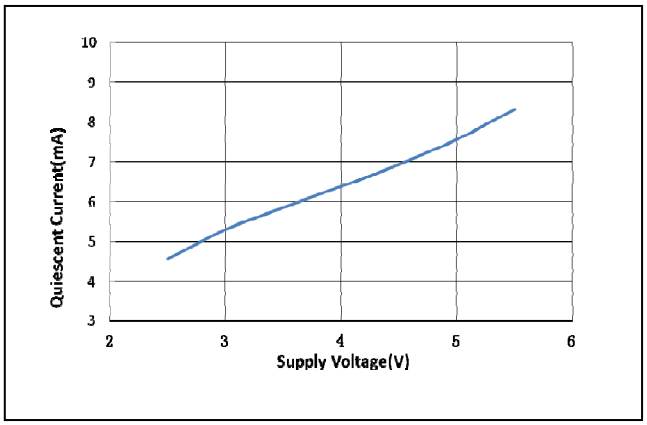
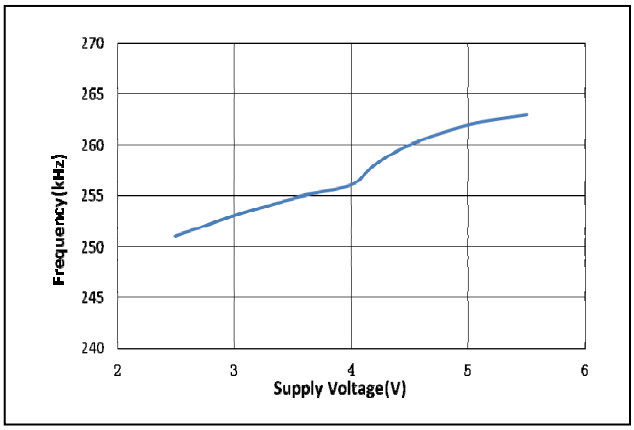
Performance Characteristics (cont.)

(@T_A = +25°C, V_{DD} = 5V, Gain = 24dB, R_L = 8Ω (33μH)+R+L(33μH), unless otherwise noted.)

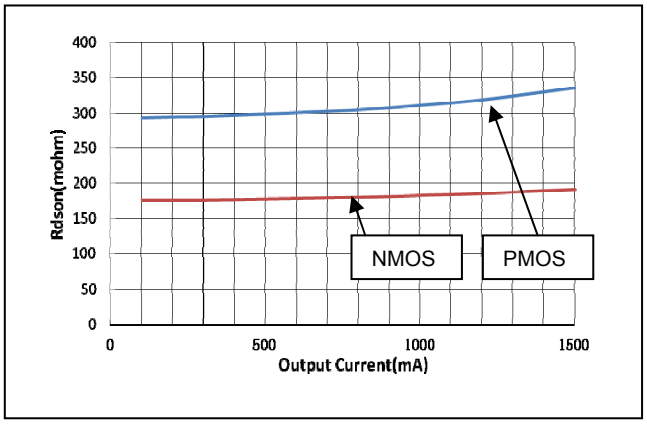
Quiescent Current vs. Supply Voltage



OSC Frequency vs. Supply Voltage



Rdson vs. Output Current



Up/Down Volume Control (dB)

STEP	Gain	STEP	Gain	STEP	Gain
1	24	12	7.5	23	-10
2	22.5	13	6	24	-12
3	21	14	4.5	25	-14
4	19.5	15	3	26	-16
5	18	16	1.5	27	-18
6	16.5	17	0	28	-20
7	15	18	-1.5	29	-22
8	13.5	19	-3	30	-24
9	12*	20	-4.5	31	-26
10	10.36	21	-6	32	-80
11	9	22	-8	-	-

*Default Gain = 12dB

NEW PRODUCT

Application Information

Maximum Gain

As shown in block diagram, the PAM8408 has two internal amplifiers stage. The first stage's gain is externally con-figurable, while the second stage's is internally fixed in a fixed-gain, inverting configuration. The closed-loop gain of the first stage is set by selecting the ratio of Rf to Ri while the second stage's gain is fixed at 2x. Consequently, the differential gain for the IC is

$$A_{VD}=20*\log [2*(Rf/Ri)]$$

The PAM8408 sets maximum Rf=218kΩ and minimum Ri=27kΩ, thus the maximum closed-gain is 24dB.

UP/DOWN Volume Control (DVC)

The PAM8408 features a UP/DOWN volume control which consists of the UP and DOWN pins. An internal clock is used where the clock frequency value is determined from the following formula:

$$f_{CLK} = f_{OSC} / 2^{13}$$

The oscillator frequency f_{OSC} value is 250kHz typical with ±20% tolerance. The DVC's clock frequency is 30Hz (cycle time 33ms) typical.

Volume changes are then effected by toggling either the UP or DOWN pins with a logic low. After a period of 1 cycle pulses with either the UP or DOWN pins held low, the volume will change to the next specified step, either UP or DOWN, and followed by a short delay. This delay decreases the longer the line is held low, eventually reaching a delay of zero. The delay allows the user to pull the UP or DOWN terminal low once for one volume change, or hold down to ramp several volume changes. The delay is optimally configured for push button volume control.

If either the UP or DOWN pin remains low after the first volume transition the volume will change again, but this time after 10 cycles. The followed transition occurs at 4 cycles for each volume transition. This is intended to provide the user with a volume control that pauses briefly after initial application, and then slowly increases the rate of volume change as it is continuously applied. This cycle is shown in the timing diagram shown in figure 1.

There are 32 discrete gain settings ranging from +24dB as maximum to -80dB as minimum. Upon device power on, the amplifier's gain is set to a default value of 12dB, and the gain will remain when applied a logic low to the SD pin, Volume levels for each step vary and are specified in Gain Setting table on page 7.

If both the UP and DOWN pins are held high, no volume change will occur. Trigger points for the UP and DOWN pins are at 70% of VDD minimum for a logic high, and 20% of VDD maximum for a logic low. It is recommended, however, to toggle UP and DOWN between VDD and GND for best performance.

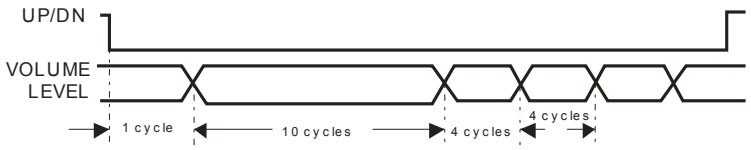


Figure 1 Timming Diagram

Shutdown Operation

In order to reduce power consumption while not in use, the PAM8408 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the SD pin. By switching the SD pin connected to GND, the PAM8408 supply current draw will be minimized in idle mode. The SD pin cannot be left floating due to the pull-down internal.

Power Supply decoupling

The PAM8408 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR are as low as possible. Power supply decoupling is affecting low frequency response. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0μF, placed as close as possible to the device VDD terminal works best. For filtering lower-frequency noise signals, a larger capacitor of 10μF (ceramic) or greater placed near the audio power amplifier is recommended.

NEW PRODUCT

Application Information (cont.)

Input Capacitor (Ci)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenu-ation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system perfor-mance. In this case, input capacitor (Ci) and input resistance (Ri) of the amplifier form a high-pass filter with the corner frequency determined equation below,

$$f_C = \frac{1}{2\pi R_i C_i}$$

In addition to system cost and size, click and pop perfor-mance is affected by the size of the input coupling capacitor, Ci. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 VDD). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Under Voltage Lock-Out (UVLO)

The PAM8408 incorporates circuitry designed to detect when the supply voltage is low. When the supply voltage drops to 2.4V or below, the PAM8408 outputs are disable, and the device comes out of this state and starts to normal functional when the supply voltage increases.

Short Circuit Protection (SCP)

The PAM8408 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output and output-to-GND short. When a short circuit is detected on the outputs, the outputs are disable immediately. If the short was removed, the device activates again.

Over Temperature Protection

Thermal protection on the PAM8408 prevents damage to the device when the internal die temperature exceeds 150°C. There is a 15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 60°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000μF at power supply terminal for power line coupling if the traces from amplifier to speakers are short (<20cm). Most applications require a ferrite bead filter which shows at Figure 3. The ferrite filter reduces EMI around 1 MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

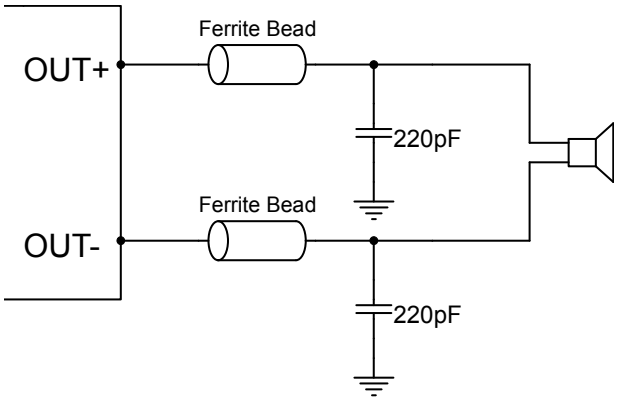


Figure 3 Ferrite Bead Filter to Reduce EMI

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Application Information (cont.)

PCB Layout Guidelines

Grounding

At this stage it is paramount that we acknowledge the need for separate grounds. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. Were these currents to circulate elsewhere, they may get into the power supply, the signal ground, etc, worse yet, they may form a loop and radiate noise. Any of these instances results in degraded amplifier performance. The logical returns for the output noise currents associated with Class D switching are the respective PGND pins for each channel. The switch state diagram illustrates that PGND is instrumental in nearly every switch state. This is the perfect point to which the output noise ground trace should return. Also note that output noise ground is channel specific. A two channels amplifier has two mutually exclusive channels and consequently must have two mutually exclusive output noise ground traces. The layout of the PAM8408 offers separate PGND connections for each channel and in some cases each side of the bridge. Output noise grounds must tie to system ground at the power in exclusively. Signal currents for the inputs, reference, etc need to be returned to quite ground. This ground only ties to the signal components and the GND pin. GND then ties to system ground.

Power Supply Line

As same to the ground, VDD and each channel PVDD need to be separated and tied together at the system power supply. Recommend that all the trace could be routed as short and thick as possible. For the power line layout, just imagine water stream, any barricade placed in the trace (shows in figure 4) could result in the bad performance of the amplifier.

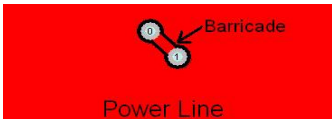
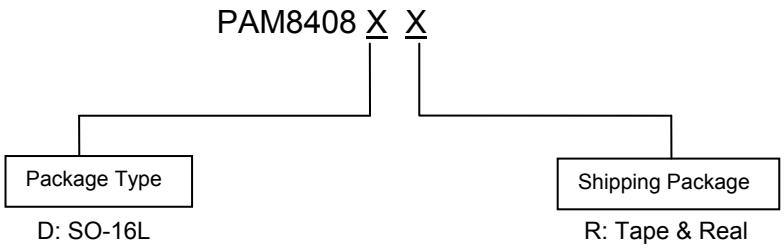


Figure 4

Components Placement

The power supply decoupling capacitors need to be placed as close to VDD pins as possible. The inputs need to be routed away from the noisy trace.

Ordering Information



Part Number	Package	Standard Package
PAM8408DR	SO-16L	2,500Units/Tape&Real

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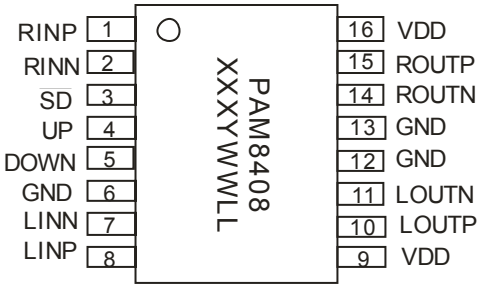
Marking Information



PAM8408: Product Code

X: Internal Code

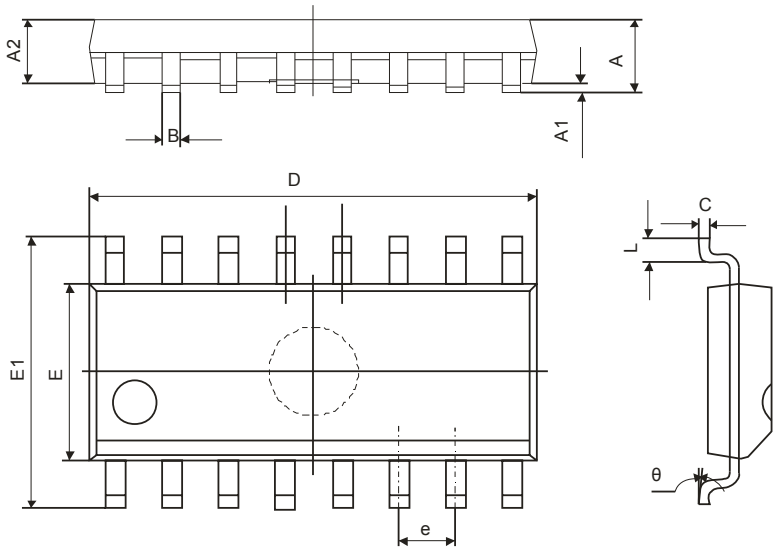
Y: Year

W: Week

LL: Internal Code

Package Outline Dimensions (All dimensions in mm.)

Package: SO-16L



Symbol	Dimensions Millimeters	
	Min	Max
A	-	1.260
A1	0.100	0.230
A2	1.020	-
B	0.310	0.510
C	0.100	0.250
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.200
e	1.270(TYP)	
L	0.400	1.270
θ	0°	8°

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