MOSFET - POWERTRENCH®, N-Channel

100 V, 240 A, 2.6 mΩ

FDBL86063

Features

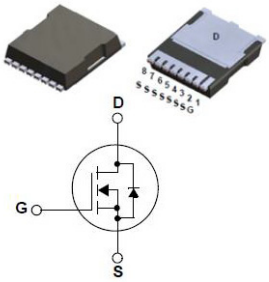
- Typical $R_{DS(on)}$ = 2 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 73 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- This Device is Pb−Free and is RoHS Compliant

Typical Applications

- Industrial Battery Switch
- Primary Switch for 12 V Systems

ON Semiconductor®

www.onsemi.com



H−PSOF8L 11.68x9.80
CASE 100CU

MARKING DIAGRAM

$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86063	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_J = 25°C, Unless otherwise noted)

Symbol	Parameter			Ratings	Units
V_{DSS}	Drain−to−Source Voltage			100	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Drain Current	−Continuous (V_{GS} = 10 V) (Note 1)	T_C = 25°C	240	A
		−Pulsed	T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy		(Note 2)	160	mJ
P_D	Power Dissipation			357	W
	Derate Above 25°C			2.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature			−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case			0.42	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient		(Note 3)	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 50 μH, I_{AS} = 80 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping†
FDBL86063	FDBL86063	H−PSOF8L 11.68x9.80 (Pb−Free)	2000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS						
B_{VDSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 100 V, V_{GS} = 0 V, T_J = 25°C			1	μA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 175°C (Note 4)			1.5	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	2.9	4.0	V
$R_{DS(on)}$	Drain−to−Source On−Resistance	I_D = 80 A, V_{GS} = 10 V, T_J = 25°C		2.0	2.6	mΩ
		I_D = 80 A, V_{GS} = 10 V, T_J = 175°C (Note 4)		4.2	5.6	
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		5120		pF
C_{oss}	Output Capacitance			3220		pF
C_{rss}	Reverse Transfer Capacitance			32		pF
R_g	Gate Resistance	V_{GS} = 0.5 V, f = 1 MHz		0.4		Ω
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 80 A		73	95	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 V to 2 V; V_{DD} = 50 V, I_D = 80 A		9		nC
Q_{gs}	Gate−to−Source Gate Charge	V_{DD} = 50 V, I_D = 80 A		22		nC
Q_{gd}	Gate−to−Drain “Miller” Charge	V_{DD} = 50 V, I_D = 80 A		17		nC
SWITCHING CHARACTERISTICS						
t_{on}	Turn−On Time	V_{DD} = 50 V, I_D = 80 A, V_{GS} = 10V, R_{GEN} = 6 Ω			53	ns
$t_{d(on)}$	Turn−On Delay			25		ns
t_r	Rise Time			16		ns
$t_{d(off)}$	Turn−Off Delay			32		ns
t_f	Fall Time			8		ns
t_{off}	Turn−Off Time				51	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source−to−Drain Diode Voltage	V_{GS} = 0 V, I_{SD} = 80 A V_{GS} = 0 V, I_{SD} = 40 A		0.9 0.8	1.25 1.2	V
t_{rr}	Reverse−Recovery Time	I_F = 80 A, $\Delta I_{SD}/\Delta t$ = 100 A/μs		107	139	ns
Q_{rr}	Reverse−Recovery Charge			175	260	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

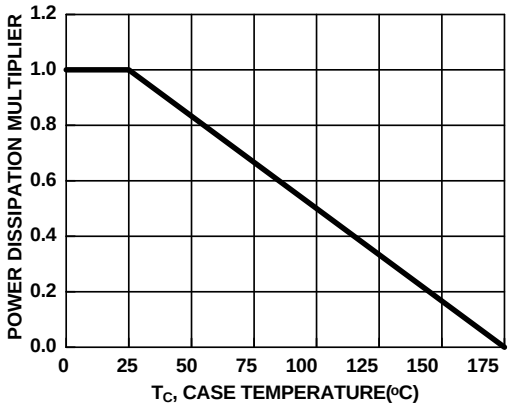


Figure 1. Normalized Power Dissipation vs. Case Temperature

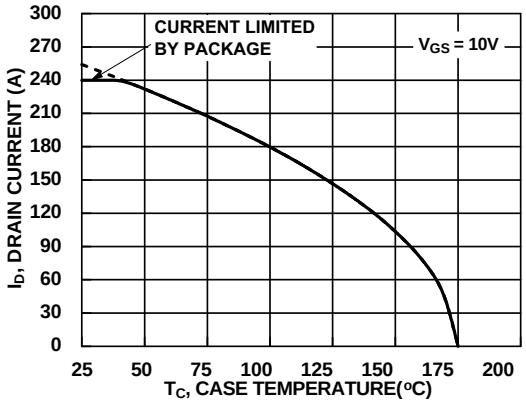


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

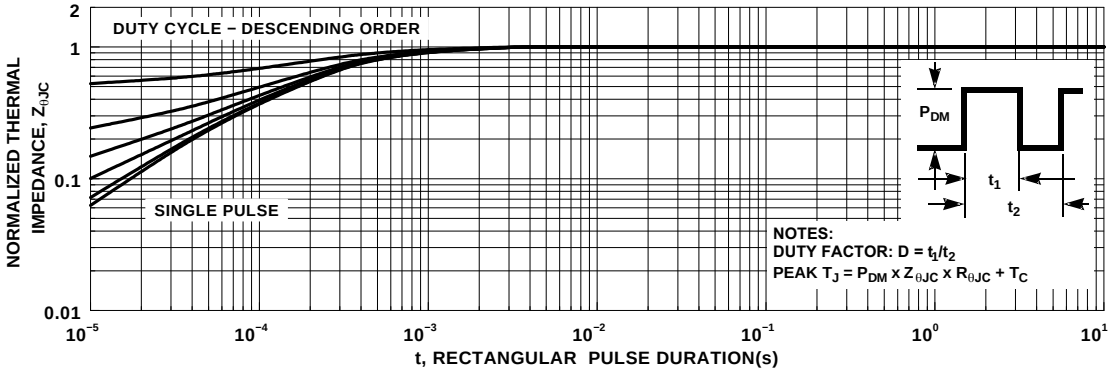


Figure 3. Normalized Maximum Transient Thermal Impedance

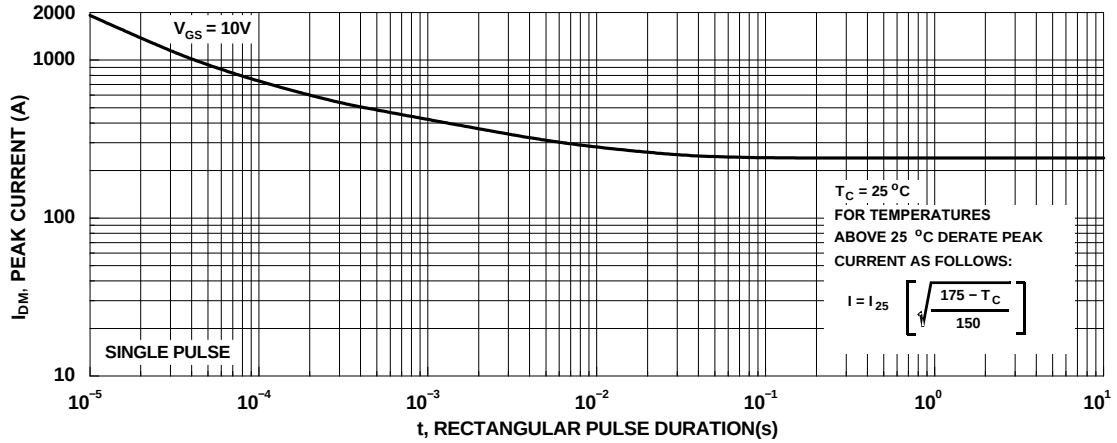


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

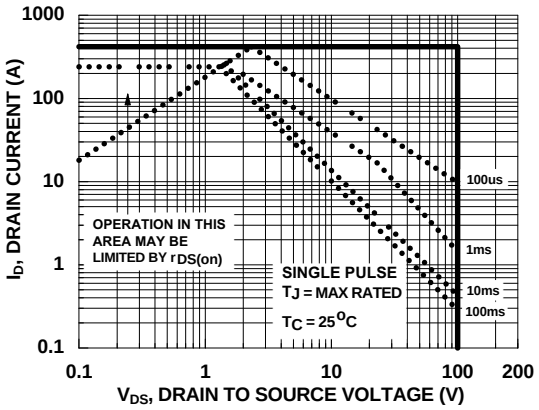
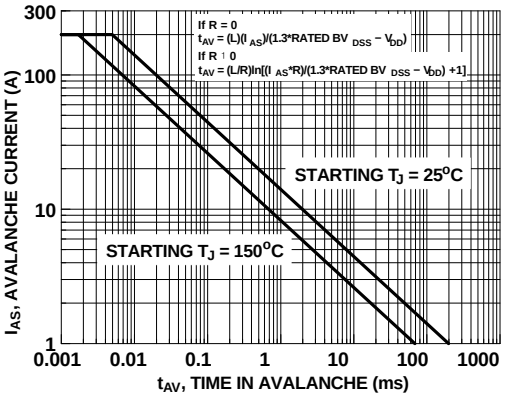


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

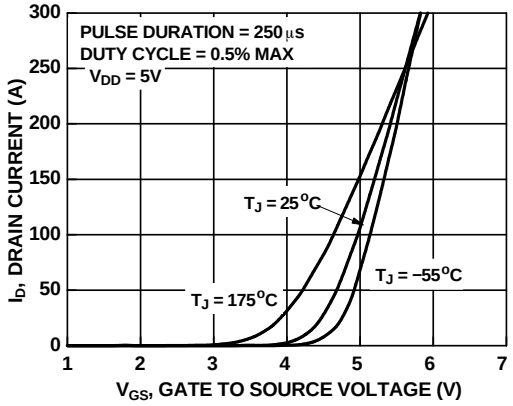


Figure 7. Transfer Characteristics

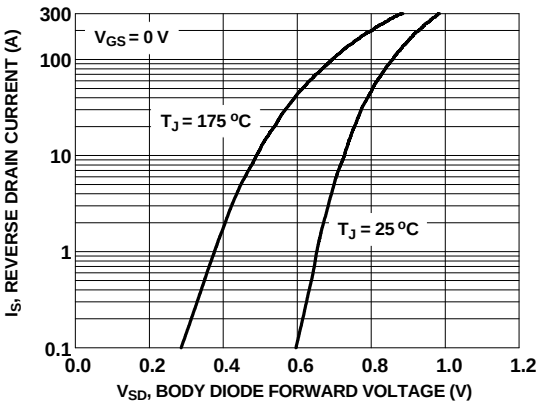


Figure 8. Forward Diode Characteristics

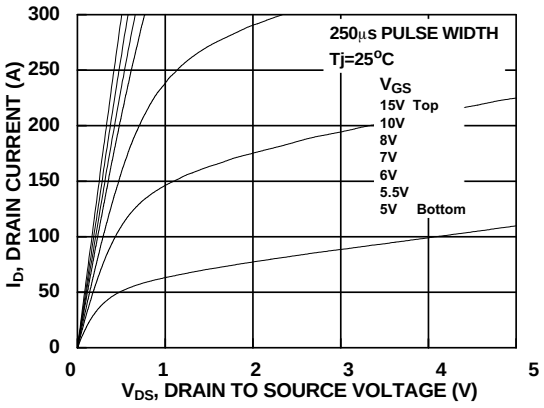


Figure 9. Saturation Characteristics

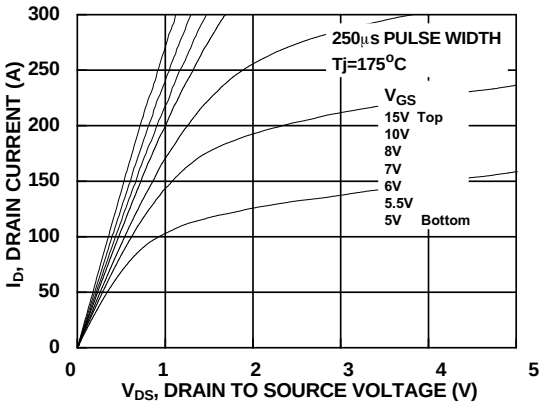


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

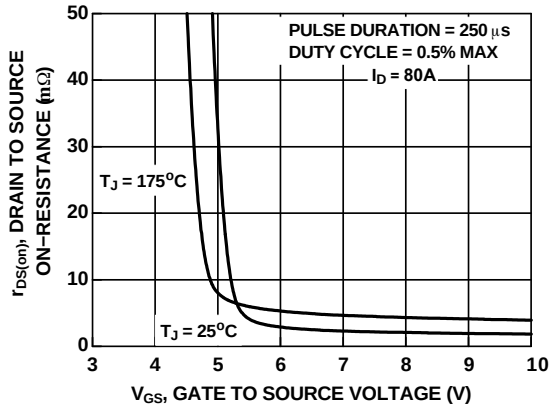


Figure 11. R_{DSON} vs. Gate Voltage

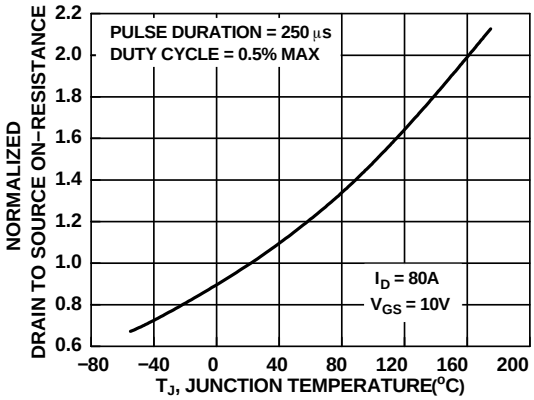


Figure 12. Normalized R_{DSON} vs. Junction Temperature

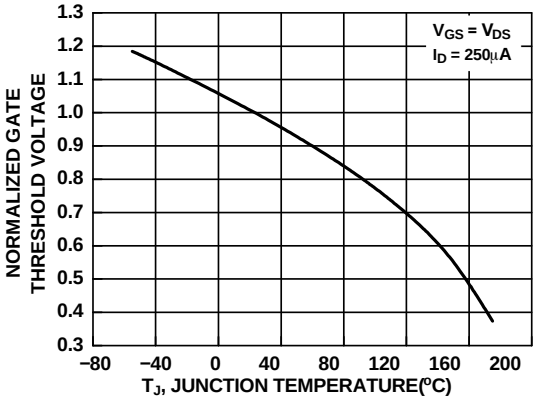


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

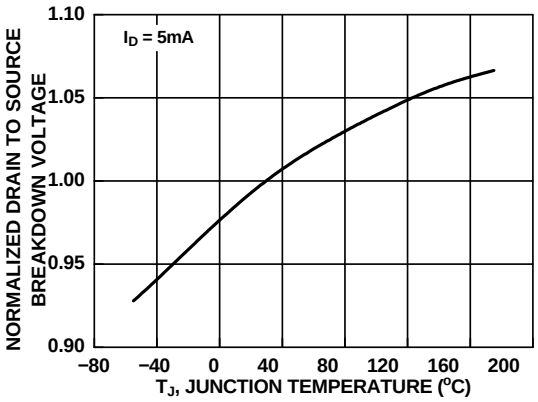


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

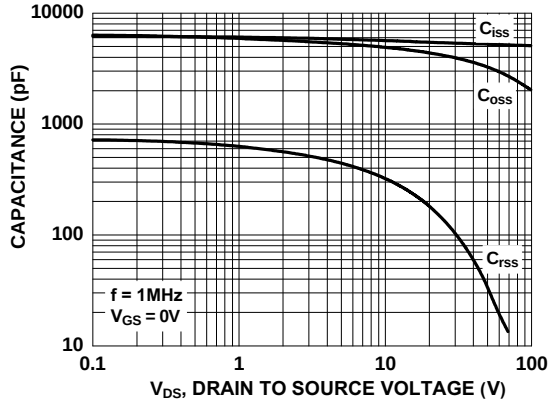


Figure 15. Capacitance vs. Drain to Source Voltage

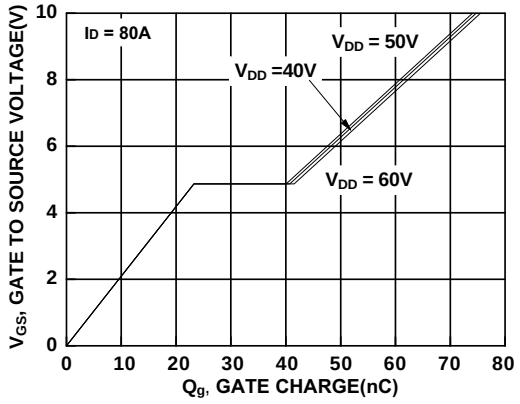
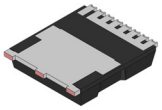


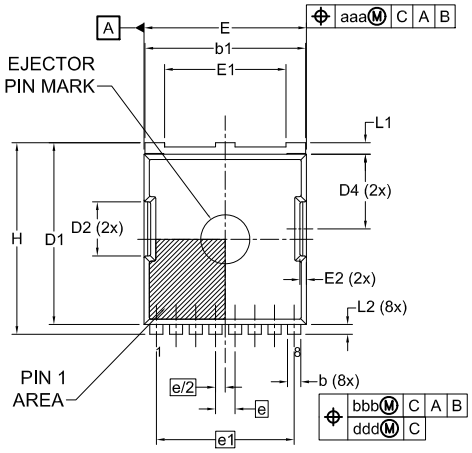
Figure 16. Gate Charge vs. Gate to Source Voltage

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

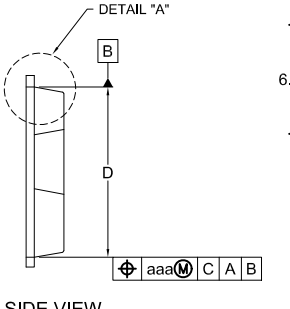


H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE C

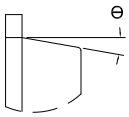
DATE 22 MAY 2023



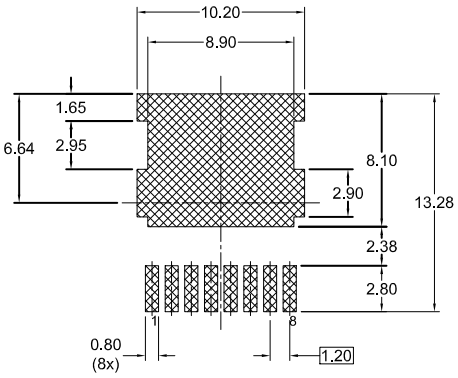
TOP VIEW



SIDE VIEW

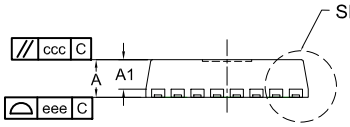


DETAIL "A"
SCALE: 2X

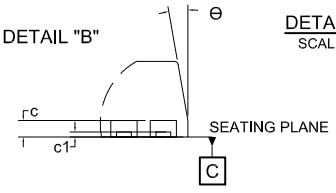


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



FRONT VIEW



DETAIL "B"
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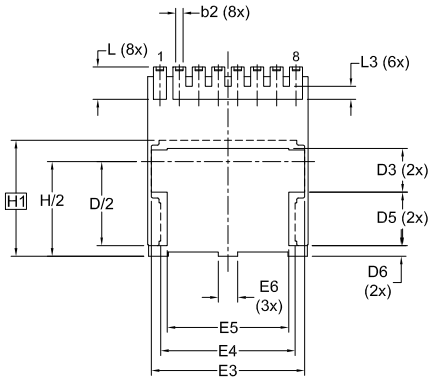


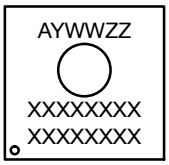
BOTTOM VIEW

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
c1	0.10	—	—
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	9.36	9.46	9.56

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E4	8.20	8.30	8.40
E5	7.40	7.50	7.60
E6	1.10	1.20	1.30
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	0°	—	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13813G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**H−PSOF8L 11.68x9.80**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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onsemi Website: www.onsemi.com

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