A product Line of
Diodes Incorporated

PI3PCIE2612-A

High Bandwidth, 6-Differential Channel 1:2 DP/PCIe Gen2 Display Mux, ATX Pinout

Features

- Six Differential Channel, One-to-Two Demux Supports 5.0Gbps PCI Express (PCIe) Gen2 Signals on one Path, and DP 1.1 Signals on the Second Path
- Insertion Loss for High-Speed Channels @ 5.0Gbps: -5.0dB
- Low Bit-to-Bit Skew , 7ps Maximum (Between + and - bits)
- Latched Mux Select
- Matched Paths for all PCIe Signals
- Low Crosstalk for High-Speed Channels: -35dB @ 2.5GHz
- Low Off Isolation for High-Speed Channels: -35dB @ 2.5GHz
- V_{DD} Operating Range: 3.3V ± 10%
- ESD Tolerance: 8kV HBM on Display Port Path Output 3kV HBM on PCIExpress Path Output
- Low Channel-to-Channel Skew, 35ps Maximum
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Packaging (Pb-free & Green):**
  - **56 TQFN (ZFE)**

Truth Table (SEL Control)

SEL	Function
L	PCI Express Gen2 path is active (Tx)
H	Digital Video Port is active (Dx)

Truth Table (Latch Control)

LE#	Internal Mux Select
0	Respond to changes on SEL
1	Latched

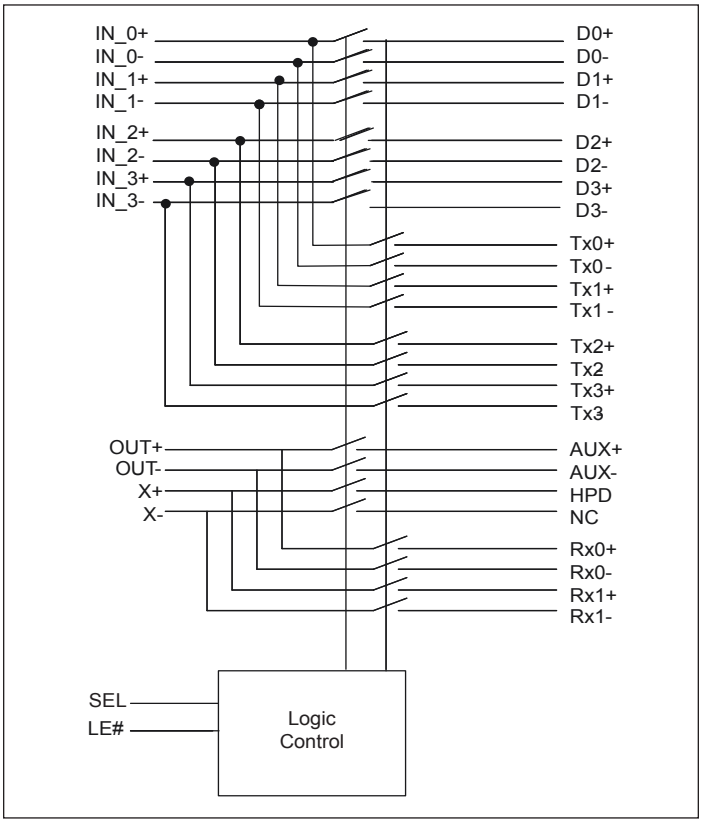
Description

Diodes' PI3PCIE2612-A one-to-two mux/demux is targeted for next generation systems that combine PCI Express Gen2 signals with display port signals.

Application

Routing DP and PCI Express Gen1 or Gen2 signals with low-signal attenuation.

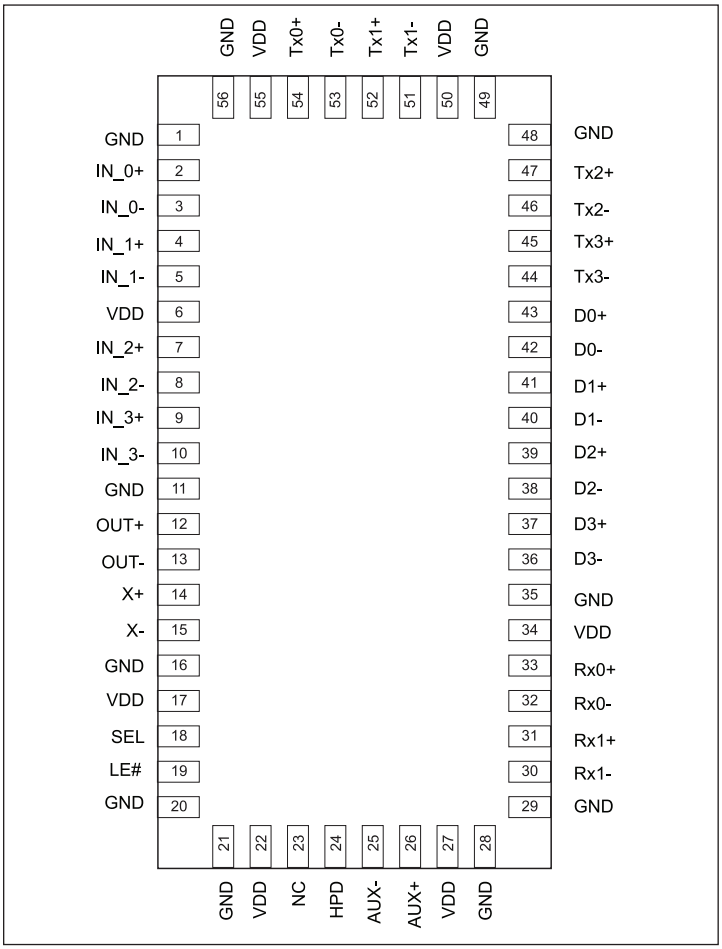
Block Diagram



Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Diagram (Top-Side View)



Pin Description

Pin Number	Pin Name	Type	Description
26	AUX+	O	Differential input from HDMI/DP connector. AUX+ makes a differential pair with AUX-. AUX+ is passed through to the OUT+ pin when SEL = 1.
25	AUX-	O	Differential input from HDMI/DP connector. AUX- makes a differential pair with AUX+. AUX- is passed through to the OUT- pin when SEL = 1.
43, 42	D0+, D0-	O	Analog *pass through* output#1 corresponding to IN_0+ and IN_0-, when SEL = 1.
41, 40	D1+, D1-	O	Analog *pass through* output#1 corresponding to IN_1+ and IN_1-, when SEL = 1.
39, 38	D2+, D2-	O	Analog *pass through* output#1 corresponding to IN_2+ and IN_2-, when SEL = 1.
37, 36	D3+, D3-	O	Analog *pass through* output#1 corresponding to IN_3+ and IN_3-, when SEL = 1.
1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	GND	Power	Power - Ground
24	HPD	I	The HPD signal comes from the HDMI or DP connector. This is a low-frequency 0V to 5V (HDMI) or 3.6V (DP) input signal at the connector. The HPD input at the mux is 3.6V max, so HDMI HPD must be shifted down from 5V before it is passed to the mux.

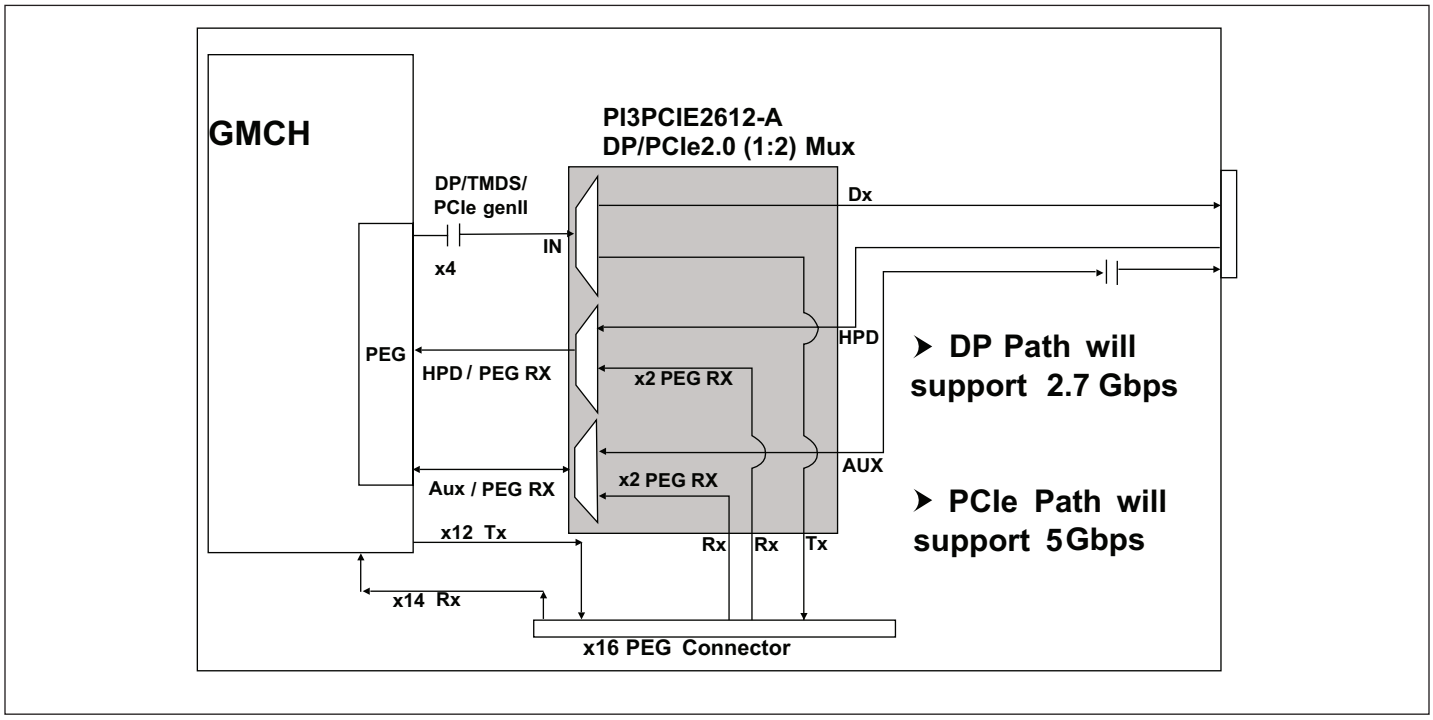
Pin Description Cont.

Pin Number	Pin Name	Type	Description
2	IN_0+	I	Differential input from GMCH PCIE outputs. IN_0+ makes a differential pair with IN_0-.
3	IN_0-	I	Differential input from GMCH PCIE outputs. IN_0- makes a differential pair with IN_0+.
4	IN_1+	I	Differential input from GMCH PCIE outputs. IN_1+ makes a differential pair with IN_1-.
5	IN_1-	I	Differential input from GMCH PCIE outputs. IN_1- makes a differential pair with IN_1+.
7	IN_2+	I	Differential input from GMCH PCIE outputs. IN_2+ makes a differential pair with IN_2-.
8	IN_2-	I	Differential input from GMCH PCIE outputs. IN_2- makes a differential pair with IN_2+.
9	IN_3+	I	Differential input from GMCH PCIE outputs. IN_3+ makes a differential pair with IN_3-.
10	IN_3-	I	Differential input from GMCH PCIE outputs. IN_3- makes a differential pair with IN_3+.
19	LE#	I	The latch gate is controlled by LE. 3.6V tolerant, low-voltage, single-ended input.
23	NC	NC	Do Not Connect
12	OUT+	O	Pass-through output from AUX+ input when SEL = 1. Pass-through output from Rx0+ input when SEL = 0.
13	OUT-	O	Pass-through output from AUX- input when SEL = 1. Pass-through output from Rx0- input when SEL = 0.
33	Rx0+	I/O	Differential input from PCIE connector or device. Rx0+ makes a differential pair with Rx0-. Rx0+ is passed through to the OUT+ pin when SEL = 0.
32	Rx0-	I/O	Differential input from PCIE connector or device. Rx0- makes a differential pair with Rx0+. Rx0- is passed through to the OUT- pin when SEL = 0.
31	Rx1+	I	Differential input from PCIE connector or device. Rx1+ makes a differential pair with Rx1-. Rx1+ is passed through to the X+ pin when SEL = 0.
30	Rx1-	I	Differential input from PCIE connector or device. Rx1- makes a differential pair with Rx1+. Rx1- is passed through to the X- pin on a path that matches the Rx1+ to X+ path.
18	SEL	I	SEL controls the mux through a flow-through latch. 3.6V tollerant low-voltage single-ended output SEL = 0 for PCIE Mode SEL = 1 for DP Mode
54, 53	Tx0+,Tx0-	O	Analog *pass through* output#2 corresponding to IN_0+ and IN_0-, when SEL = 0.
52, 51	Tx1+, Tx1-	O	Analog *pass through* output#2 corresponding to IN_1+ and IN_1-, when SEL = 0.
47, 46	Tx2+, Tx2-	O	Analog *pass through* output#2 corresponding to IN_2+ and IN_2-, when SEL = 0.
45, 44	Tx3+, Tx3-	O	Analog *pass through* output#2 corresponding to IN_3+ and IN_3-, when SEL = 0.
6, 17, 22, 27, 34, 50, 55	VDD	Power	3.3V DC Supply, 3.3V ±10%

Pin Description Cont.

Pin Number	Pin Name	Type	Description
14	X+	I/O	HPD: Low-frequency 0V to 5V/3.3V (nominal) input signal at the connector. This signal comes from the HDMI/DP connector. X+: Analog *pass through* output corresponding to Rx1+.
15	X-	I	X- is an analog *pass through* output corresponding to the Rx1- input. The path from Rx1- to X- must be matched with the path from Rx1+ to X+. X+ and X- form a differential pair when the pass-through mux mode is selected.

Application Diagram



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
DC Input Voltage	–0.5V to V_{DD}
DC Output Current	120mA
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	3.3V Power Supply	—	3.0	3.3	3.6	V
I_{DD}	Total Current from VDD 3.3V Supply	—	0	—	2.5	mA
T_{CASE}	Case Temperature Range for Operation Within Specification	—	-40	—	85	°C

DC Electrical Characteristics (T_A = –40°C to +85°C, V_{DD} = 3.3V ± 10%)

Parameter	Description	Test Conditions	Min	Typ(1)	Max	Units
$V_{IH\text{-}EN}$(2)	Input High Level	—	2.0	—	3.6	V
$V_{IL\text{-}EN}$(2)	Input Low Level	—	0	—	0.8	V
I_{IN_EN}(2)	Input Leakage Current	Measured with Input at VIH-EN Maximum and VIL-EN Minimum	–10	—	10	µA
R_{ON}	On Resistance	V_{DD} = Min., V_{IN} = 1.3V, I_{IN} = 40mA	—	—	10	Ω
C_{ON}	On Channel Capacitance	V_{IN} = 0, V_{DD} = 3.3V	—	3.0	—	pF

Note: 1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.
2. For SEL and LE# inputs.

Dynamic Electrical Characteristics for IN_x+/-, Rxy+/-, and Txy+/-

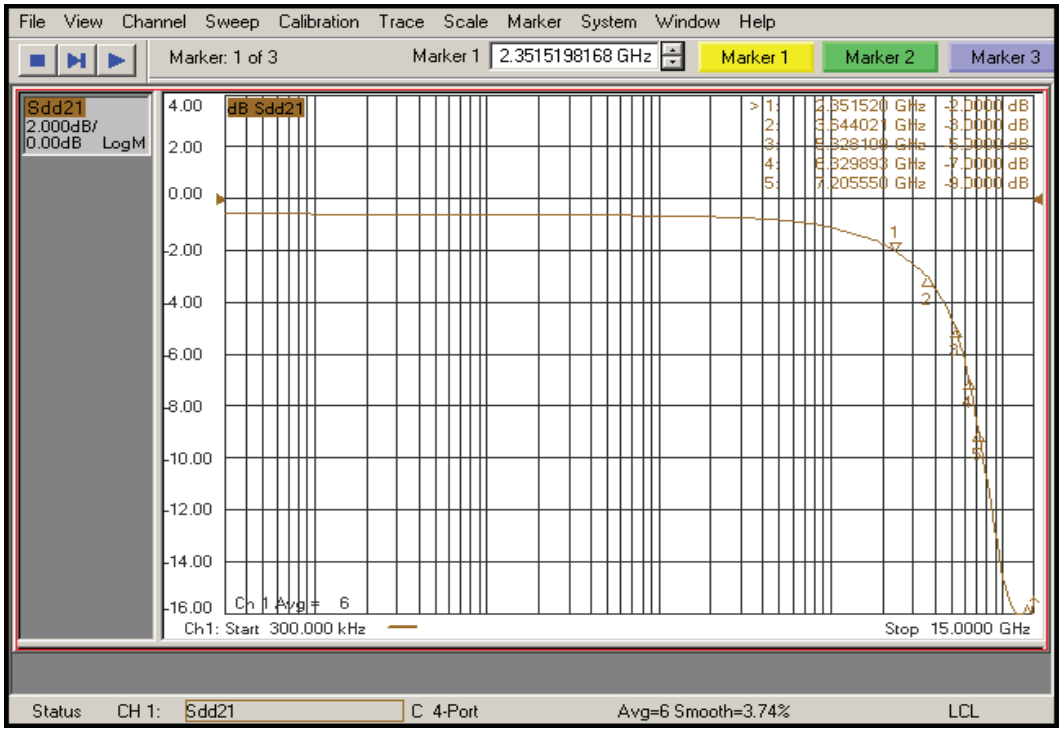
Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
DDIL	Differential Insertion Loss	f = 1.2GHz f = 2.5GHz f = 5.0GHz f = 7.5GHz	—	-1.5 -2.0 -5.0 -9.0	—	dB
$DDIL_{OFF}$	Differential Off Isolation	f = 0 to 3.0GHz f = 5.0GHz	—	-23.0 -20.0	—	
DDRL	Differential Return Loss	f = 0 to 2.8GHz f = 2.8GHz to 5.0GHz f = 5.0GHz to 7.5GHz	—	-14.0 -8.0 -4.0	—	
DDNEXT	Near End Crosstalk	f = 0 to 2.5GHz f = 2.5GHz to 5.0GHz f = 5.0GHz to 7.5GHz	—	-32.0 -26.0 -20.0	—	

Dynamic Electrical Characteristics for Dx+/-

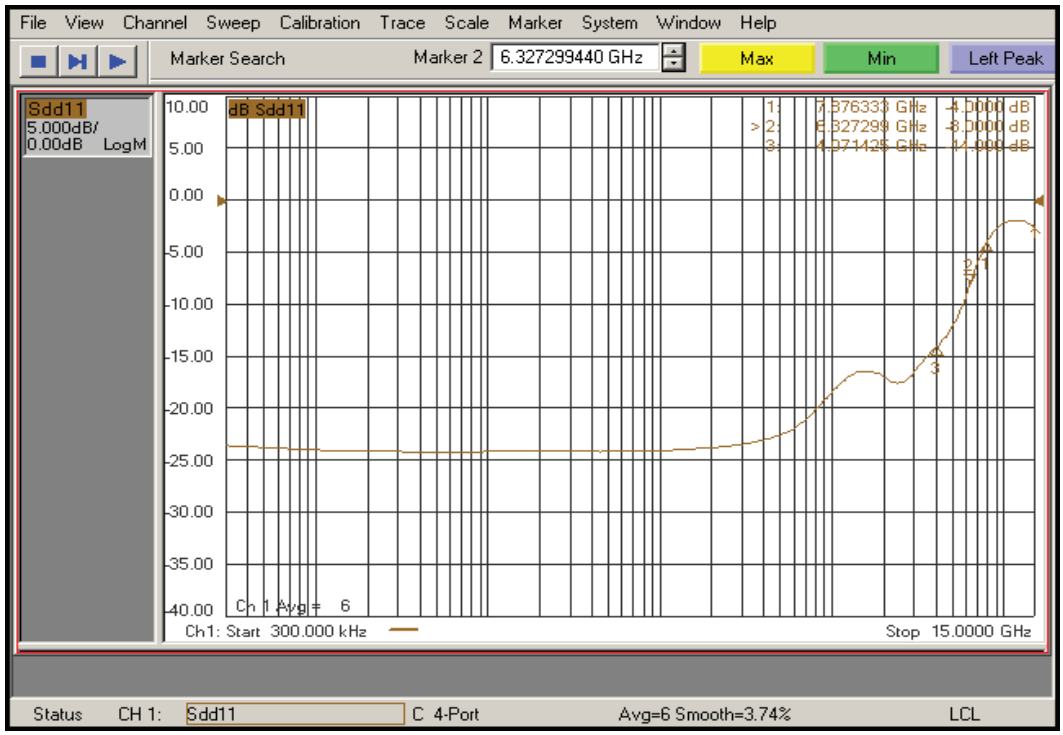
Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
$DDIL_{DP}$	Display Port Differential Insertion Loss	f = 0 to 1.35GHz f = 1.35GHz to 2.7GHz	—	-1.5 -4.5	—	dB
$DDRL_{DP}$	Display Port Differential Return Loss	f = 0 to 2.7GHz	—	-14	—	
$DDNEXT_{DP}$	Display Port Near End Crosstalk	f = 0 to 2.7GHz	—	-32.0	—	

Switching Characteristics (T_A= -40º to +85ºC, V_{DD} = 3.3V±10%)

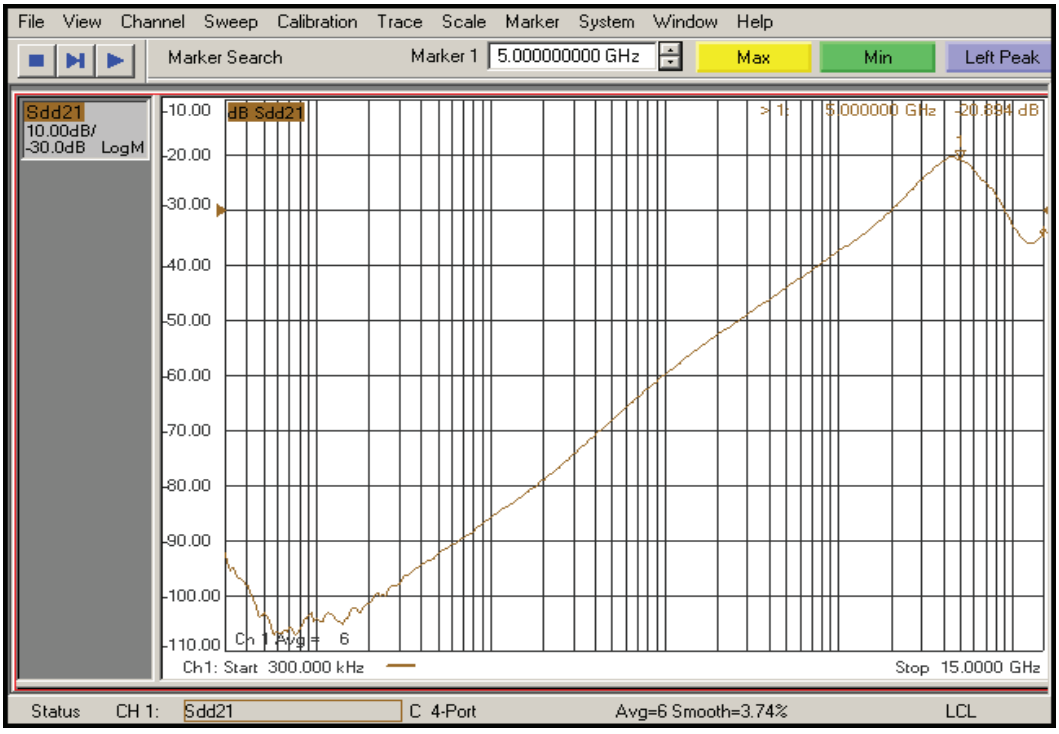
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time - SEL to D_X±, T_{XY}±, R_{XY}±, AUX±, HPD	See *Test Circuit for Electrical Chatacteristics*	0.5	—	12.0	ns
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to D_X±, T_{XY}±, R_{XY}±, AUX±, HPD	See *Test Circuit for Electrical Chatacteristics*	0.5	—	12.0	ns
$t_{b\text{-}b}$	Bit-to-Bit Skew Within the Same Differential Pair	See *Test Circuit for Electrical Chatacteristics*	—	—	7	ps
$t_{ch\text{-}ch}$	Channel-to-Channel skew	See *Test Circuit for Electrical Chatacteristics*	—	—	35	ps



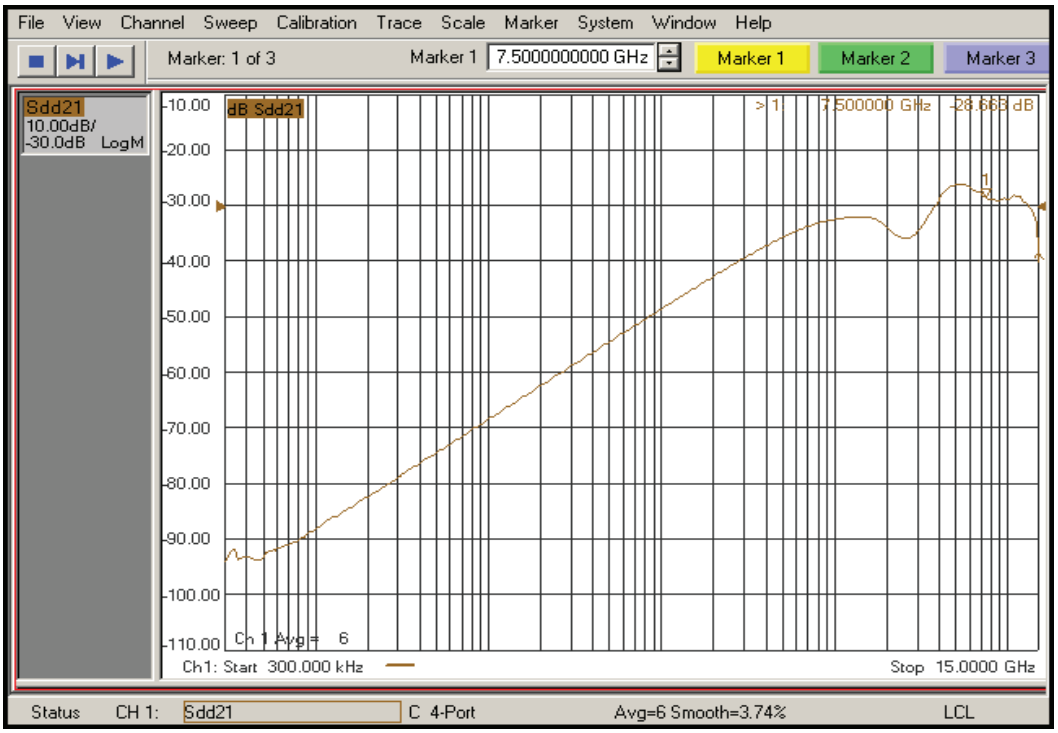
Differential Insertion Loss



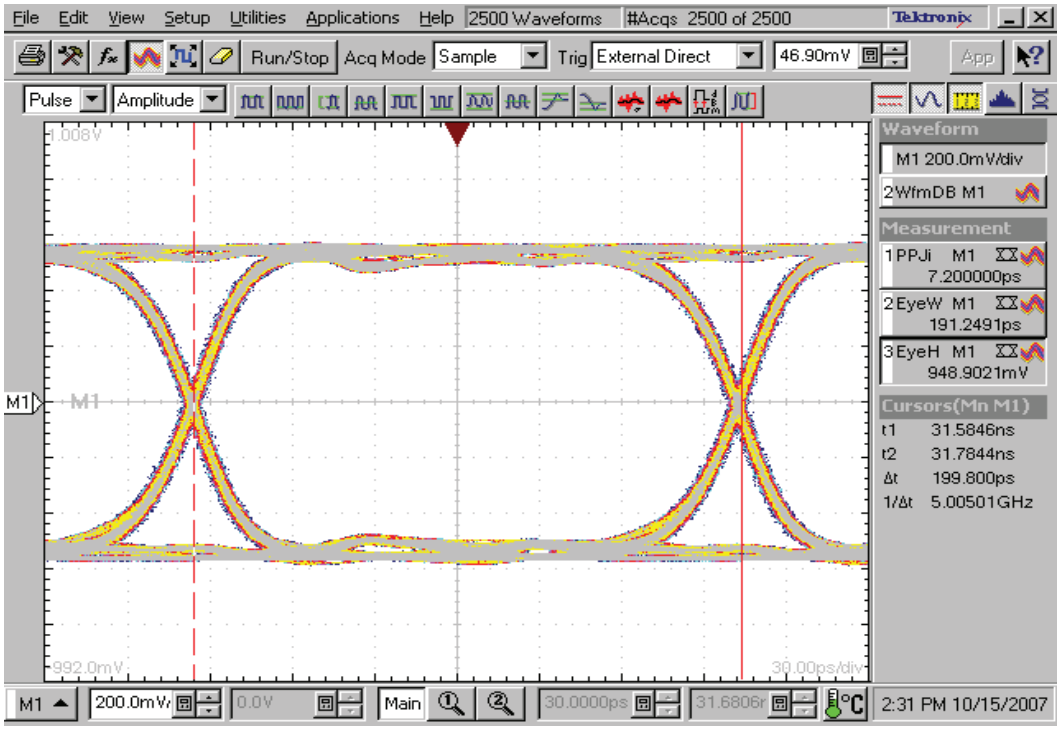
Differential Return Loss



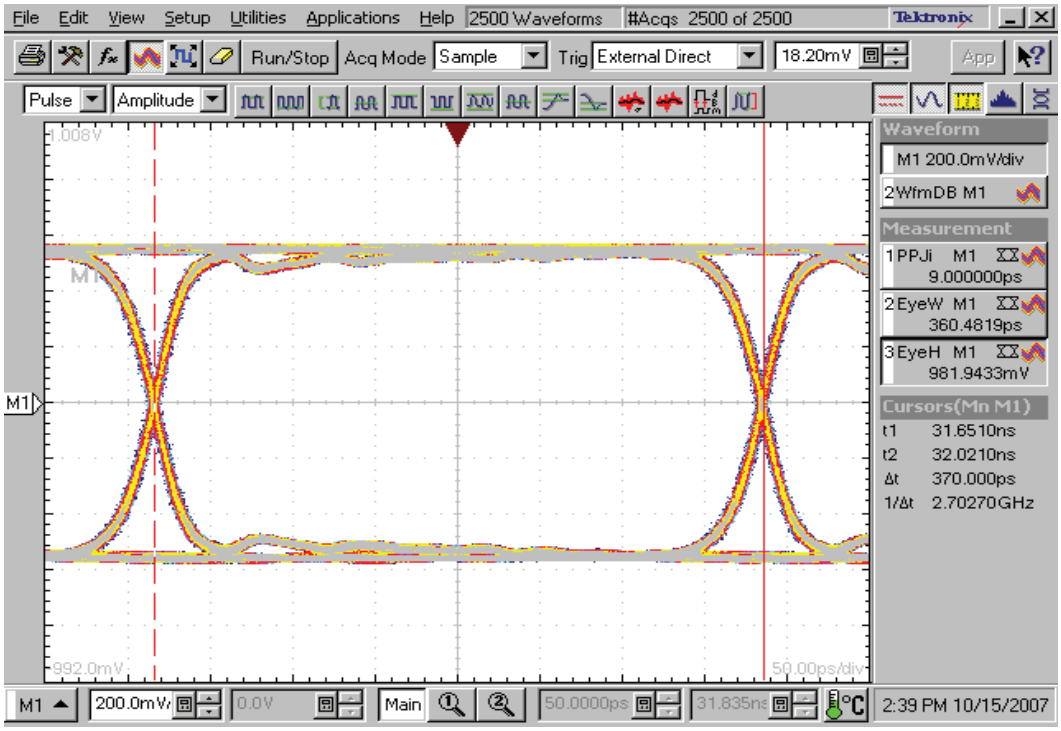
Off Isolation



Crosstalk

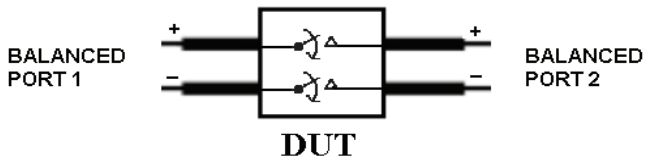


Tx Eye Diagram, 5.0Gbps

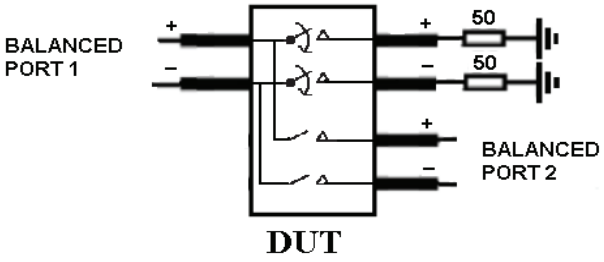


Dx Eye Diagram, 2.7Gbps

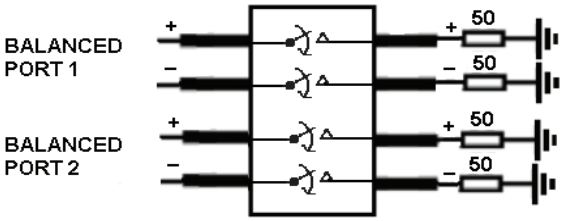
Differential Insertion Loss and Return Loss Test Circuit



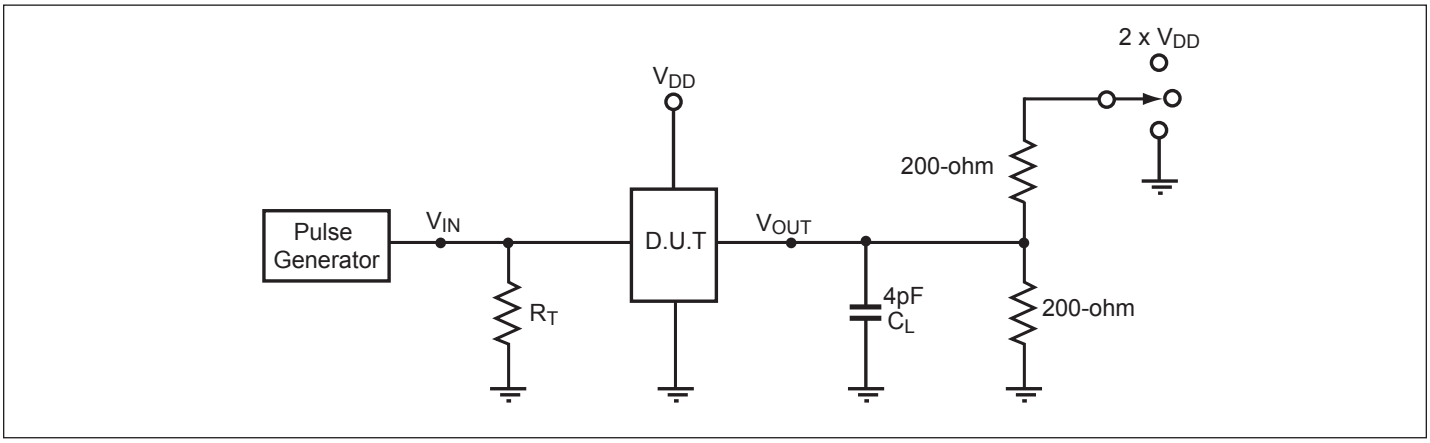
Differential Off Isolation Test Circuit



Differential Near End Crosstalk Test Circuit



Test Circuit for Electrical Characteristics(1-5)

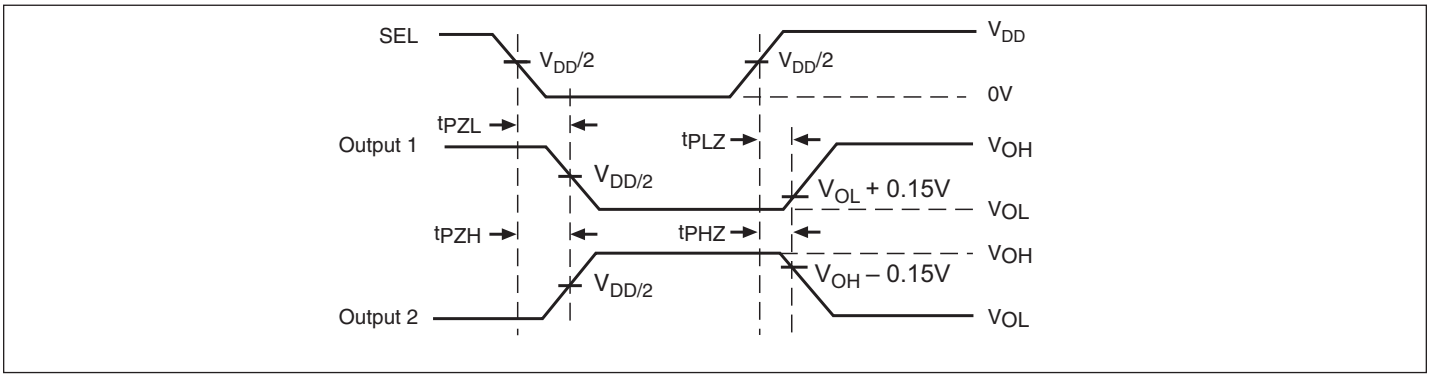


Notes:
1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.
5. The outputs are measured one at a time with one transition per measurement.

Switch Positions

Test	Switch
t_{PLZ}, t_{PZL}	2 × V_{DD}
t_{PHZ}, t_{PZH}	GND
Prop Delay	Open

Switching Waveforms



Voltage Waveforms Enable and Disable Times

Applications Information

Differential Input Characteristics for IN_x+/- and Rxx+/- signals

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	199.94	200.00	200.06	Ps	Defined by Gen2 Specification
$V_{RX-Diffp-p}$	Differential Input Peak to Peak Voltage	0.175	—	1.200	V	VRX-DIFFp-p = 2 × |VRX-D+ - VRX-D-| Applies to IN_D and RX_IN signals.
T_{RX-EYE}	Minimum Eye Width at IN_D Input Pair	TBD	—	—	Tbit	—
$V_{CM-AC-pp}$	AC Peak Common-Mode Input Voltage	—	—	100	mV	VCM-AC-pp = |VRX-D+ + VRX-D-| / 2 – VRX-CM-DC; VRX-CM-DC = DC(avg) of |VRX-D++ VRX-D-| / 2 VCM-AC-pp includes all frequencies above 30kHz.
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	W	Rx DC Differential Mode Impedance
Z_{RX-DC}	DC Input Impedance	40	50	60	W	Required IN_D+ as well as IN_D- DC impedance (50 W ±20% tolerance). Includes mux resistance.
$V_{RX-Bias}$	Rx Input Termination Voltage	0	—	2.0	V	Intended to limit power-up stress on PCIe output buffers.
DDIL	Differential Insertion Loss	≥-[0.6 × (f) + 0.5]dB up to 2.5GHz (for example, ≥ -2dB at f = 2.5GHz); ≥-[1.2 × (f-2.5) + 2]dB for 2.5GHz < f ≤ 5GHz (for example, ≥ -5dB at f = 5GHz); ≥-[1.6 × (f-5) + 5]dB for 5GHz < f ≤ 7.5GHz (for example, ≥ -9dB at f = 7.5GHz);			dB	—
DDRL	Differential Return Loss	≤ -14dB up to 2.8GHz; ≤ -8dB up to 5GHz; ≤ -4dB up to 7.5GHz.			dB	—
DDNEXT	Near End Crosstalk	-32dB max up to 2.5GHz; -26dB max up to 5.0GHz; -20dB max up to 7.5GHz;			dB	—
DDIL when Switch is off	Differential Insertion Loss when Switch is off	≤ -20dB up to 3GHz;			dB	—

PCIe Gen2 Output Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	W	Rx DC Differential Mode Impedance
Z_{RX-DC}	DC Input Impedance	40	50	60	W	Required IN_D+ as well as IN_D- DC impedance (50W ±20% tolerance). Includes mux resistance.
$V_{RX-Bias}$	Rx Input Termination Voltage	0	—	2.0	V	Intended to limit power-up stress on PCIe output buffers.
DDIL	Differential Insertion Loss	≥-[0.6 × (f) + 0.5]dB up to 2.5GHz (for example, ≥ -2dB at f = 2.5GHz); ≥-[1.2 × (f - 2.5) + 2]dB for 2.5GHz < f ≤ 5GHz (for example, ≥ -5dB at f = 5GHz); ≥-[1.6 × (f - 5) + 5]dB for 5GHz < f ≤ 7.5GHz (for example, ≥ -9dB at f = 7.5GHz)			dB	—
DDRL	Differential Return Loss	≤ -14dB up to 2.8GHz; ≤ -8dB up to 5GHz; ≤ -4dB up to 7.5GHz			dB	—
DDNEXT	Near End Crosstalk	-32dB max up to 2.5GHz; -26dB max up to 5.0GHz; -20dB max up to 7.5GHz			dB	—
DDIL when Switch is off	Differential Insertion Loss when Switch is off	≤ -20dB up to 3GHz			dB	—

Display Port Output Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	333	—	—	ps	Normal Tbit at 2.7Gb/s = 370ps; 333ps = 370ps - 10%
$V_{RX-Diffp-p}$	Differential Input Peak-to-Peak Voltage	0.340	—	1.38	V	VRX-DIFFp-p = 2 × |VRX-D+ - VRX-D-|; Applies to IN_D and RX_IN signals.
T_{JIT}	Jitter Added to High-Speed Signals	—	—	7.4	ps	Jitter budget for high-speed signals as they pass through the display mux. 7.4ps = 0.02 Tbit at 2.7Gb/s
DDIL	Differential Insertion Loss	≥-[0.75 × (f) + 0.5]dB up to 1.35GHz; ≥-[2.2 × (f - 1.35) + 1.5]dB for 1.35GHz < f ≤ 2.7GHz			dB	For example, ≥-1.5dB at f = 1.35GHz For example, ≥-4.5dB at f = 2.7GHz
DDRL	Differential Return Loss	≤ -14dB up to 2.7GHz			dB	—
DDNEXT	Near End Crosstalk	-32dB max up to 2.7GHz			dB	—

HPD Input Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{IH-HPD}	Input High Level	—	—	3.6	V	Low-speed input changes state on cable plug/unplug.
V_{IL-HPD}	HPD Input Low Level	0	—	—	—	V
I_{IN_HPD}	HPD Input Leakage Current	—	—	|10|	µA	Measured with HPD at VIH-HPD maximum and VIL-HPD minimum.
T_{HPD}	HPD_IN to HPD Propagation Delay	—	—	200	ns	Time from HPD_IN changing state to HPD changing state. Includes HPD rise/fall time.
T_{RF-HPD}	HPD Rise/Fall Time	1	—	20	ns	Time required to transition from VOH-HPD to VOL-HPD or from VOL-HPD to VOH-HPD.

Termination Resistors

Symbol	Parameter	Min	Nom	Max	Units	Comments
R_{DDC}	DDC Termination Resistors	1.3K	1.5k	2.2k	W	Applies to both 3.3V and 5V pull up resistors.

Switch Signal Integrity Requirements and Test Procedures for 5.0 Gb/s

Signal integrity requirements for 5.0Gb/s applications of the switch are specified. Also included are the requirements of the test fixture for switch S-parameter measurements.

Signal Integrity Requirements

The procedures outlined in ANSI Electronics Industry Alliance (EIA) standards documents must be followed:

- EIA 364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- EIA 364-90 – Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- EIA 364-108 – Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems

Signal Integrity Requirements and Test Procedures for 5.0Gb/s

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to a 100Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 1.12. 3. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.	≥-[0.6 × (f) + 0.5]dB up to 2.5GHz (for example, ≥ -2dB at f = 2.5GHz); ≥-[1.2 × (f-2.5) + 2]dB for 2.5GHz < f ≤ 5GHz (for example, ≥ -5dB at f = 5GHz); ≥-[1.6 × (f-5) + 5]dB for 5GHz < f ≤ 7.5GHz (for example, ≥ -9dB at f = 7.5GHz); Refer to Figure 1.
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to a 100Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 1.12. 3. The test fixture effect shall be removed. Refer to Note 1.	≤ -14dB up to 2.8GHz ≤ -8dB up to 5GHz ≤ -4dB up to 7.5GHz Refer to Figure 2.
Intrapair Skew	Intrapair skew must be achieved by design; measurement not required.	5ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs	-32 dB max up to 2.5 GHz -26 dB max up to 5.0 GHz -20 dB max up to 7.5 GHz See Figure 3.
Differential Insertion Loss (DDIL) when switch is turned off	EIA 364-101	≤ -20dB up to 3GHz

Notes: 1. The specified S parameters requirements are for switch component only, not including the test fixture effect. While the TRL calibratio method is recommended, other calibration methods are allowed.

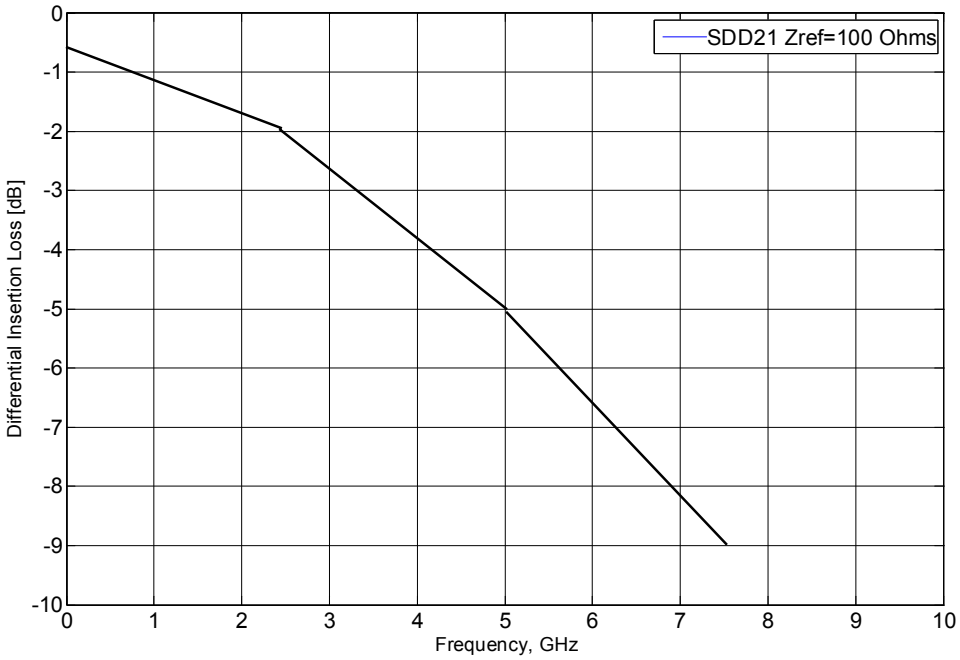


Figure 1: Illustration of differential insertion loss requirement.

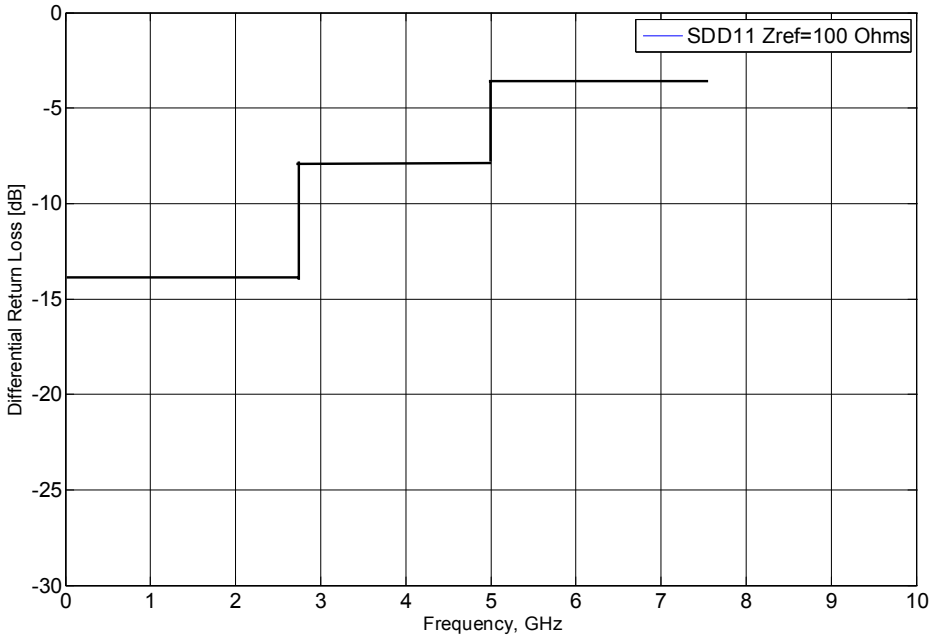


Figure 2: Illustration of differential return loss requirement.

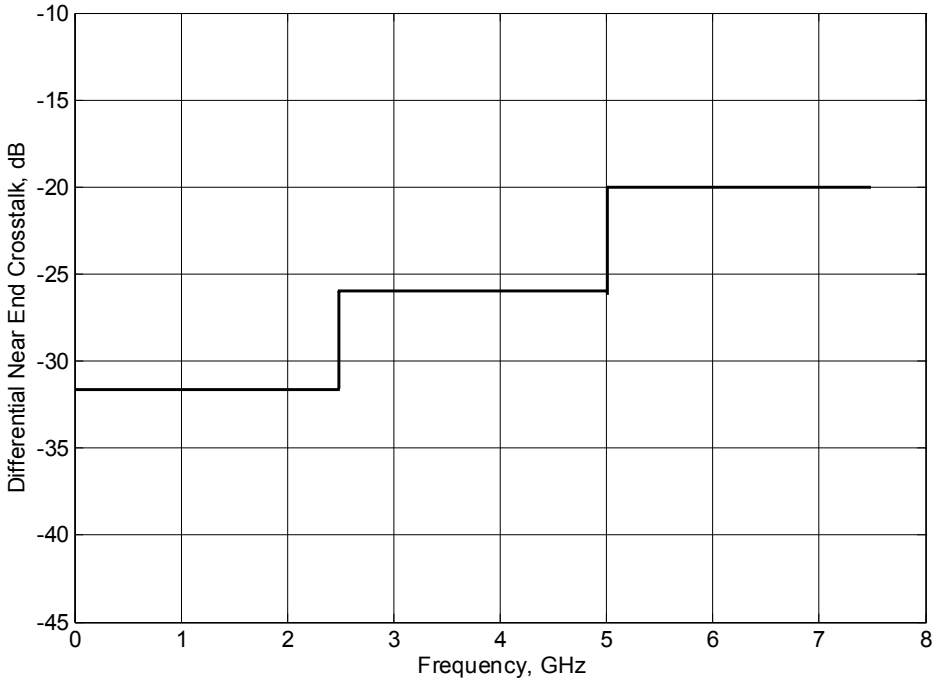


Figure 3: Illustration of different ial near end crosstalk requirement.

Switch Test Fixture Requirements

The test fixture for switch S-parameter measurement must be designed and built to specific requirements, as described below, to ensure good measurement quality and consistency:

- The test fixture must be a FR4-based PCB of the microstrip structure; the dielectric thickness or stackup shall be about 4mils.
- The total thickness of the test fixture PCB is 1.57mm (0.62").
- The measurement signals are launched into the switch from the top of the test fixture, capturing the through-hole stub effect.
- Traces between the DUT and measurement ports (SMA or microprobe) must be uncoupled from each other as much as possible. Therefore, the traces must be routed in a way that traces diverge from each other exiting from the switch pin field.
- The trace lengths between the DUT and measurement port must be minimized. The maximum trace length must not exceed 1000mils. The trace lengths between the DUT and measurement port must be equal.
- All of the traces on the test board and add-in card must be held to a characteristic impedance of 50Ω with a tolerance of ±7%.
- SMA connector is recommended for ease of use. The SMA launch structure must be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 60ps risetime must be within 50±7Ω.

Part Marking

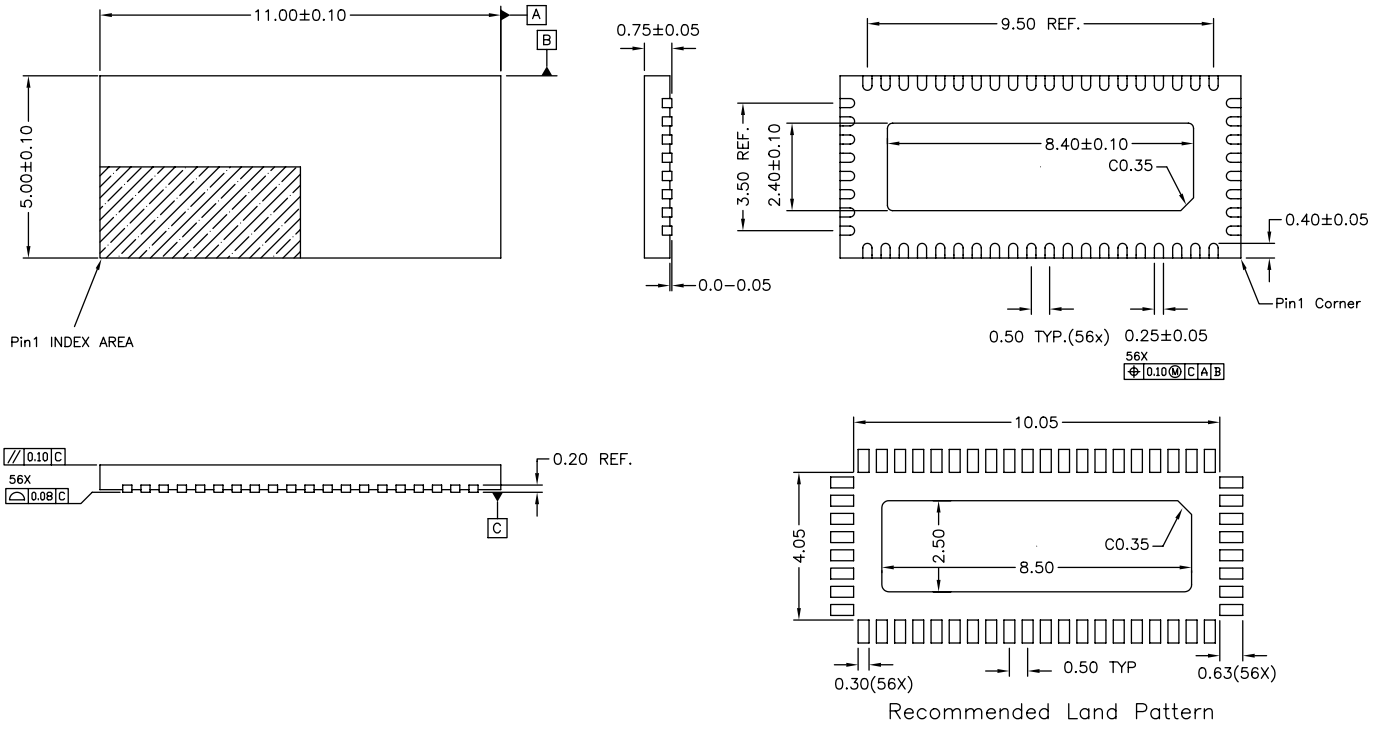
ZF Package - Cu Version

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

ZF Package - Au Version

YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 56-TQFN (ZF)



NOTE :
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−220 MODIFIED.
4. Thermal Via Diameter. Recommended 0.2~0.33mm
5. Thermal Via Pitch. Recommended 1.27mm

PERICOM Semiconductor Corporation	DATE: 05/15/08
DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)	
PACKAGE CODE: ZF56	
DOCUMENT CONTROL #: PD-2024	REVISION: C

08-0208

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE2612-AZFEX	ZF	56-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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