PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-DIS/13/8275
Dated 02 Jan 2014

Front-end diffusion Multi sourcing and additional

Electrical Wafer Sorting capacity for Field Effect Rectifiers Diodes

Table 1. Change Implementation Schedule

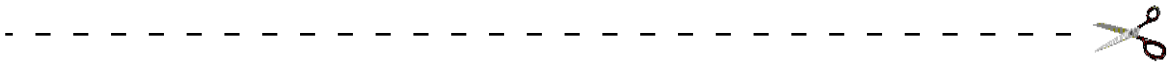
Forecasted implementation date for change	26-Dec-2013
Forecasted availability date of samples for customer	26-Dec-2013
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	26-Dec-2013
Estimated date of changed product first shipment	03-Apr-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	Field Effect Rectifiers Diodes
Type of change	Waferfab additional location
Reason for change	increase the production capacity
Description of the change	- Additional Front-end in subcontractor for the production of the silicons in Singapore - Additional Wafer testing capability in ST Toa Payoh plant
Change Product Identification	Trace code and QA number
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-DIS/13/8275**
Please sign and return to STMicroelectronics Sales Office	**Dated 02 Jan 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Paris, Eric	Marketing Manager
Duclos, Franck	Product Manager
Cazaubon, Guy	Q.A. Manager

PCN
Product/Process Change Notification

Front-end diffusion Multi sourcing and additional Electrical Wafer Sorting capacity for Field Effect Rectifiers Diodes

Notification number:	IPG-DIS/13/8275	**Issue Date**	26/12/2013
Issued by	Aline AUGIS		
Product series affected by the change		FERD product family	
Type of change		Wafer fab additional location	

Description of the change

- Additional Front-end in subcontractor for the production of the silicons in Singapore
- Additional Wafer testing capability in ST Toa Payoh plant

Reason for change

- Increase production capacity
- Back-up silicon production , both at dice production and die test levels

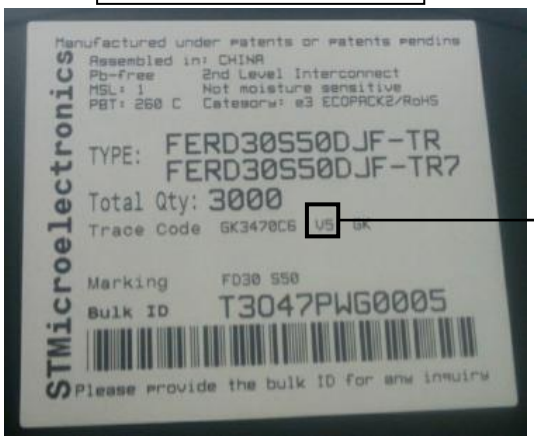
Former versus changed product:	The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Disposition of former products

Former products will be continued, as ST is implementing a capacity increase in this change.

Marking and traceability

CURRENTLY



AFTER PCN

V5 (ST plant)
or F2 (subcontractor)

Qualification complete date	W05-2014

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
RECTIFIER	FERD	FERD30S50DJF-TR	Now
	FERD	FERD30M45CT	Now
	FERD	FERD30M45CG-TR	Now

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
FERDxxxx50xx	**Wk06-2014**	**Wk13-2014**
FERDxxxx45xx		

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	13352QRP Attached

Reliability Report

Qualification of additional Front-End and Electrical Wafer Sorting AFER rectifiers dice production

General Information	
Product Line	*RECTIFIERS (BU 78)*
Product Description	*FERD30M45CT* *FERD30M45CGTR* *FERD30S50DJFTR*
Product division	*ASD&IPAD*
Packages	*TO-220, D²PAK, PQFN 6x5 8L*
Die Technology	*AFER*
Maturity level step	*TEMPORARY QUALIFICATION*

Locations	
Wafer fab	*SUBCONTRACTOR SINGAPORE*
Assembly plant	*ST SHENZHEN*
Reliability Lab	*ST TOURS*
Reliability assessment	*ON GOING*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Comment
1.0	04/12/2013	11	Aude DROMEL	Initial release

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
RER1321008	Reliability Evaluation Feport

2 GLOSSARY

SS	Sample Size
PC	Pre-conditionning
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
AC	Autoclave Test (Pressure Pot)
THB	Temperature Humidity Bias
IOLT	Intermittent Operating Life Test

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to assess a new subcontractor as FE Plant for AFER technology diffusion for 30Amps, 45/50V products mounted in D²PAK, TO-220 and PowerFlat 6x5 8leads packages.

Products perimeter and qualification test vehicles are listed below:

Product sub-family	Part Number	Packages
AFER Diodes 30A 45V	FERD30M45CT	TO-220AB
	FERD30M45CG	D²PAK
AFER Diodes 30A 50V	FERD30S50DJF	Power Flat

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology ».
The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB and HTFB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- THB, AC to check the robustness to corrosion and the good package hermeticity.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception at this time (no failure). It is stressed that reliability tests have shown that the devices behave correctly against environmental tests. Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime. No weakness has been identified by reliability test plan comparing results and drift analysis with initial technology's qualification results.

To prepare final qualification, test plan has to be fulfilled with last results available at this time. A final version of this reliability report will be issued once all tests finished.

4 DEVICE CHARACTERISTICS

4.1 Device description

Field Effect Rectifier

4.2 Construction note

	FERDx0x45Cx
Wafer/Die fab. information	
Wafer fab manufacturing location	Subcontractor Singapore
Technology	AFER
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Toa Payoh
Assembly information	
Assembly site	ST CHINA
Package description	TO-220AB / D²PAK/ PQFN
Molding compound	ECOPACK
Lead finishing process	Tin (Sn)
Final testing information	
Testing location	ST CHINA

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Part Number	Package	Comments
1	FERD30M45CT	TO-220	
2	FERD30M45CT	TO-220	
3	FERD30M45CGTR	D^2PAK	
4	FERD30M45CGTR	D^2PAK	
5	FERD30S50DJFTR	PQFN 6x5 8L	

Detailed results in below chapter will refer to these references.

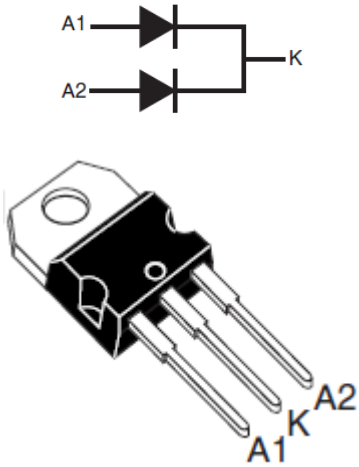
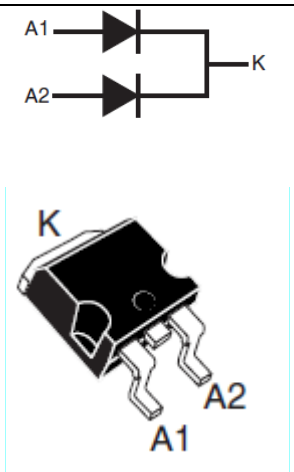
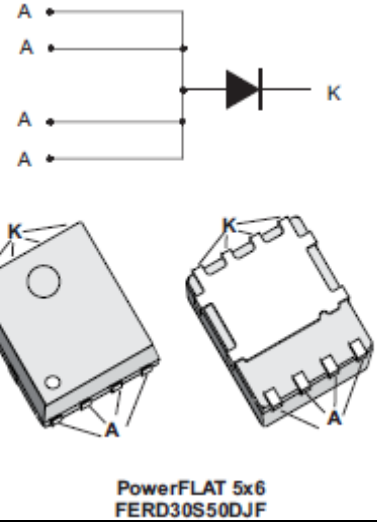
5.2 Test plan and results summary

Missing results for first release are replaced by the expected results availability date

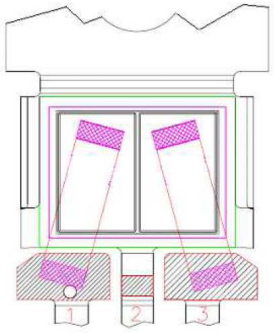
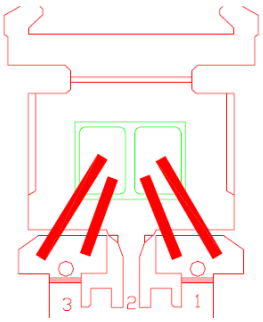
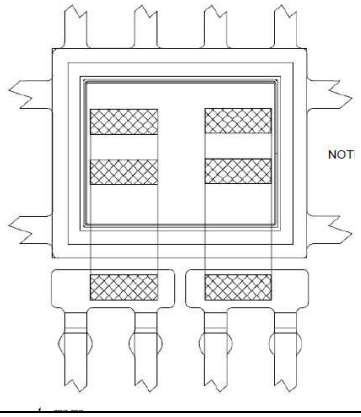
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	
Die Oriented Tests											
HTRB	-	JESD22 A-108	Tj = Tjmax* VR=36V	187	168H					W51-13	
					500H	0/25**	0/25**	0/30**	0/30**	W01-14	
					1000H	0/25**	0/25**	0/30**	0/30**	W04-14	
* Tjmax=maximal available temperature preventing from thermal runaway. ***for lots with no 168h results, reverse current @high temperature is monitored on all DUTs during the test											
HTFB	-	JESD22 A-108	Tj=150°C	381	168H	0/76	0/77	0/77	0/77	W49-13	
					504H	0/76	0/77	0/77	W49-13	W51-13	
					1000H	0/76	0/77	0/77	W52-13	W02-14	
Package Oriented Tests											
TC	Y	JESD22 A-104	-65°C/+150°C 2cy/h	177	500 cycles	0/25	0/25	0/25	0/25	W50-13	
IOLT	Y	MIL-STD 750 Method 1037	ΔTc = 85°C t_{on} = t_{off} = 210s	50	5K cycles		0/25		0/25		
					10K cycles		0/25		0/25		
AC	Y	JESD22 A-102	121°C 2 bars 100%RH	100	96H	0/25	0/25	0/25	0/25		
THB	Y	JESD22 A-101	85°C; 85%HR VR=36V	100	168H	0/25	0/25	0/25	0/25		
					504H						
					1000H						

6 ANNEXES

6.1 Pin connection

Package	Product	Pin connection
TO-220AB	**FERD30M45CT**	
D²PAK	**FERD30M45CG**	
PowerFLAT	**FERD30S50DJF**	

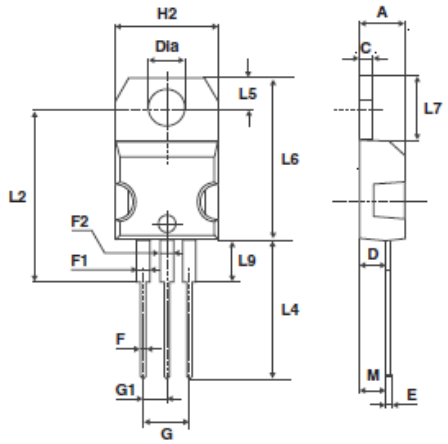
6.2 Bonding diagram

Package	Product	Bonding diagram
TO-220AB	**FERD30M45CT**	
D²PAK	**FERD30M45CG**	
PowerFLAT	**FERD30S50DJF**	

Note : Generic scheme (die / wire bonding sizes and die design given as example)

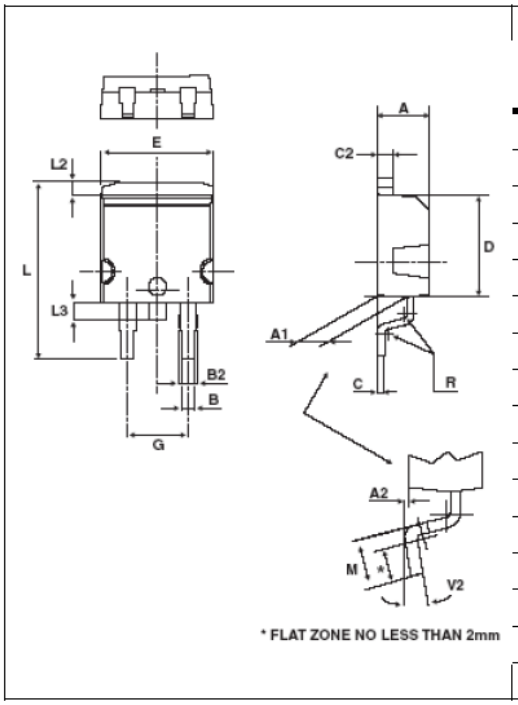
6.3 Package outline/Mechanical data

TO-220AB dimensions



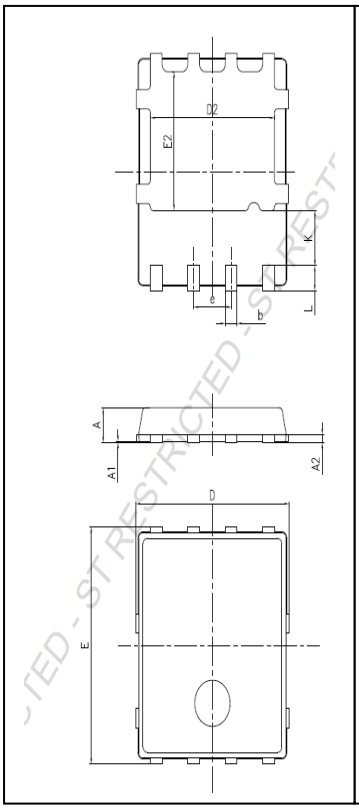
Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
C	1.23	1.32	0.048	0.051
D	2.40	2.72	0.094	0.107
E	0.49	0.70	0.019	0.027
F	0.61	0.88	0.024	0.034
F1	1.14	1.70	0.044	0.066
F2	1.14	1.70	0.044	0.066
G	4.95	5.15	0.194	0.202
G1	2.40	2.70	0.094	0.106
H2	10	10.40	0.393	0.409
L2	16.4 typ.		0.645 typ.	
L4	13	14	0.511	0.551
L5	2.65	2.95	0.104	0.116
L6	15.25	15.75	0.600	0.620
L7	6.20	6.60	0.244	0.259
L9	3.50	3.93	0.137	0.154
M	2.6 typ.		0.102 typ.	
Diam.	3.75	3.85	0.147	0.151

D²PAK dimensions



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
A1	2.49	2.69	0.098	0.106
A2	0.03	0.23	0.001	0.009
B	0.70	0.93	0.027	0.037
B2	1.14	1.70	0.045	0.067
C	0.45	0.60	0.017	0.024
C2	1.23	1.36	0.048	0.054
D	8.95	9.35	0.352	0.368
E	10.00	10.40	0.393	0.409
G	4.88	5.28	0.192	0.208
L	15.00	15.85	0.590	0.624
L2	1.27	1.40	0.050	0.055
L3	1.40	1.75	0.055	0.069
M	2.40	3.20	0.094	0.126
R	0.40 typ.		0.016 typ.	
V2	0°	8°	0°	8°

PowerFLAT di_ mensions



DIMENSIONS				
REF. DIM	DATA BOOK (mm)			NOTES
	NOM	MIN	MAX	
A		0.80	1.00	
A1		0.02	0.05	
A2	0.25			
b		0.30	0.50	
D	5.20			
E	6.15			
D2		4.11	4.31	
E2		3.50	3.70	
e	1.27			
L		0.50	0.80	
K		1.275	1.575	

Tests Description

6.4 Tests Description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
IOLT	All test samples shall be subjected to the specified number of cycles. When stabilized after initial warm-up cycles, a cycle shall consist of an "on" period, when power is applied suddenly, not gradually, to the device for the time necessary to achieve a delta case temperature (delta is the high minus the low mounting surface temperatures) of +85°C (+60°C for thyristors) +15°C, -5°C, followed by an off period, when the power is suddenly removed, for cooling the case through a similar delta temperature. Auxiliary (forced) cooling is permitted during the off period only. Heat sinks are not intended to be used in this test, however, small heat sinks may be used when it is otherwise difficult to control case temperature of test samples, such as with small package types (e.g., TO39).	The purpose of this test is to determine compliance with the specified numbers of cycles for devices subjected to the specified conditions. It accelerates the stresses on all bonds and interfaces between the chip and mounting face of devices subjected to repeated turn on and off of equipment and is therefore most appropriate for case mount style (e.g., stud, flange, and disc) devices.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
AC Autoclave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.

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