3.3V, PCI Express® 3.0 2-Lane, 2:1 Mux/DeMux Switch

Features

- 4 Differential Channel, 2:1 Mux/DeMux
- PCI Express® 3.0 Performance, 8.0Gbps
- Pinout optimized for placement between two PCIe slots
- Bi-directional operation
- Low Bit-to-Bit Skew, 10ps max
- Low Crosstalk: -48dB @4GHz
- High Off Isolation: -22dB @4GHz
- Low Insertion Loss: -1.6dB @4GHz
- Return Loss: -15dB @4GHz
- V_{DD} Operating Range: +3.3V
- Industrial Temperature Range: -40°C to 85°C
- ESD Tolerance: 2kV HBM
- Low channel-to-channel skew, 20ps max
- Packaging (Pb-free & Green):
  - 42-contact, TQFN (ZH42), 3.5 x 9mm
  - 40-contact, TQFN (ZL40), 3 x 6mm

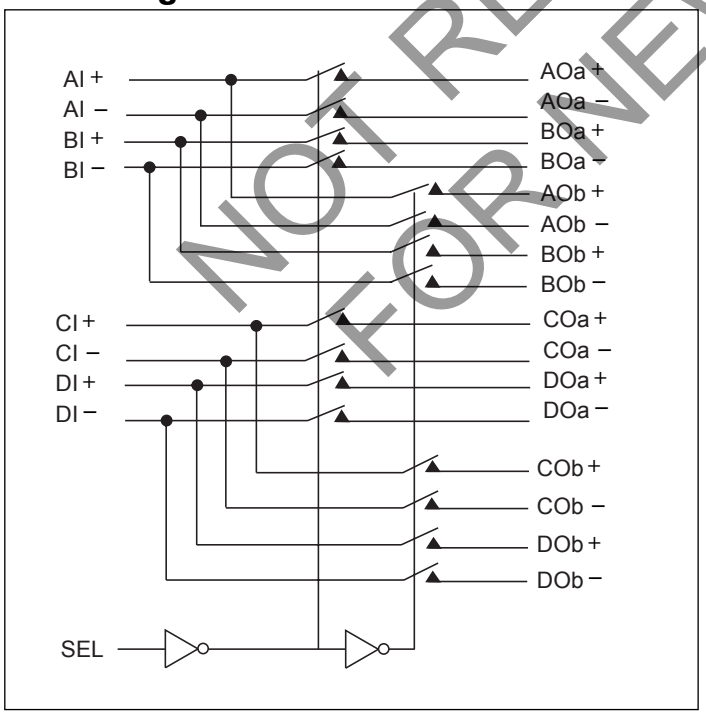
Description

Diodes Incorporated PI3PCIE3415 is an 8 to 4 differential channel multiplexer/demultiplexer switch. This solution can switch 2 full PCI Express® 3.0, lanes to one of two locations. Using a unique design technique, Diodes has been able to minimize the impedance of the switch such that the attenuation observed through the switch is negligible. The unique design technique also offers a layout targeted for PCI Express signals, which minimizes the channel to channel skew as well as channel to channel crosstalk as required by the PCI Express specification.

Application

Routing of PCI Express 3.0, DP1.2, USB3.0, SAS2.0, SATA3.0, XAUI, RXAUI signals with low signal attenuation.

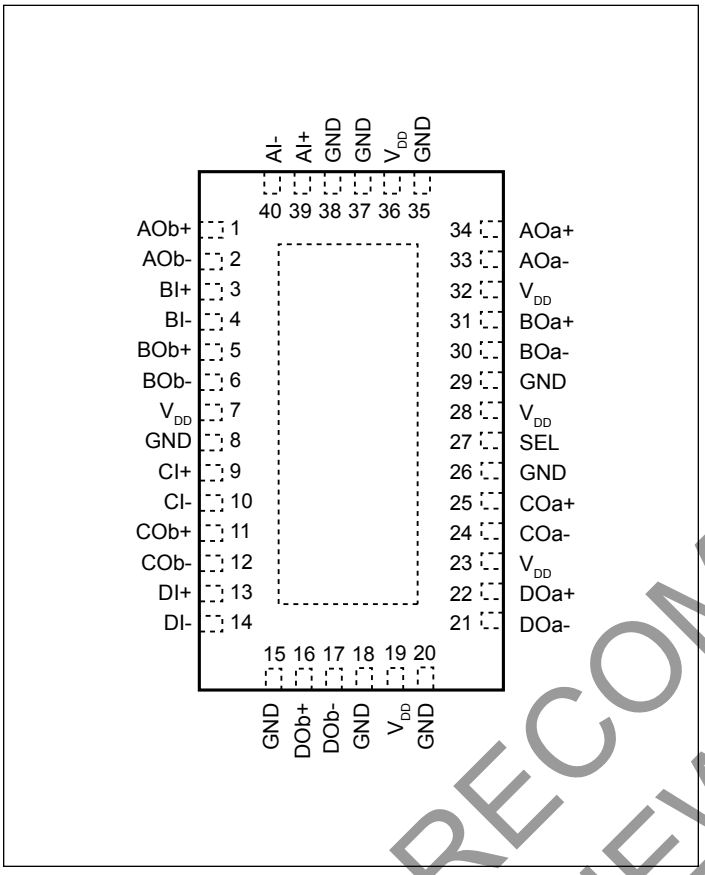
Block Diagram



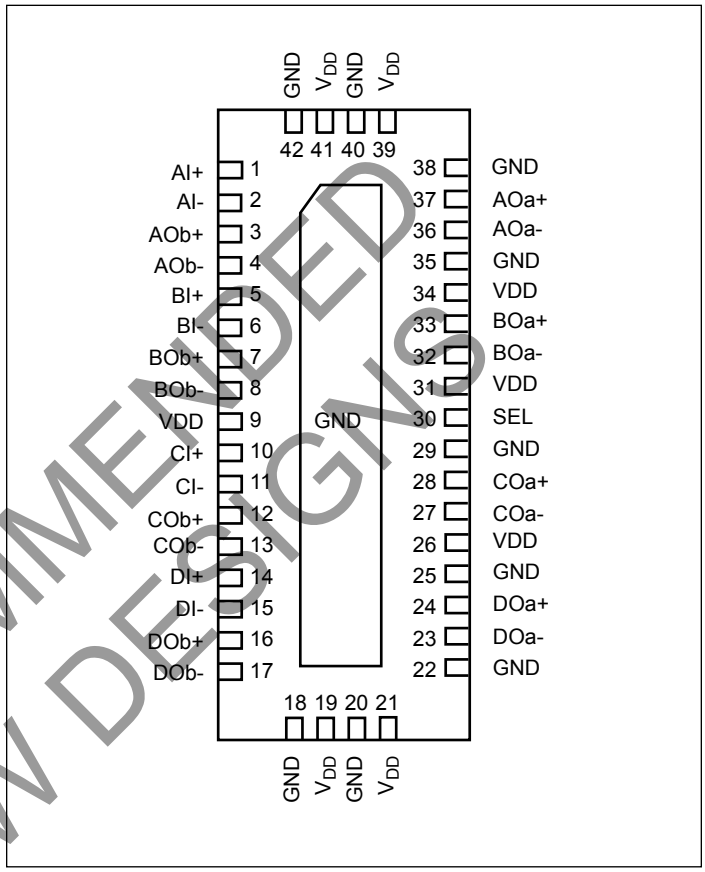
Truth Table

Function	SEL
xIy to xOay	L
xIy to xOby	H

Pin Description 40-Contact TQFN (Top-Side View)



Pin Description 42-Contact TQFN (Top-Side View)



Signal Descriptions

Pin Number		Pin Name	Type	Description
42-TQFN	40-TQFN			
1, 2	39, 40	AI+, AI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the AOa+, AOa- pin respectively when SEL=0. Signal is routed to the AOb+, AOb- pin respectively when SEL = 1.
37, 36	34, 33	AOa+, AOa-	Differential I/O	Differential analog pass-through I/O. Signal from AI+ and AI- is routed to AOa+ and AOa- respectively when SEL=0.
3, 4	1, 2	AOb+, AOb-	Differential I/O	Differential analog pass-through I/O. Signal from AI+ and AI- is routed to AOb+ and AOb- respectively when SEL=1.
5, 6	3, 4	BI+, BI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the BOa+, BOa- pin respectively when SEL=0. Signal is routed to the BOb+, BOb- pin respectively when SEL = 1.
33, 32	31, 30	BOa+, BOa-	Differential I/O	Differential analog pass-through I/O. Signal from BI+ and BI- is routed to BOa+ and BOa- respectively when SEL=0.
7, 8	5, 6	BOb+, BOb-	Differential I/O	Differential analog pass-through I/O. Signal from BI+ and BI- is routed to BOb+ and BOb- respectively when SEL=1.
10, 11	9, 10	CI+, CI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the COa+, COa- pin respectively When SEL=0. Signal is routed to the COb+, COb- pin respectively when SEL = 1.
28, 27	25, 24	COa+, COa-	Differential I/O	Differential analog pass-through I/O. Signal from CI+ and CI- is routed to COa+, COa- pin respectively when SEL = 0.
12, 13	11, 12	COb+, COb-	Differential I/O	Differential analog pass-through I/O. Signal from CI+ and CI- is routed to COb+, COb- pin respectively when SEL = 1.
14, 15	13, 14	DI+, DI-	Differential I/O	Differential I/O pair from PCIE signal source. Signal is routed to the DOa+, DOa- pin respectively When SEL=0. Signal is routed to the DOb+, DOb- pin respectively when SEL = 1.
24, 23	22, 21	DOa+, DOa-	Differential I/O	Differential analog pass-through I/O. Signal from DI+ and DI- is routed to DOa+, DOa- pin respectively when SEL = 0.
16, 17	16, 17	DOb+, DOb-	Differential I/O	Differential analog pass-through I/O. Signal from DI+ and DI- is routed to DOb+, DOb- pin respectively when SEL = 1.
18, 20, 22, 25, 29, 35, 38, 40, 42	15, 18, 20, 26, 29, 35, 37, 38, Center Pad	GND	Ground input	Ground
30	27	SEL	3.6V tolerant low-voltage single-ended input	SEL controls the mux through a flow-through latch.
9, 19, 21, 26, 31, 34, 39, 41	7, 19, 23, 28, 32, 36	VDD	Power supply	Power, 3.3V ±10%

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C
Supply Voltage to Ground Potential .....–0.5V to +4.6V
Channel DC Input Voltage .....–0.5V to 1.5V
DC Output Current 120mA
Power Dissipation 0.5W
SEL DC Input Voltage .....–0.5V to 4.6V

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	3.3V Power Supply		3.0	3.3	3.6	V
I_{DD}	Total current from V_{DD} 3.3V supply	SEL = 0V or V_{DD}	0	0.15	1	mA
T_A	Operating temperature range		-40		85	°C

DC Electrical Characteristics (T_A = –40°C to +85°C, V_{DD} = 3.3V ± 10%)

Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{IH-SEL}	Input high level, SEL input		2.0		3.6	V
V_{IL-SEL}	Input Low Level, SEL input		0		0.8	V
I_{IN_SEL}	Input Leakage Current, SEL input	Measured with input at VIH-SEL max and VIL-SEL min	–10		10	uA
I_{IH}	Input High Current, xI, xO	V_{DD} = Max, V_{IN} = 1.5V	–10		10	uA
I_{IL}	Input Low Current, xI, xO	V_{DD} = Max, V_{IN} = 0V	–10		10	uA
I_{IH}	Input High Current, SEL	V_{DD} = Max, V_{IN} = V_{DD}	–5		5	uA
I_{IL}	Input Low Current, SEL	V_{DD} = Max, V_{IN} = 0V	–5		5	uA
I_{OZH}	HighZ High Current xOa, xOb	V_{DD} = Max, V_{IN} = 1.5V	–10		10	uA
I_{OZL}	HighZ Low Current xOa, xOb	V_{DD} = Max, V_{IN} = 0V	–10		10	uA

Note:

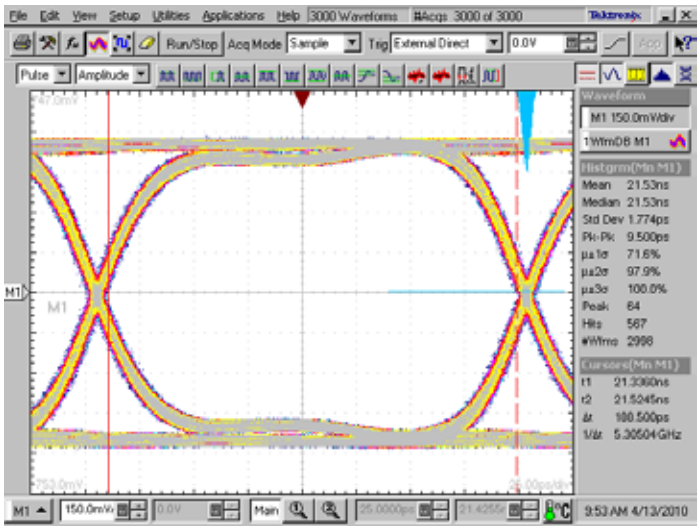
1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics for xI+/-, xOy+/-

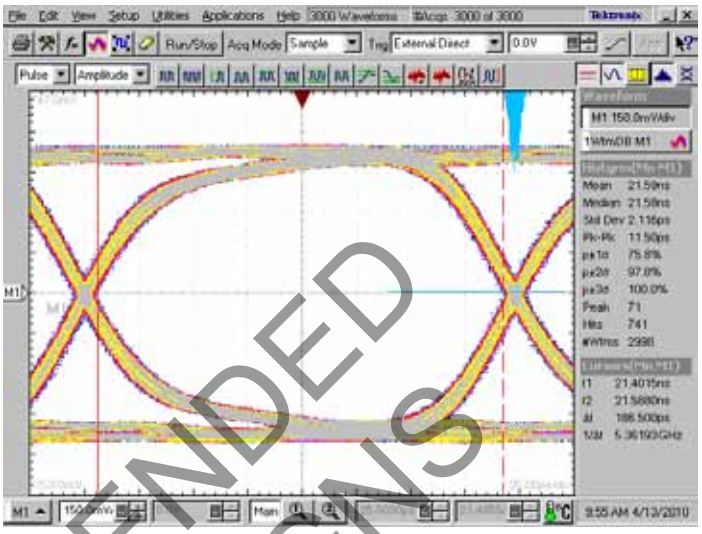
Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
DDIL	Differential Insertion Loss	f=50MHz -1.25GHz f=1.25GHz - 2.5GHz f=2.5GHz - 4GHz f=5.0GHz		-0.8 -1.1 -1.6 -1.7	-1.0 -1.3 -1.9 -2.0	dB
$DDIL_{OFF}$	Differential Off Isolation	f= 0 to 4.0GHz	-25.8 -20.6 -17.6 -15.4	-32.2 -25.8 -22.0 -19.3		
DDRL	Differential Return Loss	f=50MHz - 1.25GHz f=1.25GHz - 2.5GHz f=2.5GHz - 4GHz f=5.0GHz	-18.2 -16.8 -12 -8	-22.7 -21.0 -15.0 -10.0		
DDNEXT	Near End Crosstalk	f=50MHz -1.25GHz f=1.25GHz - 2.5GHz f=2.5GHz - 4GHz f=5.0GHz	-44.8 -41.6 -38.4 -36	-56 -52 -48 -45		
BW	Bandwidth -3dB			8.7		GHz

Switching Characteristics

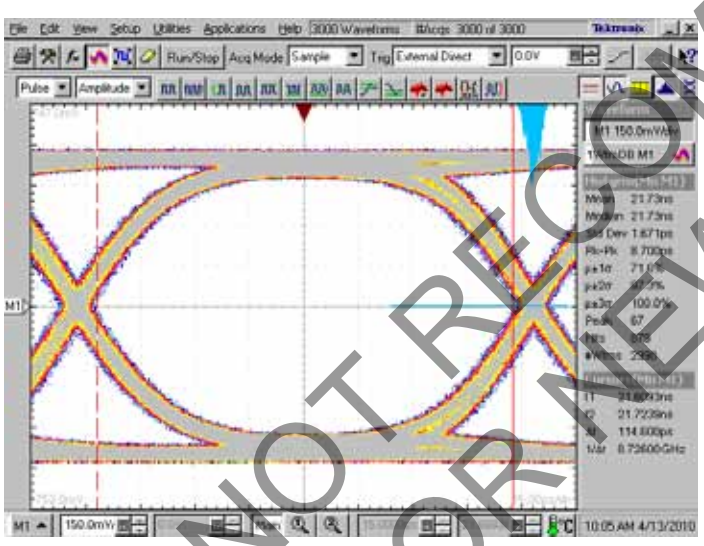
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time - SEL to xI+/-, xOy+/-	See "Test Circuit for Electrical Characteristics"	0.5	15	25	ns
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to xI+/-, xOy+/-	See "Test Circuit for Electrical Characteristics"	0.5	5	25	ns
t_{b-b}	Bit-to-bit skew within the same differential pair	See "Test Circuit for Electrical Characteristics"		4	10	ps
t_{ch-ch}	Channel-to-channel skew	See "Test Circuit for Electrical Characteristics"			20	ps



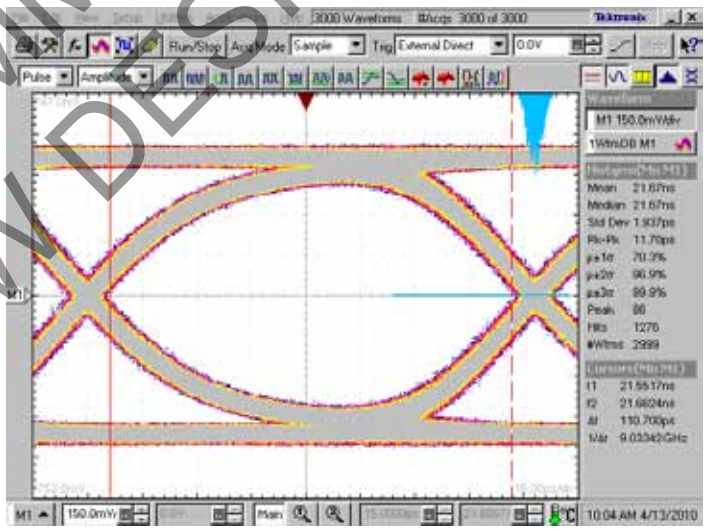
5.0 Gbps RX signal eye without PI3PCIE3415



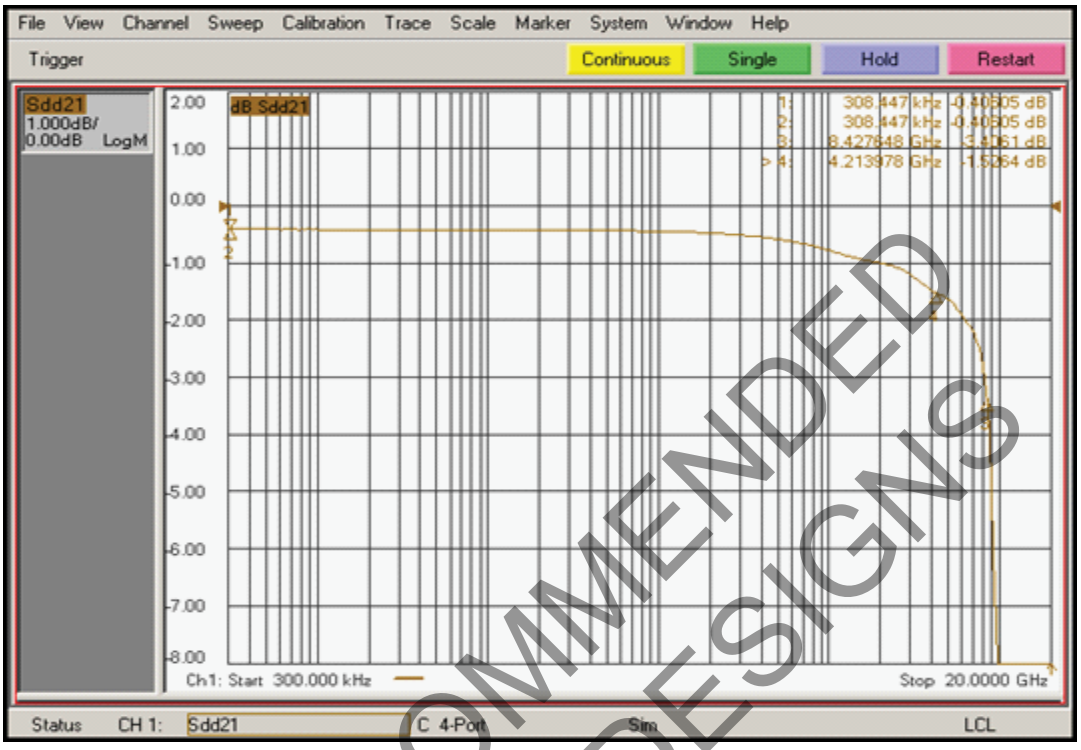
5.0 Gbps RX signal eye with PI3PCIE3415



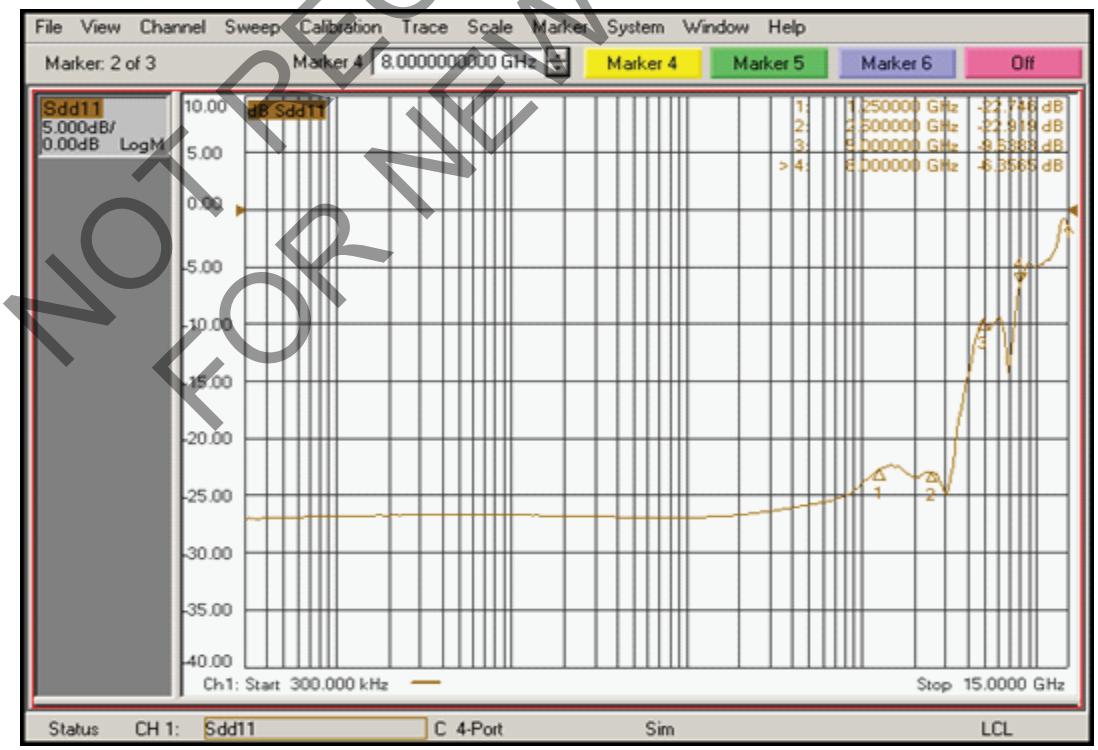
8.0 Gbps RX signal eye without PI3PCIE3415



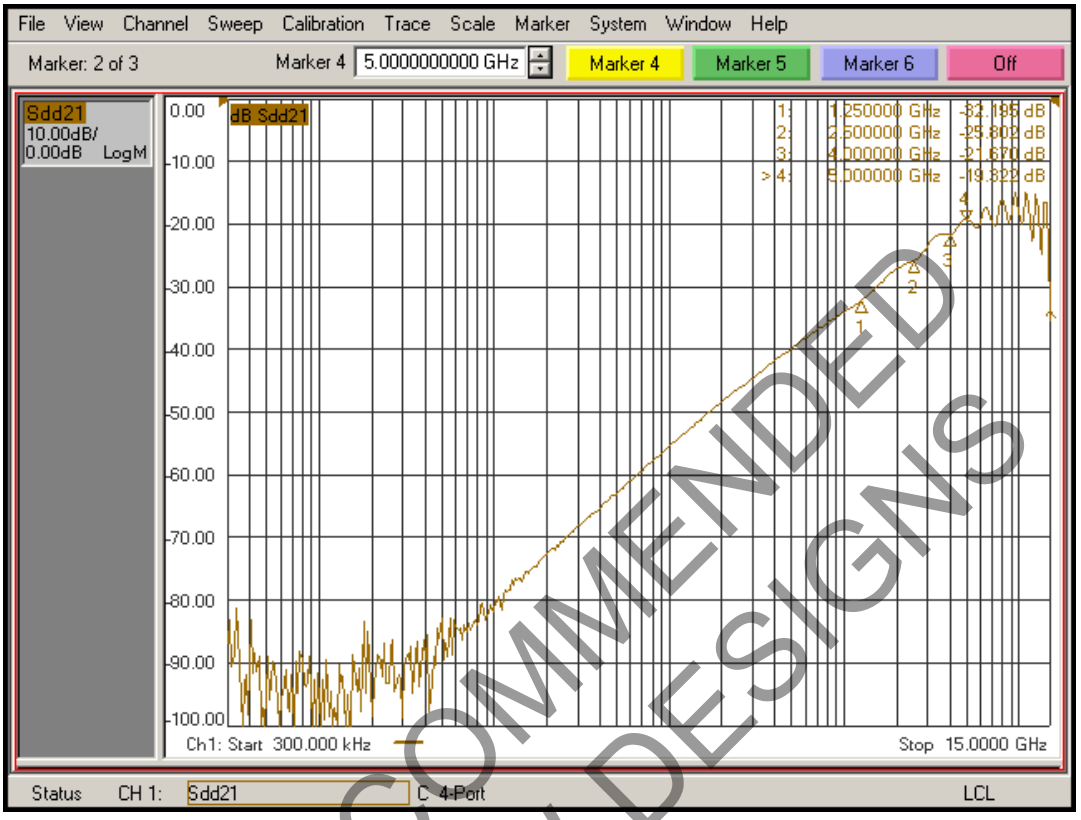
8.0 Gbps RX signal eye with PI3PCIE3415



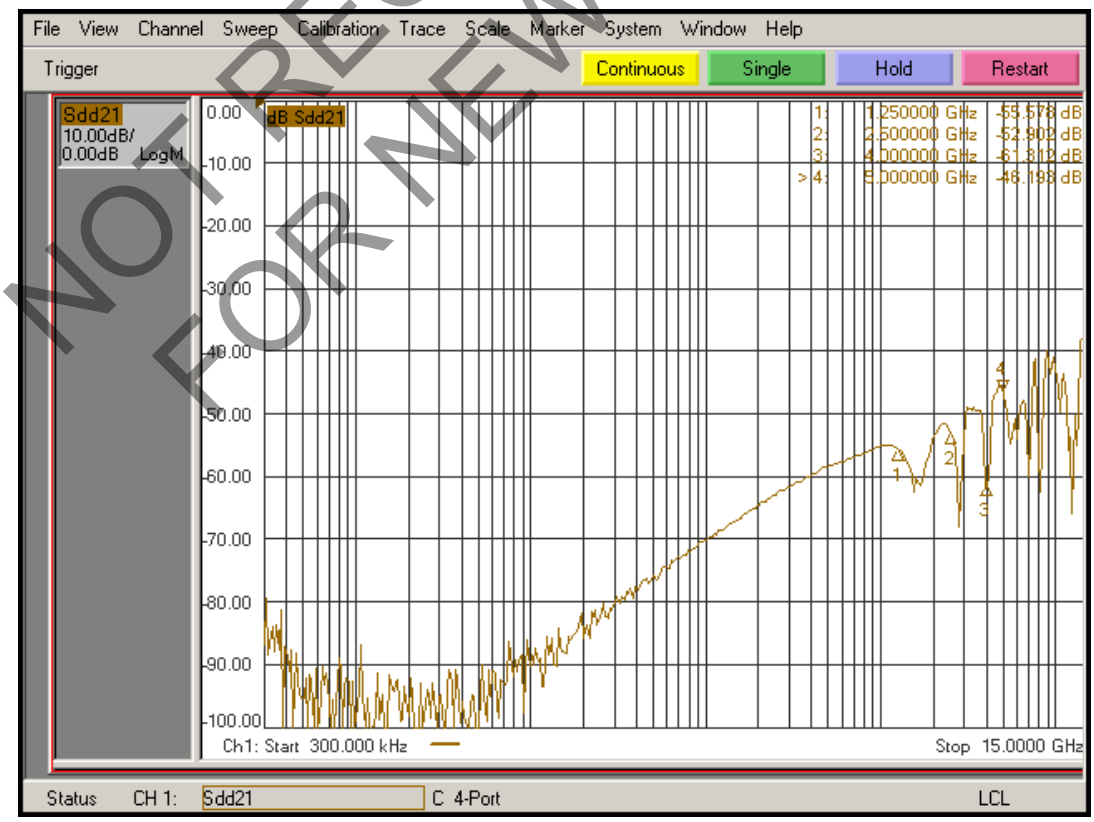
Differential Insertion Loss



Differential Return Loss

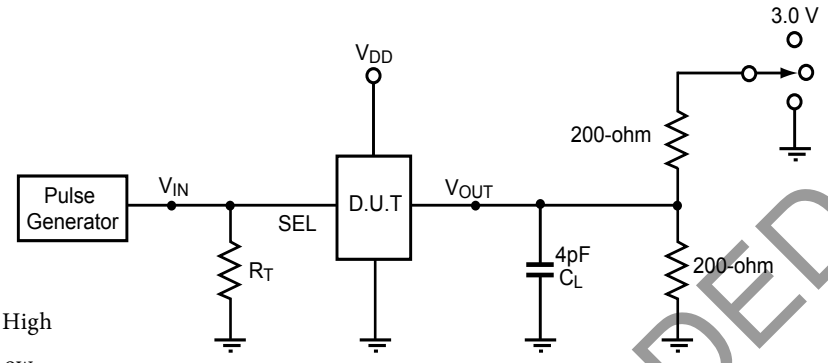


Differential Off Isolation



Differential Crosstalk

Test Circuit for Electrical Characteristics(1-5)



*V_{OUT} = Port 1 or Port 2

tpZH/HZ = COM Port is High

tpLZ/ZL = COM Port is Low

Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.

2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

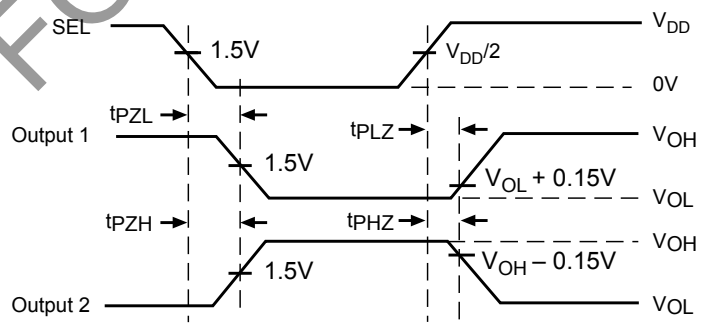
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.

5. The outputs are measured one at a time with one transition per measurement

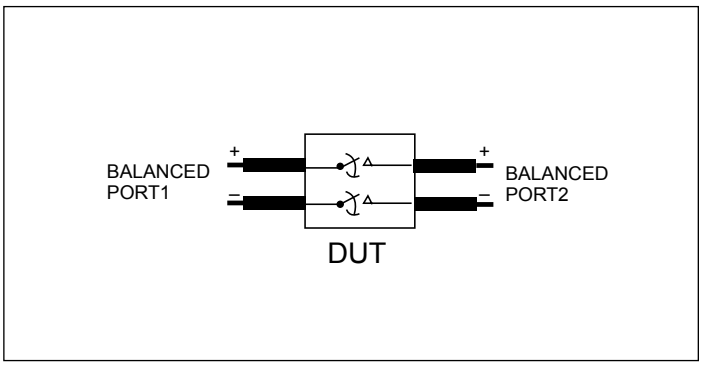
Switch Positions

Test	Switch
t_{PLZ}, t_{PZL}	3.0V
t_{PHZ}, t_{PZH}	GND

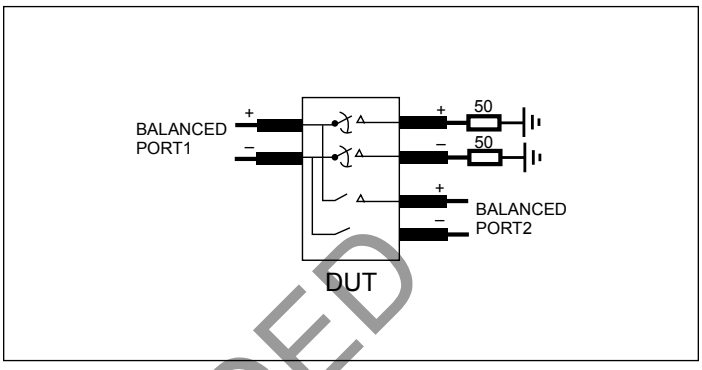
Switching Waveforms



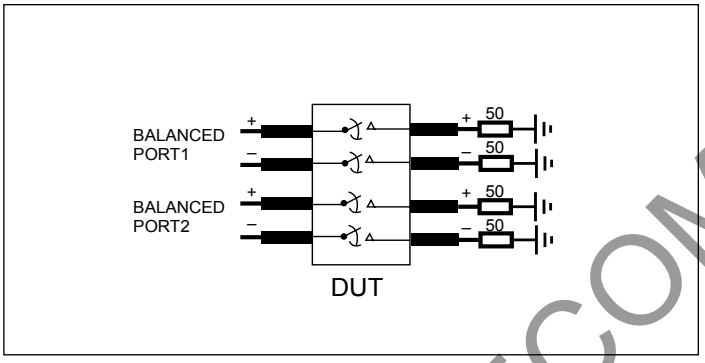
Voltage Waveforms Enable and Disable Times



Differential Insertion Loss and Return Test Circuit

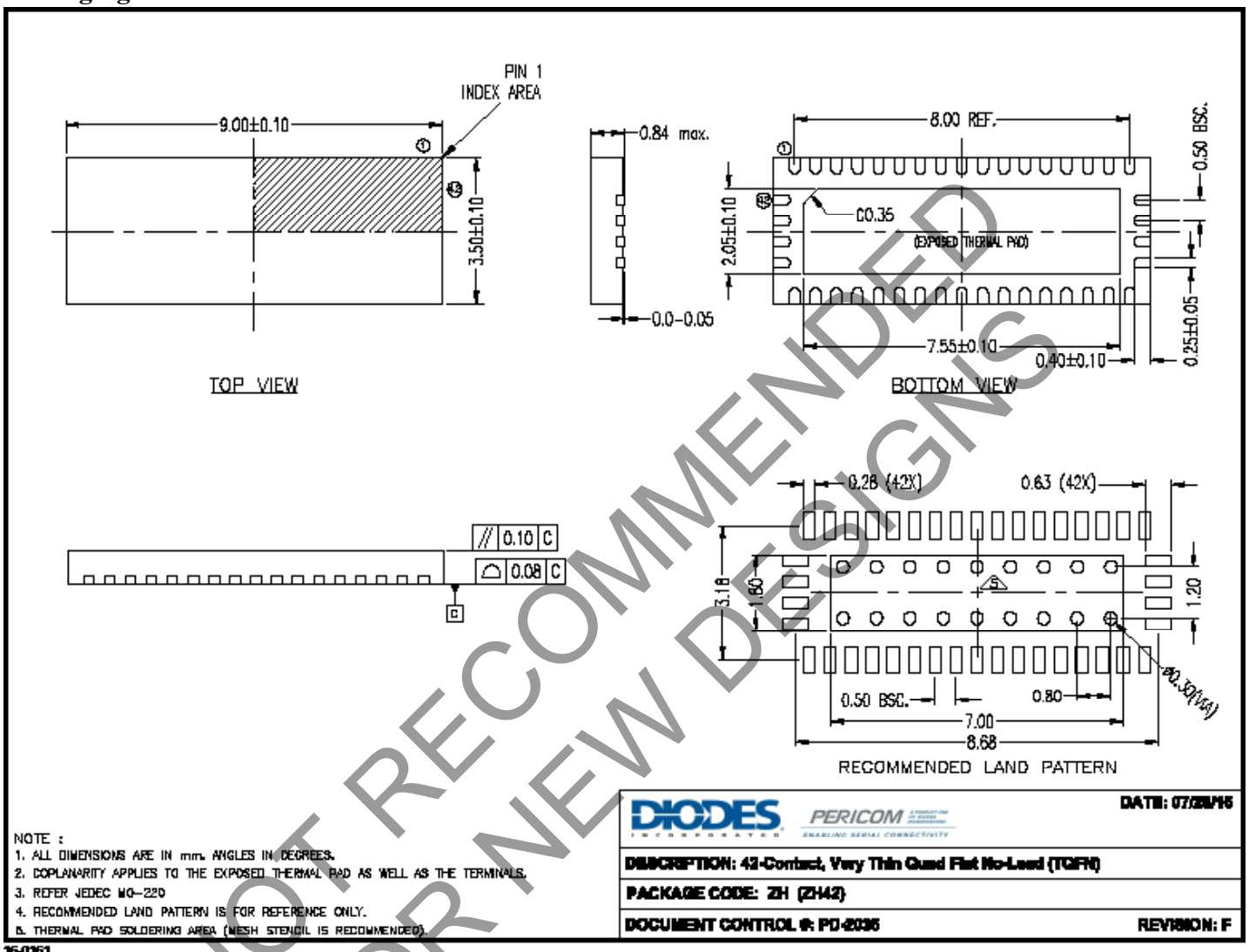


Differential Off Isolation Test Circuit

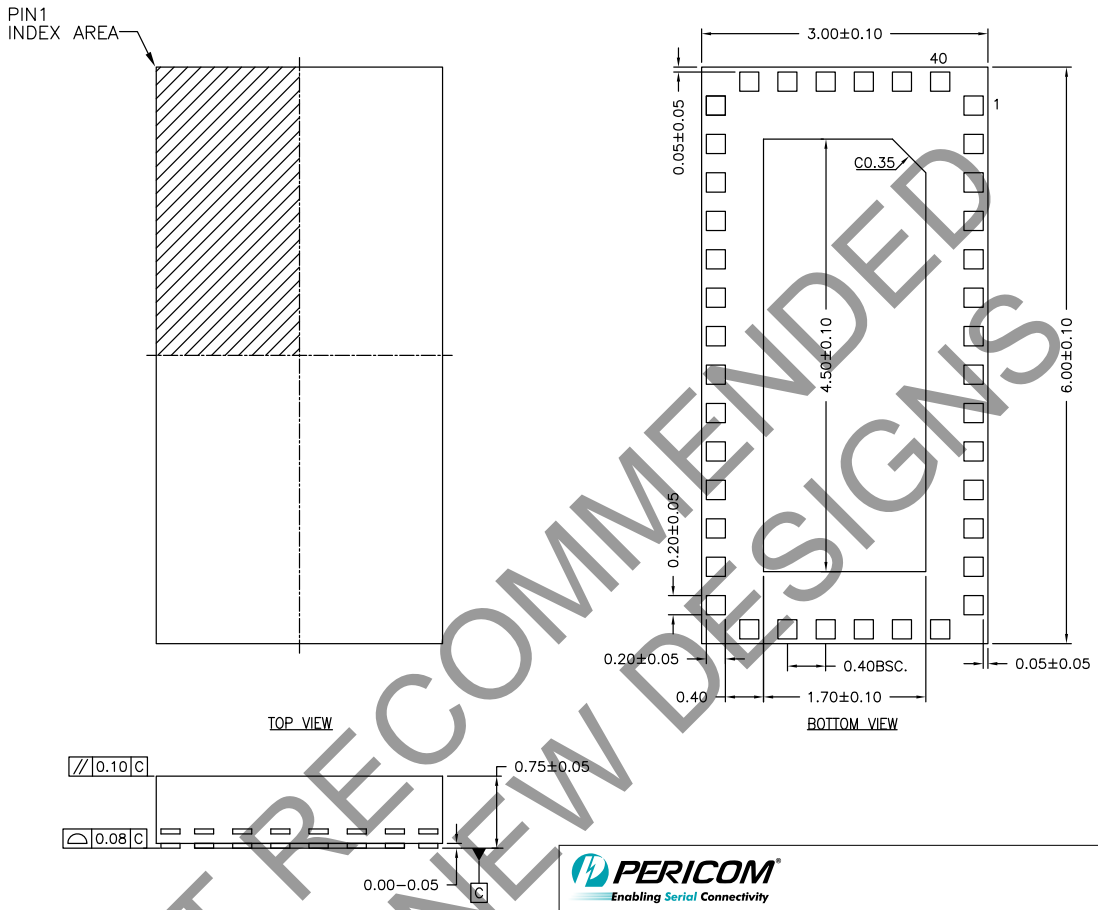


Differential Near End Xtalk Test Circuit

Packaging Information



Packaging Information



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
3. Refer JEDEC MO-220

PERICOM Enabling Serial Connectivity

DATE: 07/11/13

DESCRIPTION: 40-contact, Thin Fine Pitch Quad Flat No-Lead, TQFN

PACKAGE CODE: ZL (ZL40)

DOCUMENT CONTROL #: PD-2165 **REVISION: --**

Note: For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE3415ZHE	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN)
PI3PCIE3415ZHEX	ZH	42-contact, Very Thin Quad Flat No-Lead (TQFN), Tape & Reel
PI3PCIE3415ZLE	ZL	40-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)
PI3PCIE3415ZLEX	ZL	40-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN), Tape & Reel

Notes:

- **Thermal characteristics can be found on the company web site at www.pericom.com/packaging/**
- **"E" denotes Pb-free and Green**
- **Adding an "X" at the end of the ordering code denotes tape and reel packaging**