Keywords: MAX8660, PCB, printed circuit board, layout

APPLICATION NOTE 4049

MAX8660/MAX8661 PCB Layout Guide

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Abstract: The MAX8660/MAX8661 evaluation kit provides an example that uses a one-sided printed circuit board (PCB) layout to optimize performance. Whereas the evaluation kit PCB layout provides optimal performance and eases evaluation, other layouts are also acceptable. This application note provides a step-by-step procedure for achieving a reliable PCB layout with the MAX8660/MAX8661.

Introduction

The MAX8660/MAX8661 are highly integrated power-management ICs (PMICs). The high efficiency and small size of these devices make them ideal for portable battery-powered applications, such as smart cell phones, PDAs, and portable media players.

Good printed circuit board (PCB) layout is necessary to achieve optimal MAX8660/MAX8661 performance. The evaluation kit (EVKIT) for the MAX8660 provides an example layout that optimizes its performance. For implementations that cannot utilize this layout, this application note provides procedures and design tips for maximizing the performance of your MAX8660-based design.

MAX8660EVKIT

The MAX8660EVKIT has been provided as a PCB layout example and has the following characteristics:

- Four layers
- 1oz copper
- All components on one side of the PCB
- 5mil vias between layers 1 and 2 to route digital signals

The MAX8660/MAX8661 do not require a one-sided PCB layout—two-sided layouts are also acceptable. The MAX8660EVKIT utilizes a one-sided PCB layout for the following reasons:

- All dynamic switching currents for the step-down regulators are contained to the top layer of metal. There are no dynamic switching currents that flow through vias.
- Many designs use 8- to 12-layer PCB designs. It is common to place noisy components such as the PMIC on one side of the PCB, while placing sensitive components such as a GPS receiver on the other side. Because the middle layers of the board are ground, they effectively isolate the two sides from each other. The MAX8660EVKIT was created to be single-sided so that it can easily be ported to these applications.
- For lab evaluations, it is convenient to have all components on one side so they can all be easily probed.
- Additionally, having all components on one side allows the board to lie flat on the table, further easing lab evaluation.

To maintain a small PCB area, the evaluation kit utilizes blind microvias (5mil vias between layers 1 and 2) to route digital signals. Similar layouts can be achieved without these blind microvias at the expense of area.

Maxim encourages MAX8660/MAX8661 users to follow the MAX8660EVKIT layout as closely as possible. To facilitate this we provide the Gerber files[1] for the MAX8660EVKIT layout. For PCB designs in which the MAX8660EVKIT layout cannot be adopted, this application note provides a step-by-step procedure that can be followed to achieve a reliable layout.

Support Documents for this Application Note

- MAX8660 data sheet
- MAX8660EVKIT data sheet
- MAX8660EVKIT Gerber files
- Mechanical description of the board (**Appendix**)

PCB Layout Procedure for the MAX8660/MAX8661

The reference designators used in this section match the schematics shown in the EVKIT data sheet (refer to Figure 4 in the MAX8660EVKIT data sheet). It is highly recommended that you consult the layout within the EVKIT data sheet (Figures 5, 6, 7, 8, and 9 in the EVKIT data sheet) and these recommendations at the same time.

The elements of this procedure are listed in order of importance. Items at the top are most important.

1. Step-Down Converter Input Bypass Capacitors
    - Place C12 between PV3(28) and PG3(26) as close as possible to the IC.
    - Place C11 between PV1(36) and PG1(34) as close as possible to the IC.
    - Place C15 between PV2(14) and PG2(16) as close as possible to the IC.
    - Place C18 between PV4(3) and PG4(5) as close as possible to the IC.
    - The step-down converter input bypass capacitors are the most critical components because they carry discontinuous currents with a high rate of change (di/dt). Minimizing the inductance between the step-down converter input bypass capacitors and the PVx and PGx pins is critical. **Install the input capacitors on the same side of the PCB as the MAX8660/MAX8661 IC in order to minimize inductance.** Placing the input capacitor on the opposite side of the PCB as the MAX8660 IC is not ideal because the vias that are necessary to connect the two halves of the PCB add inductance to this critical path.
    - The MAX8660/MAX8661 provide one buck converter on each side of the IC package, thereby allowing buck input capacitors to be placed close to their PVx and PGx pins.
    - Each buck converter has a pinout with PVx, LXx, and PGx such that PVx and PGx are separated by one pin. The pinout, along with the package's pin pitch, makes a 0603 size input capacitor ideal.
    - Connect each input capacitor ground terminal to the internal ground plane with multiple vias. Multiple vias reduce resistance and inductance.
    - Connect each input capacitor positive terminal to the internal power plane with multiple vias. Multiple vias reduce resistance and inductance.
2. IC Power Input, Ramp-Setting Resistor, and Low-Battery Comparator Components
    - Place C22 between IN(18) and AGND(19) as close as possible to the IC.
    - Place R10 next to C22.
    - Place R2 between LBF(21) and LBR(22) as close as possible to the IC.
    - Place R1 and R3 next to R2; keep the high-impedance nodes at LBF(21) and LBR(22) as

small as possible.

- Place R4 as close to RAMP(24) as possible.
- Collect the grounds for the components in this section together on a small analog ground island. Use a single via to connect this analog ground island to the internal ground plane.
- Connect the power-input filter resistor (R10) to the internal power plane with a via.
- Connect the top of the low-battery comparator resistor string (R1) to the internal power plane with a via.

3. Step-Down Converter Output Capacitors
   - Place C3, C4, and C5 such that their ground terminal is as close as possible to PG3(26).
   - Place C1 and C2 such that their ground terminal is as close as possible to PG1(34).
   - Place C6 and C7 such that their ground terminal is as close as possible to PG2(16).
   - Place C8 and C9 such that their ground terminal is as close as possible to PG4(5).
   - Use a thick trace/plane to connect the capacitor ground terminals to their respective power ground pin (PGx). Use as wide of a trace as possible when connecting to PGx.
   - Connect each copper pour to the internal ground plane with multiple vias.
4. Step-Down Converter Inductors
   - Place L3 between LX3(27) and the output capacitors C3, C4, and C5.
   - Place L1 between LX1(35) and the output capacitors C1 and C2.
   - Place L2 between LX2(15) and the output capacitors C6 and C7.
   - Place L4 between LX4(4) and the output capacitors C8 and C9.
   - Use a wide trace to connect the inductor to its respective LX node (LXx). The trace needs to be wide to carry the converter's output current.
   - Minimize the area of the LXx nodes. These nodes need to be wide to carry current; however, they should be as short as possible to minimize total radiating area since these nodes switch very rapidly between PVx and PGx and, subsequently, are a source of noise.
   - Minimize stray capacitance on the LXx nodes. Stray capacitance will result in poor efficiency.
   - Minimize the electrical length and loop area of the current paths shown in **Figure 1** and described below. Minimizing the electrical length of these paths reduces parasitic resistance; minimizing loop area reduces radiated noise.
     - From the positive terminal of the input capacitor → into PVx → out of LXx → through the inductor → through the output capacitors → back to the input capacitor ground terminal.
     - From LX → through the inductor → through the output capacitors → to the power ground pin (PGx).
   - Note that inductors store energy in a magnetic field. This magnetic field can interfere with sensitive circuits that are placed near the inductor. To contain the magnetic flux within the area of the inductor, many inductors are shielded. Shielded inductors are typically very good and present no noise-related applications problems. If using an unshielded inductor, use great care to ensure that the magnetic flux does not corrupt sensitive circuits.

     When using shielded inductors, take a little time to investigate the construction of the inductor. Many shielded inductors have a gap in the shield on one side where the inductor windings enter/exit the bobbin and connect to the inductor terminals. The emitted magnetic field is much larger on the side of the inductor that has this gap. It is best to orient the inductor so that any gaps in the shielding face away from sensitive circuits. The shielded inductors used in the MAX8660EVKIT have a small gap in the shielding—this gap is oriented facing the bracket "[" on the EVKIT silk screen. This ensures the region of higher magnetic field is away from the sensitive output-sense lines.

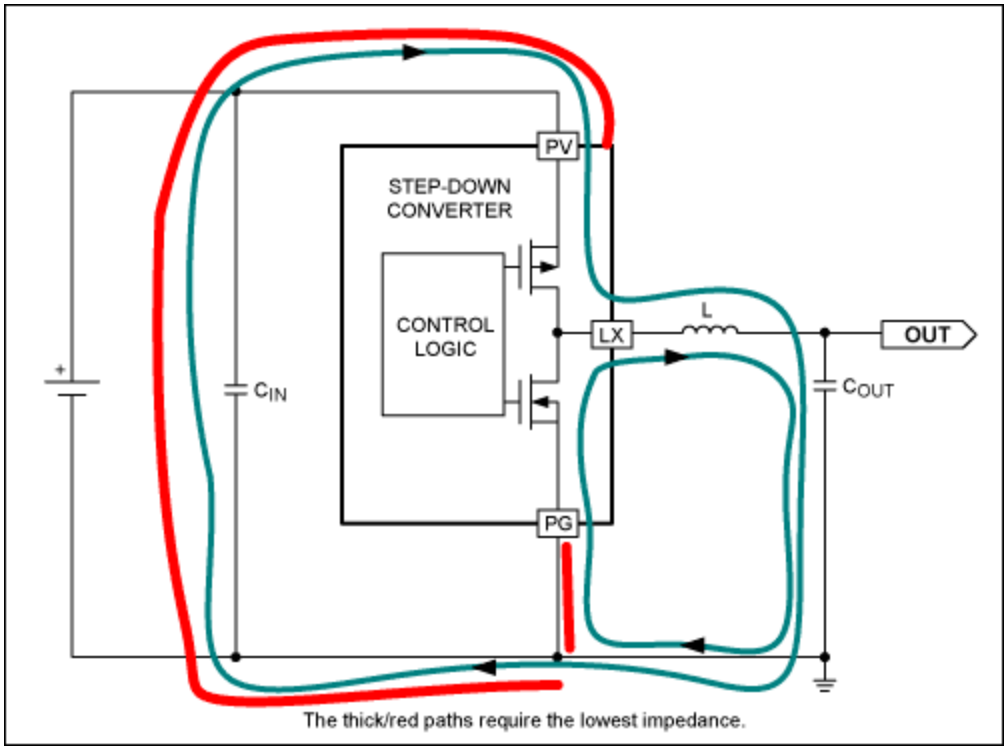

Figure 1. Step-down converter current loops.

5. Step-Down Converter Output-Sense Lines
    - Connect V3(30) to the positive terminal of the output capacitors C3, C4, and C5.
    - Connect V1(36) to the positive terminal of the output capacitors C1 and C2.
    - Connect V2(10) to the positive terminal of the output capacitors C6 and C7.
    - Connect V4(40) to the positive terminal of the output capacitors C8 and C9.
    - Connect each sense line to its respective output capacitors in a location where there is relatively low dynamic current flow—refer to the MAX8660EVKIT for an example.
    - Route each sense line away from noise sources such as the inductor at the LX node. See also the note about inductor orientation in Step D above.
6. LDO Input and Output Capacitors
    - The positions of the LDO input/output capacitors are not as critical as the above-mentioned components.
    - Place the LDO capacitors in the available space around the IC using the MAX8660EVKIT as a guideline:
    - LDO5
        - IN5, V5
    - LDO8
        - IN8, V8
    - LDO6/7
        - IN67, V6, V7
7. Digital I/Os
    - The digital I/O lines are relatively insensitive to layout. Route the following signals in the available space around the IC:
        - Active-low LBO, EN1, EN2, EN34, EN5, SET1, SET2, SRAD, active-low MR, active-low RSO, SDA, SCL

8. Exposed Pad
    - The exposed pad (EP) is the main path for heat to exit the IC. Connect EP to the ground plane with multiple vias to allow heat to dissipate from the device. Heat dissipation is optimized if the top-layer PCB pad connects to as many PCB layers as possible with multiple vias. Fill the PCB landing pad with as many vias as will fit.

      Also see application note 862, "Thermal Consideration of QFN and Other Exposed-Paddle Packages" and application note 3500, "Monitor Head Dissipation in Electronics Systems by Measuring Active Component Die Temperature" for additional information.

Conclusion

By following the above layout procedure and referencing the MAX8660EVKIT data sheet you can obtain a proven, robust layout for your MAX8660-based designs.

APPENDIX

MECHANICAL DESCRIPTION OF BOARD
MAX8660 EVALUATION KIT REV-B

Material	RoHS-compliant FR-4 laminate material compatible with lead-free soldering processes
Size (in x in)	3.200 x 3.000
Thickness (in)	0.062
Layers	4
Solder Mask	Green LPI SMOBC
Legends	White (clipped all legends from exposed metal)
Copper Clad (oz)	1

Vendor Logo and Date Code: Allowed only in ink on bottom side only.

Plating	Must be lead free and RoHS compliant
Finish	Vendor should use the most economical lead-free and RoHS-compliant process available or as specified in PO. Approved Finish: HASL Lead-free solder Immersion tin Immersion gold
Thru Holes (in, min)	0.001
Quality	Manufactured in accordance with IPC-A-600

Number of Surface Mount Pads: 128

Number of Thru Holes (drl14):	183
Number of Blind Vias:	
Layer 1 to Layer 2 (drl12):	17
Number of Microvias:	17
Microvia Hole Size (in):	0.005

Tolerances

Parameter	Tolerance (in)
Board Dimensions	±0.010
Plated-Thru Holes	±0.003
Pattern to Pattern	±0.005
Solder Mask to Pattern	±0.005
Legend to Legend	±0.007

Drill schedule is located on the drill plot.

File Names and Descriptions

File Name	Description
art01.pho	Layer 1: Photo of Layer Copper
art01.rep	Layer 1: Photo-Plotter Apertures Report
art02.pho	Layer 2: Photo of Layer Copper
art02.rep	Layer 2: Photo-Plotter Apertures Report
art03.pho	Layer 3: Photo of Layer Copper
art03.rep	Layer 3: Photo-Plotter Apertures Report
art04.pho	Layer 4: Photo of Layer Copper
art04.rep	Layer 4: Photo-Plotter Apertures Report
dd0124.pho	Drill Drawing Photo
dd0124.rep	Drill Drawing Report
drl12.drl	Layer 1 to Layer 2 Drill File
drl12.lst	Layer 1 to Layer 2 Drill Location Listing
drl12.rep	Layer 1 to Layer 2 Drill Size Report
drl14.drl	Layer 1 to Layer 4 Drill File
drl14.lst	Layer 1 to Layer 4 Drill Location Listing
drl14.rep	Layer 1 to Layer 4 Drill Size Report
smb0428.pho	Bottom Solder-Mask Photo
smb0428.rep	Bottom Solder-Mask Report
smt0121.pho	Top Solder-Mask Photo
smt0121.rep	Top Solder-Mask Report
ssb0429.pho	Bottom Silk-Screen Photo
ssb0429.rep	Bottom Silk-Screen Report
sst0126.pho	Top Solder-Mask Photo

sst0126.rep	Top Solder-Mask Report

[1]Many free Gerber files viewers are available for download on the Internet.

Related Parts		
MAX8660	High-Efficiency, Low-I_Q, PMICs with Dynamic Voltage Management for Mobile Applications	Free Samples

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 4049: http://www.maximintegrated.com/an4049
APPLICATION NOTE 4049, AN4049, AN 4049, APP4049, Appnote4049, Appnote 4049