

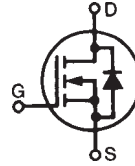
# Polar™ HiPerFET™ Power MOSFET

## IXFR140N30P

$V_{DSS} = 300V$   
 $I_{D25} = 70A$   
 $R_{DS(on)} \leq 28m\Omega$   
 $t_{rr} \leq 200ns$

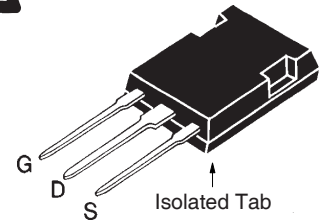
(Electrically Isolated Back Surface)

N-Channel Enhancement Mode  
Avalanche Rated



Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ C$ to $150^\circ C$	300	V
$V_{DGR}$	$T_J = 25^\circ C$ to $150^\circ C$ , $R_{GS} = 1M\Omega$	300	V
$V_{GSS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ C$	70	A
$I_{DM}$	$T_C = 25^\circ C$ , Pulse Width Limited by $T_{JM}$	300	A
$I_A$	$T_C = 25^\circ C$	70	A
$E_{AS}$	$T_C = 25^\circ C$	5	J
$dV/dt$	$I_S \leq I_{DM}$ , $V_{DD} \leq V_{DSS}$ , $T_J \leq 150^\circ C$	20	V/ns
$P_D$	$T_C = 25^\circ C$	300	W
$T_J$		-55 ... +150	$^\circ C$
$T_{JM}$		150	$^\circ C$
$T_{stg}$		-55 ... +150	$^\circ C$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ C$
$T_{SOLD}$	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
$V_{ISOL}$	50/60 Hz, RMS	$t = 1min$ 2500	V~
	$I_{ISOL} \leq 1mA$	$t = 1s$ 3000	V~
$M_d$	Mounting Force	20..120 / 4.5..27	N/lb.
<b>Weight</b>		5	g

ISOPLUS247  
E153432



G = Gate      D = Drain  
S = Source

### Features

- Silicon Chip on Direct-Copper-Bond Substrate
  - High Power Dissipation
  - Isolated Mounting Surface
  - 2500V Electrical Isolation
- Unclamped Inductive Switching (UIS) Rated
- Low package inductance
  - Easy to Drive and to Protect
- Fast Intrinsic Diode

### Advantages

- Easy to Mount
- Space Savings
- High Power Density

Symbol	Test Conditions ( $T_J = 25^\circ C$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V$ , $I_D = 3mA$	300		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 8mA$	3.0		5.0 V
$I_{GSS}$	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			$\pm 200$ nA
$I_{DSS}$	$V_{DS} = V_{DSS}$ , $V_{GS} = 0V$ $T_J = 125^\circ C$			25 $\mu A$ 1 mA
$R_{DS(on)}$	$V_{GS} = 10V$ , $I_D = 70A$ , Note 1	20		28 m $\Omega$

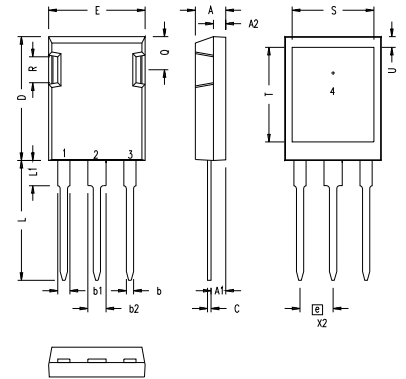
Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 20\text{V}$ , $I_D = 70\text{A}$ , Note 1	50	90	S
$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		14.8	nF
$C_{oss}$			1830	pF
$C_{rss}$			55	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 70\text{A}$ $R_G = 1\Omega$ (External)		30	ns
$t_r$			30	ns
$t_{d(off)}$			100	ns
$t_f$			20	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 70\text{A}$		185	nC
$Q_{gs}$			72	nC
$Q_{gd}$			60	nC
$R_{thJC}$			0.42	$^\circ\text{C/W}$
$R_{thCS}$		0.15		$^\circ\text{C/W}$

### Source-Drain Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$I_s$	$V_{GS} = 0\text{V}$			140 A
$I_{SM}$	Repetitive, pulse width limited by $T_{JM}$			560 A
$V_{SD}$	$I_F = 70\text{A}$ , $V_{GS} = 0\text{V}$ , Note 1			1.3 V
$t_{rr}$	$I_F = 25\text{A}$ , $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$ , $V_{GS} = 0\text{V}$			200 ns
$Q_{RM}$			0.6	$\mu\text{C}$
$I_{RM}$			6.0	A

Note 1: Pulse test,  $t \leq 300\mu\text{s}$ ; duty cycle,  $d \leq 2\%$ .

### ISOPLUS247 (IXFR) Outline



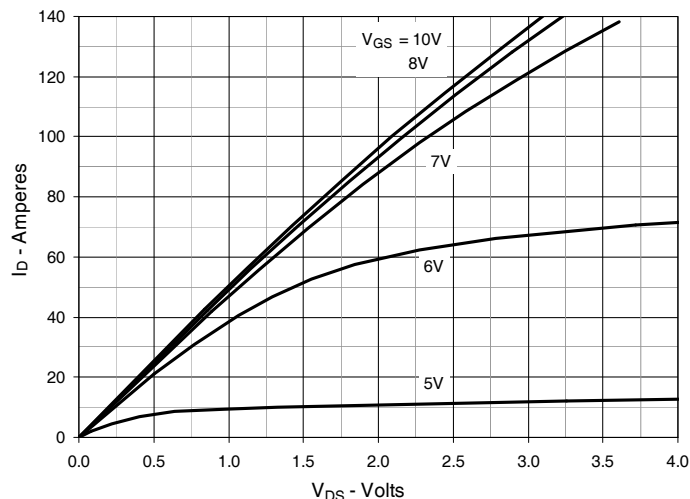
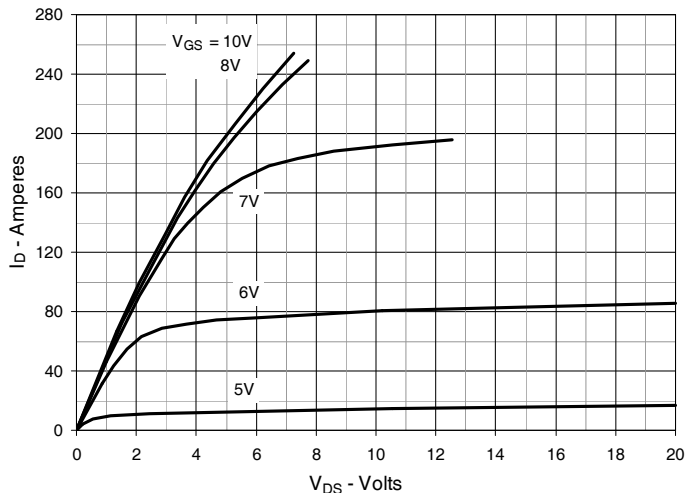
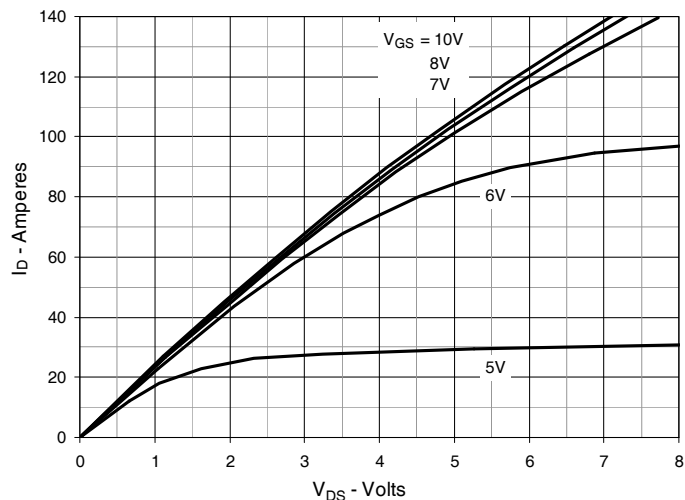
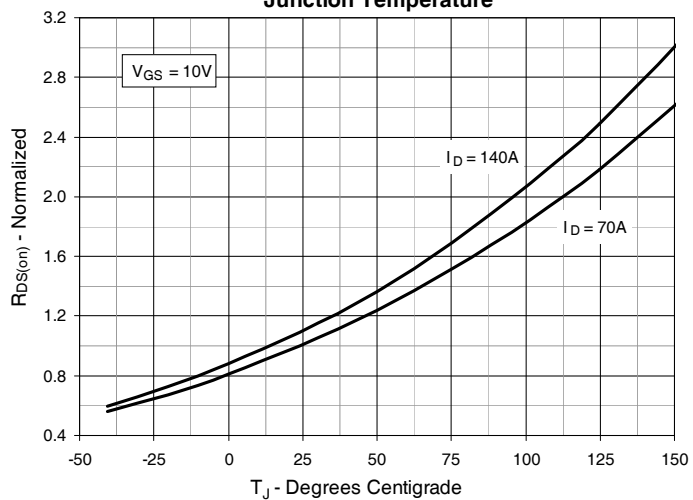
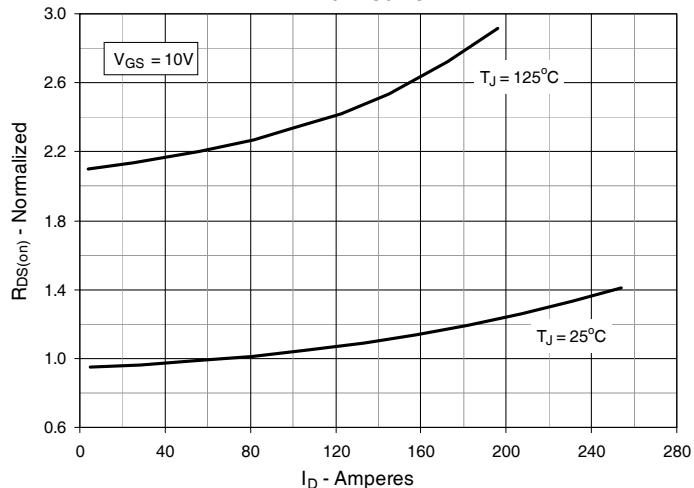
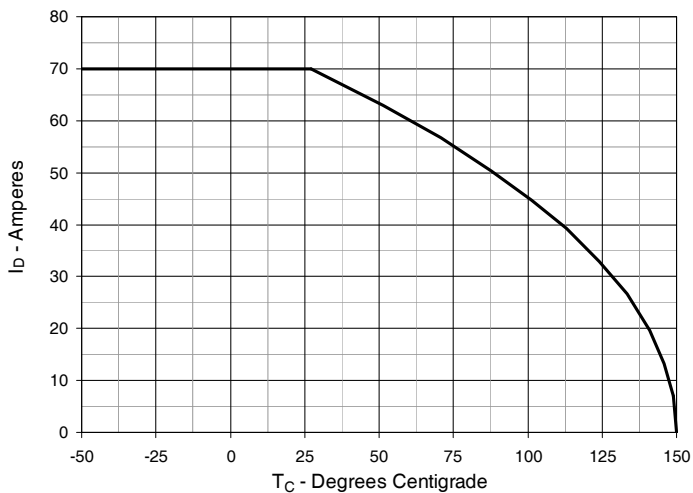
SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 - Gate      2 - Drain  
3 - Source    4 - Isolated

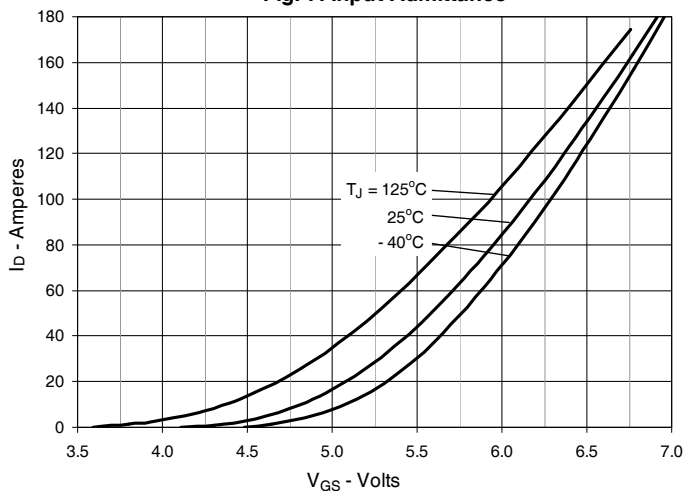
NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

IXYS reserves the right to change limits, test conditions, and dimensions.

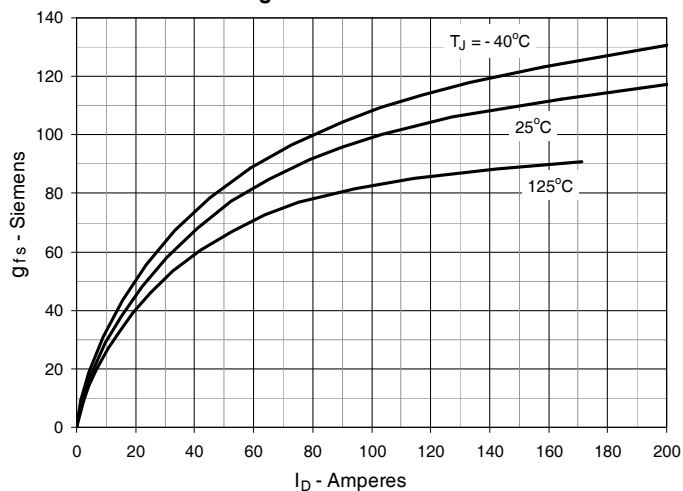
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 2. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 3. Output Characteristics @  $T_J = 125^\circ\text{C}$** 

**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 70\text{A}$  Value vs. Junction Temperature**

**Fig. 5.  $R_{DS(on)}$  Normalized to  $I_D = 70\text{A}$  Value vs. Drain Current**

**Fig. 6. Maximum Drain Current vs. Case Temperature**


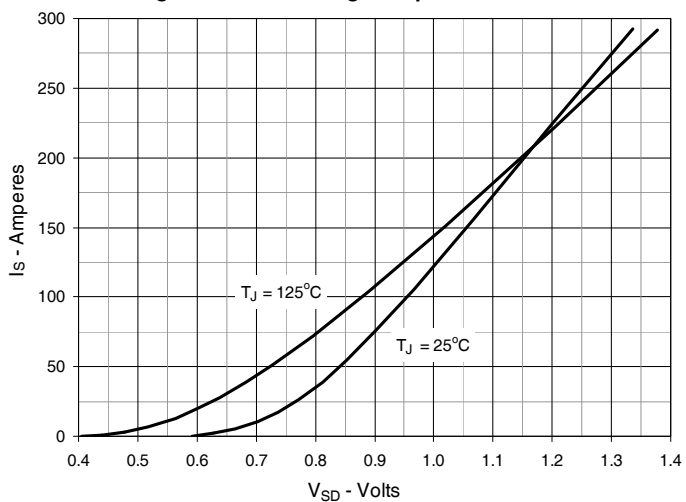
**Fig. 7. Input Admittance**



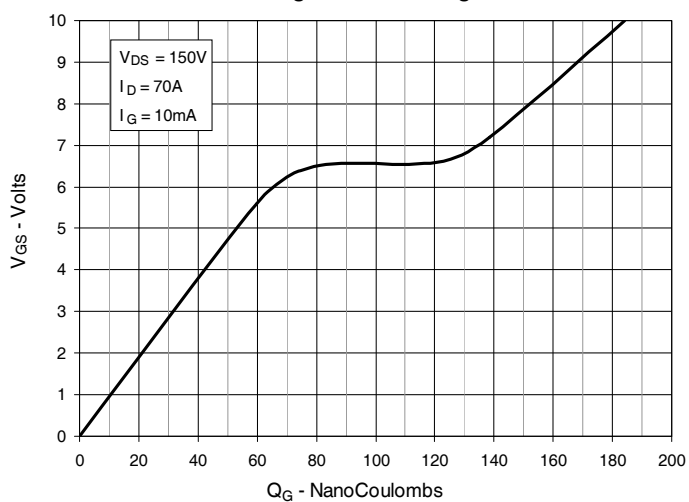
**Fig. 8. Transconductance**



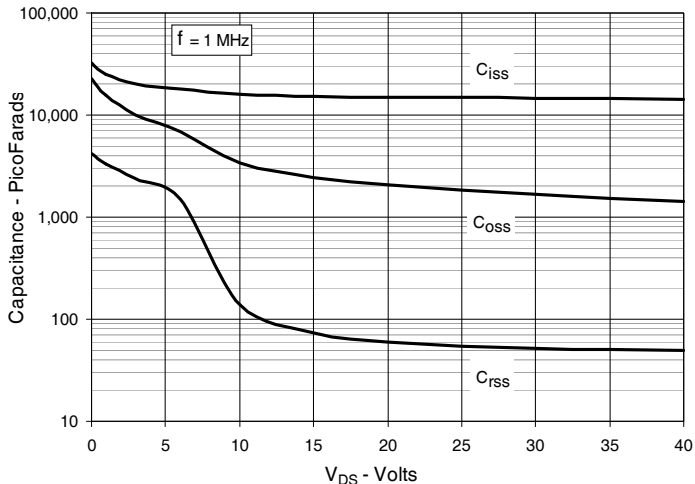
**Fig. 9. Forward Voltage Drop of Intrinsic Diode**



**Fig. 10. Gate Charge**



**Fig. 11. Capacitance**



**Fig. 12. Forward-Bias Safe Operating Area**

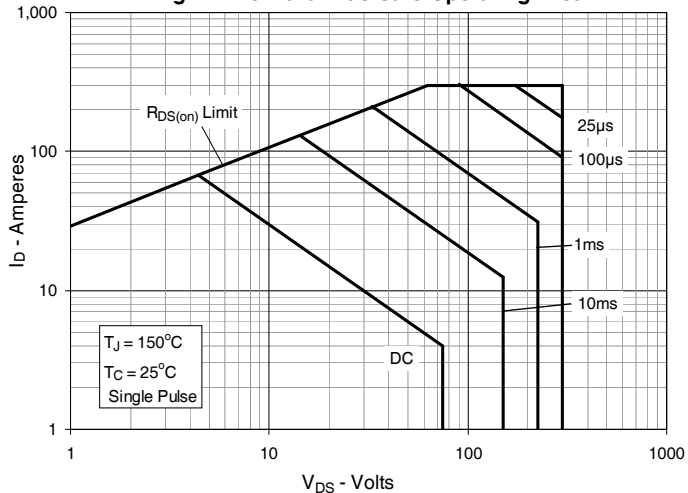
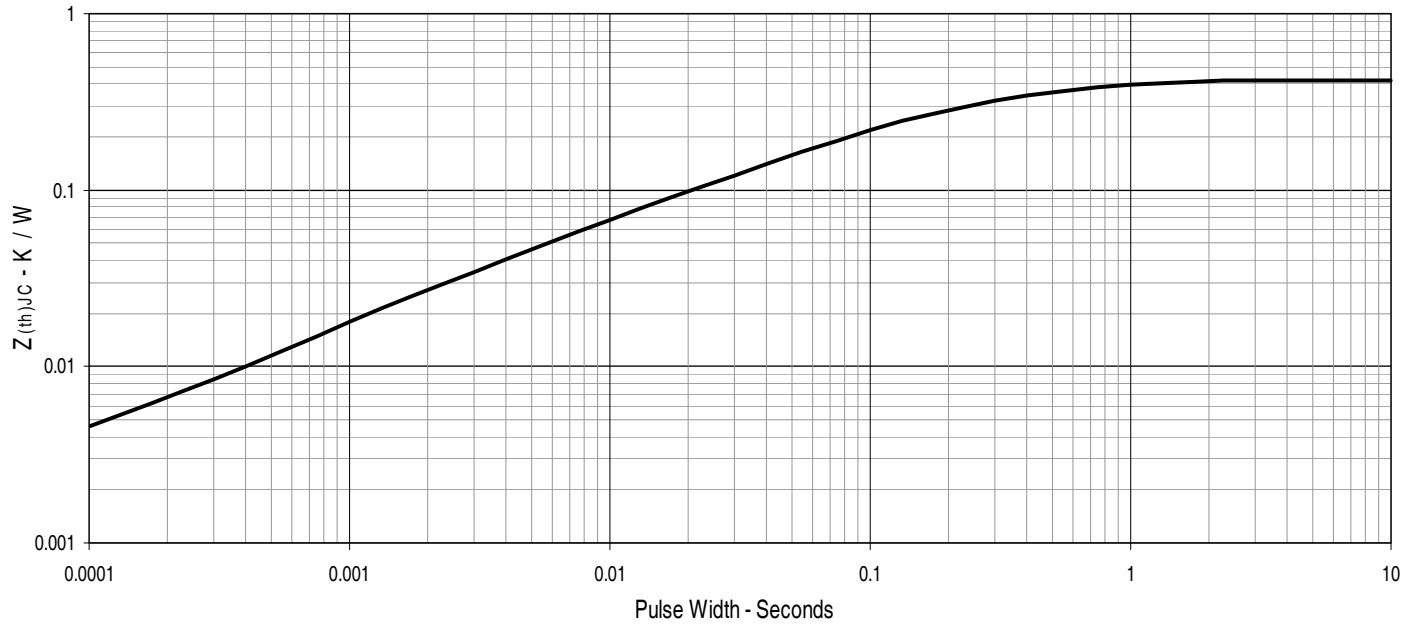


Fig. 13. Maximum Transient Thermal Impedance





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