TL4242-Q1 Adjustable LED Driver

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range for WSON package
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range for TO-263 package
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C3B
- Adjustable Constant Current up to 500 mA (±5%)
- Wide Input-Voltage Range up to 42 V
- Low Dropout Voltage
- Open-Load Detection
- Overtemperature Protection
- Short-Circuit Proof
- Reverse-Polarity Proof

2 Applications

Automotive LED Lighting Applications Including:

- Rear Light
- Daytime Running Light
- Fog Light
- Position Light
- Interior Light
- Stop or Tail Light

3 Description

The TL4242-Q1 device is an integrated adjustable constant-current source, driving loads up to 500 mA. One can adjust the output current level through an external resistor. The device design is for supplying high-power LEDs (for example, OSRAM Dragon LA W57B) under the severe conditions of automotive applications, resulting in constant brightness and extended LED lifetime. The device comes in the DRJ (WSON) and KTT (TO-263) package. Protection circuits prevent damage to the device in case of overload, short-circuit, reverse polarity, and overheat. The device provides the connected LEDs protection against reverse polarity as well as excess voltages up to 45 V.

The integrated PWM input of the TL4242-Q1 device permits LED brightness regulation by pulse-width modulation (PWM). The high-input impedance of the PWM input allows operating the LED driver as a protected high-side switch.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL4242-Q1	TO-263 (7)	10.00 mm × 9.25 mm
	WSON (8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

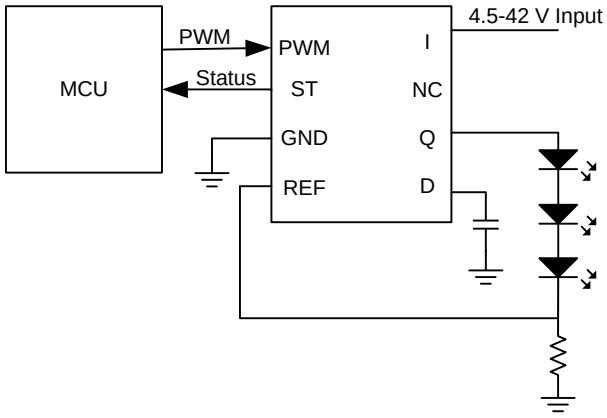


Table of Contents

4 Revision History

Changes from Revision F (January 2015) to Revision G — **Page**

- Changed the pinout drawings ... 4
- Changed all occurrences in the data sheet of QFN and SFM to WSON and TO-263, respectively ... 4
- Changed format of *Pin Functions* table ... 4
- Changed the condition statement for the *Electrical Characteristics* table ... 6
- Added layout diagram for the TO-263 package ... 15
- Added *Receiving Notification of Documentation Updates* and *Community Resources* sections to the data sheet ... 16

Changes from Revision E (July 2013) to Revision F — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (May 2013) to Revision E — **Page**

- Added new graph to Typical Characteristics ... 7

Changes from Revision C (October 2012) to Revision D — **Page**

- Changed minimum storage temperature to –55ºC ... 5

Changes from Revision B (September 2012) to Revision C — **Page**

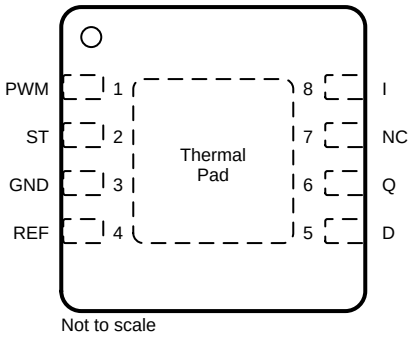
- Added Stoplight and Taillight Application section ... 12
- Added Thermal Considerations section ... 15
- Added PCB Design Guideline section ... 15

Changes from Revision A (August, 2012) to Revision B **Page**

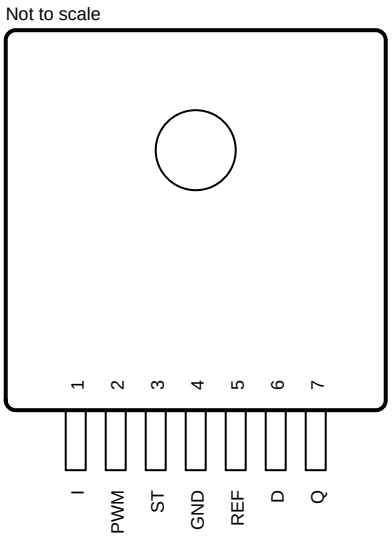
- Manually appended mechanical data, thermal pad data, and package option addendum 11

5 Pin Configuration and Functions

DRJ Package
8-Pin WSON With Exposed Thermal Pad
Top View



KTT Package
7-Pin TO-263 With Exposed Thermal Pad
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DRJ	KTT		
D	5	6	I	Status delay. To set status reaction delay, connect to GND with a capacitor. For no delay, leave open.
GND	3	4	—	Ground
I	8	1	I	Input. Connect directly to GND as close as possible to the device with a 100-nF ceramic capacitor.
NC	7	—	—	No internal connection
PWM	1	2	I	Pulse-width modulation input. If not used, connect to the I pin.
Q	6	7	O	Output
REF	4	5	I	Reference input. Connect to a shunt resistor.
ST	2	3	O	Status output. Open-collector output. Connect to an external pullup resistor (R_{PULLUP} ≥ 4.7 kΩ).
Thermal pad	—	—	—	Solder the thermal pad directly to the PCB. Connect to ground or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(2), V_{CC}		–42	45	V
Input voltage, V_I	D	–0.3	7	V
	PWM	–40	40	
	REF	–1	16	
Output voltage, V_O	Q	–1	41	V
	ST	–0.3	40	
Output current, I_O	PWM		±1	mA
	REF		±2	
	ST		±5	
Virtual-junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
DRJ Package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±1500	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±1000	
			Other pins	±1000	
		Machine model (MM) AEC-Q100 Classification Level M3		±200	
KTT Package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±1500	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1 and 7)	±1000	
			Other pins	±1000	
		Machine model (MM) AEC-Q100 Classification Level M3		±200	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	42	V
V_{ST}	Status (ST) output voltage			16	V
V_{PWM}	PWM voltage		0	40	V
C_D	Status delay (D) capacitance		0	2.2	µF
R_{REF}	Reference (REF) resistor		0	10	Ω
T_A	Operating ambient temperature	WSON	–40	105	°C
		TO-263	–40	125	
T_J	Operating junction temperature		–40	150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TL4242-Q1		UNIT
		DRJ (WSON)	KTT (TO-263)	
		8 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39	31.6	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	31.5	34.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.5	8.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.6	8.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.8	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*

6.5 Electrical Characteristics

over recommended operating ambient temperature range, V_I = 13.5 V, R_{REF} = 0.47 Ω, $V_{PWM,H}$, T_J = –40°C to 150°C, all voltages with respect to ground (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL DEVICE						
I_{qL}	Supply current	V_Q = 6.6 V		12	22	mA
I_{qOFF}	Supply current, off mode	PWM = L, T_J < 85°C		0.1	2	µA
OUTPUT						
I_Q	Output current	$V_Q – V_{REF}$ [1] = 6.6 V	357	376	395	mA
		$V_Q – V_{REF}$ = 6.6 V, R_{REF} = 1 Ω	168	177	185	
		$V_Q – V_{REF}$ = 6.6 V, R_{REF} = 0.39 Ω	431	454	476	
		$V_Q – V_{REF}$ = 5.4 V to 7.8 V, V_I = 9 V to 16 V	357	376	395	
I_{Qmax}	Output current limit	R_{REF} = 0 Ω		600		mA
V_{dr}	Drop voltage	I_Q = 300 mA		0.35	0.7	V
PWM INPUT						
$V_{PWM,H}$	High-level PWM voltage		2.6			V
$V_{PWM,L}$	Low-level PWM voltage				0.7	V
$I_{PWM,H}$	High-level PWM input current	V_{PWM} = 5 V		220	500	µA
$I_{PWM,L}$	Low-level PWM input current	V_{PWM} = 0 V	–1		1	µA
$t_{PWM,ON}$	Delay time, turnon	70% of I_{Qnom}, see Figure 7	0	15	40	µs
$t_{PWM,OFF}$	Delay time, turnoff	30% of I_{Qnom}, see Figure 7	0	15	40	µs
REFERENCE (REF)						
V_{REF}	Reference voltage	R_{REF} = 0.39 Ω to 1 Ω	168	177	185	mV
I_{REF}	Reference input current	V_{REF} = 180 mV	–1	0.1	1	µA
STATUS OUTPUT (ST)						
V_{IQL}	Lower status-switching threshold	ST = L	15	25		mV
V_{IQH}	Upper status-switching threshold	ST = H		30	40	mV
V_{STL}	Low-level status voltage	I_{ST} = 1.5 mA			0.4	V
I_{STLK}	Leakage current	V_{ST} = 5 V			5	µA
STATUS DELAY (D)						
t_{STHL}	Delay time, status reaction	C_D = 47 nF, ST H→L	6	10	14	ms
t_{STLH}	Delay time, status release	C_D = 47 nF, ST L→H		10	20	µs

(1) $V_Q – V_{REF}$ equals the forward voltage sum of the connected LEDs (see *Typical Application Schematic*).

6.6 Typical Characteristics

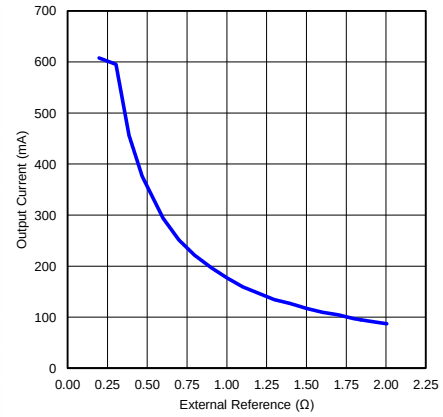


Figure 1. Output Current vs External Resistance

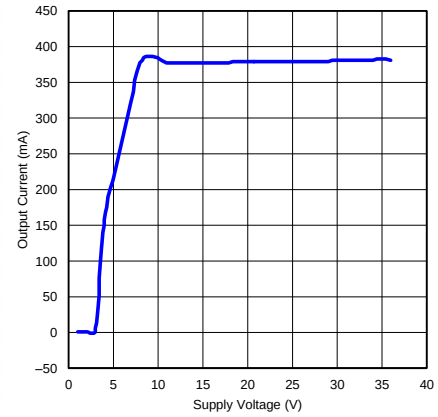


Figure 2. Output Current vs Supply Voltage

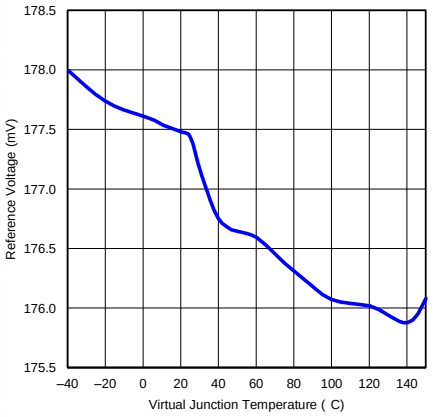


Figure 3. Reference Voltage vs Junction Temperature

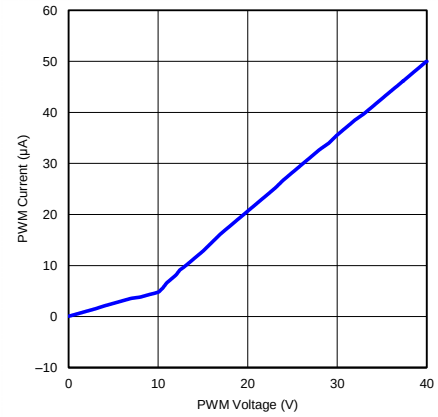


Figure 4. PWM Pin Input Current vs PWM Voltage

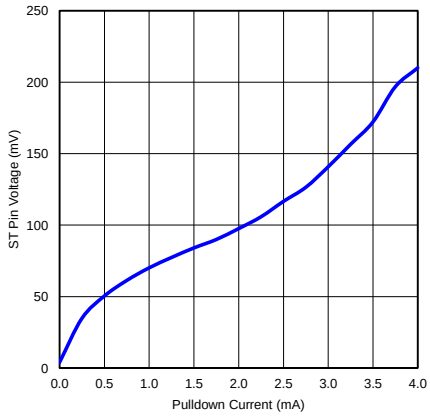


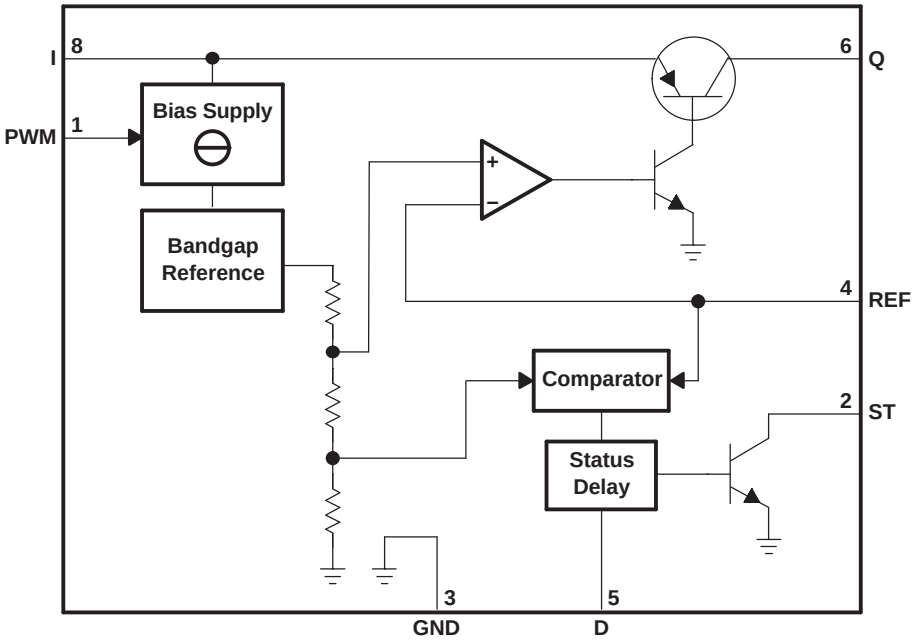
Figure 5. ST Pin Voltage vs ST Pin Pulldown Current

7 Detailed Description

7.1 Overview

The TL4242-Q1 device is an integrated adjustable constant-current source, driving loads up to 500 mA. The current can be set by an external resistor. And the load current can be modulated by a PWM input. The TL4242-Q1 device integrates protections such as open load, overtemperature, and reverse polarity.

7.2 Functional Block Diagram



7.3 Feature Description

The TL4242-Q1 device is an integrated adjustable constant-current source driving loads up to 500 mA. The TL4242-Q1 device is qualified for automotive applications. The output current level can be adjusted via an external resistor. Protection circuits prevent damage to the device in case of overload, short-circuit, reverse polarity, and overtemperature. The connected LEDs are protected against reverse polarity as well as overvoltages up to 45 V. The integrated PWM input of the TL4242-Q1 device permits LED brightness regulation by pulse-width modulation. Due to the high input impedance of the PWM input, the LED driver can be operated as a protected high-side switch.

The external shunt resistor in the ground path of the connected LEDs senses the LED current. A regulation loop holds the voltage drop at the shunt resistor at a constant level of 177 mV (typical). The selection of the shunt resistance, R_{REF}, sets the constant-current level. Calculate the typical output current using Equation 1:

$$I_{Q,typ} = \frac{V_{REF}}{R_{REF}} \quad (1)$$

where V_{REF} is the reference voltage (typically 177 mV) (see *Electrical Characteristics*). The equation applies for R_{REF} = 0.39 Ω to 10 Ω.

The output current is shown as a function of the reference resistance in Equation 1. With the PWM input, one can regulate the LED brightness through the duty cycle. Also, PWM = L sets the TL4242-Q1 device in sleep mode, resulting in a very low current consumption of < 1 μA (typical). The high impedance of the PWM input (see Figure 4) permits the use of the PWM pin as an enable input.

7.4 Device Functional Modes

7.4.1 Pulse-Width Modulation (PWM)

In general applications, PWM can be used to control the TL4242-Q1 device as a high-side driver. High level enables the device. Low level disables the device. In LED lighting, PWM input provides a convenient way to control the brightness of the LED load. Due to the high input impedance of the PWM input, the LED driver can be operated as a protected high-side switch.

7.4.2 Status Output (ST)

The ST pin is an open-collector output. Connect the pin to an external pullup resistor (R_{PULLUP} ≥ 4.7 kΩ). This output provides information of open-load and overtemperature faults.

7.4.3 Reference (REF)

REF is used to set load current. In applications, the load current is sensed by a resistor in series with the load. The voltage on the REF pin is regulated at 177 mV during normal operation. Therefore, the current of the load is determined by V_{REF} / R_{SENSE}.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TL4242-Q1 device is usually used in the automotive lighting applications. A microcontroller is usually used to generate PWM waveform to dimming the LED.

8.2 Typical Applications

8.2.1 Application Circuit

Figure 6 shows a typical application with the TL4242-Q1 LED driver. A supply current adjusted by the R_{REF} resistor drives the three LEDs, preventing brightness variations due to forward voltage spread of the LEDs. An appropriate duty cycle applied to the PWM pin can compensate through software for the luminosity spread arising from the LED production process. Therefore, it is not necessary to select LEDs for forward voltage or luminosity classes. The minimum supply voltage should be equal to or greater than the sum of the LED forward voltages, the TL4242-Q1 drop voltage (maximum 0.7 V at an LED current of 300 mA), and the maximum voltage drop at the shunt resistor R_{REF} of 185 mV.

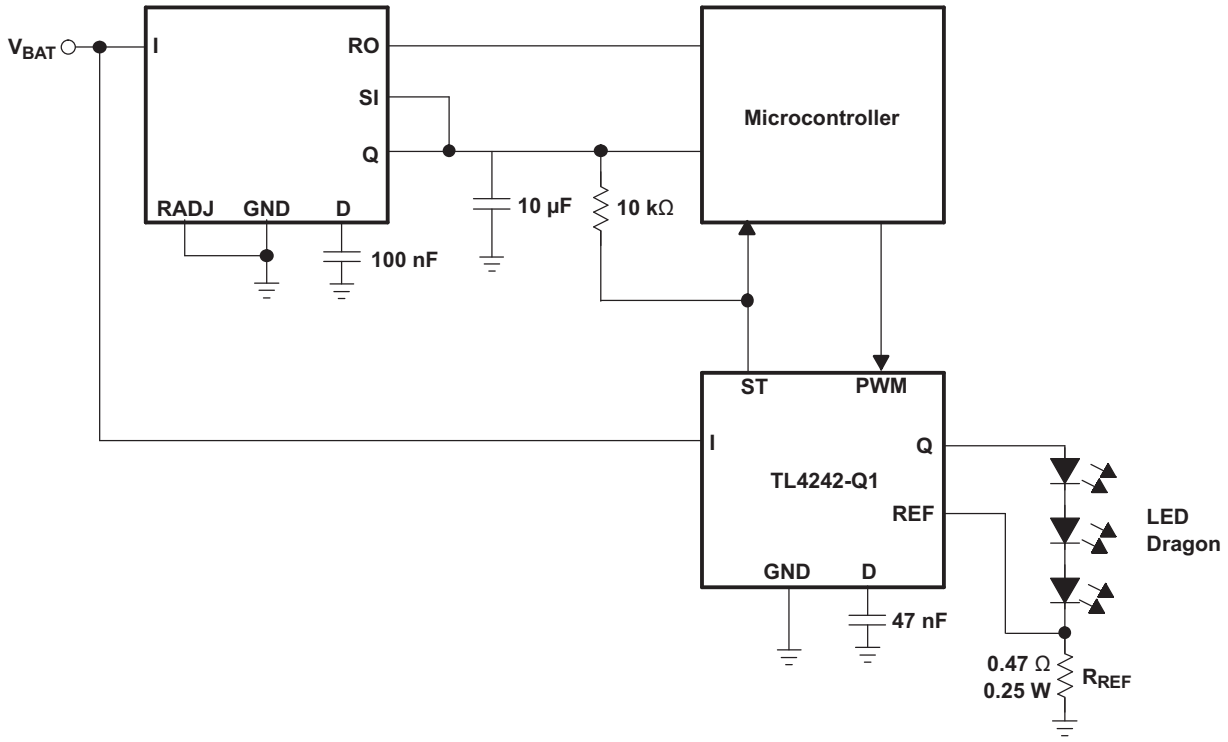


Figure 6. Application Circuit

8.2.1.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
R_{REF}	0.47 Ω

8.2.1.2 Detailed Design Procedure

The status output of the LED driver (ST) detects an open-load condition, enabling supervision of correct LED operation. A voltage drop at the shunt resistor (R_{REF}) below 25 mV (typical) detects an LED failure. In this case, the status output pin (ST) goes low after a delay time adjustable by an optional capacitor connected to pin D.

Figure 7 shows the functionality and timing of ST and PWM. One can adjust the status delay through the capacitor connected to pin D. Delay time scales linearly with the capacitance, C_D:

$$t_{STHL,typ} = \frac{C_D}{47\ nF} \times 10\ ms \quad (2)$$

$$t_{STLH,typ} = \frac{C_D}{47\ nF} \times 10\ \mu s \quad (3)$$

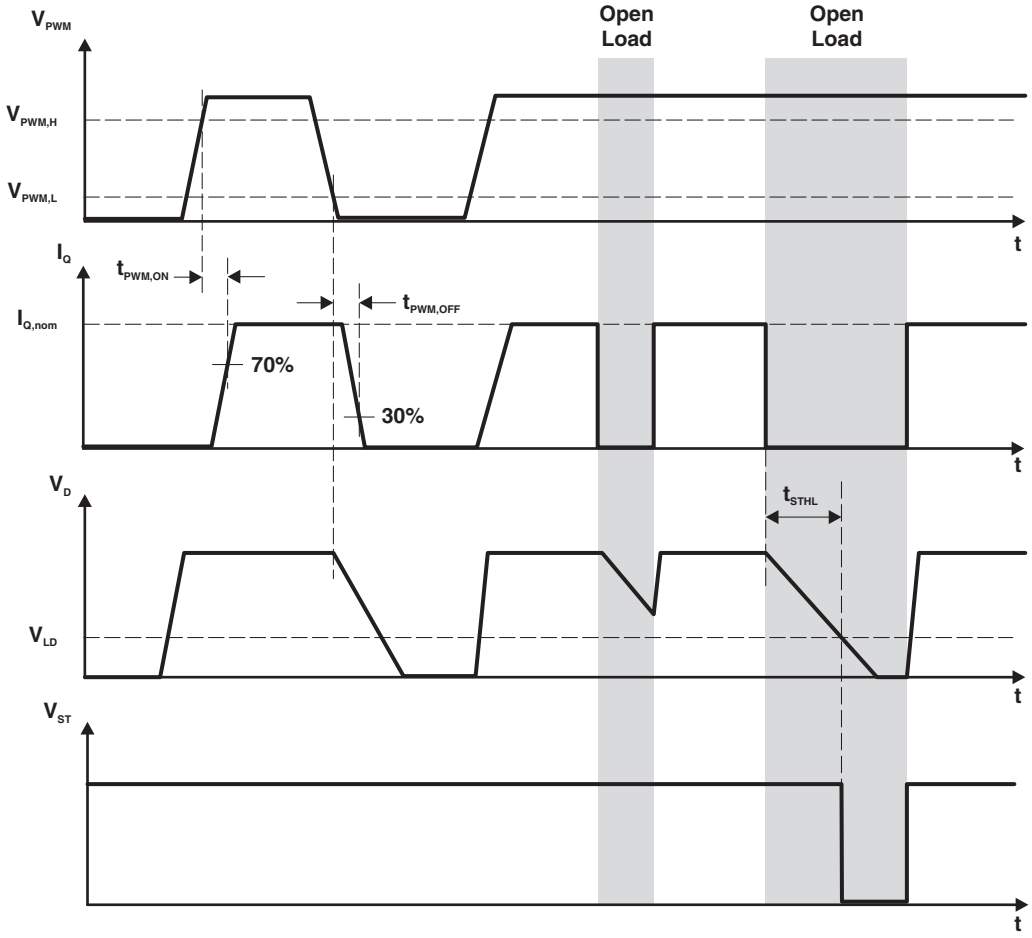


Figure 7. Function and Timing Diagram

8.2.1.3 Application Curves

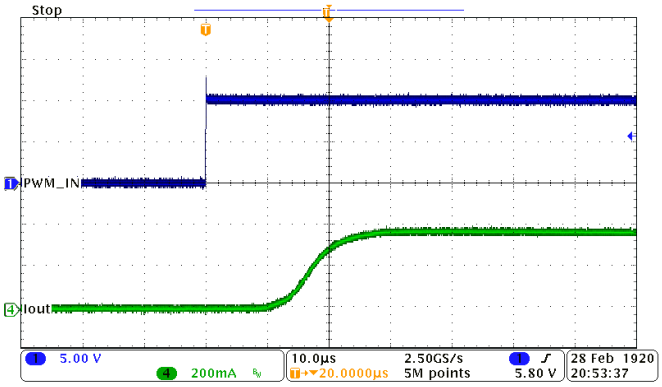


Figure 8. Start-Up Waveform

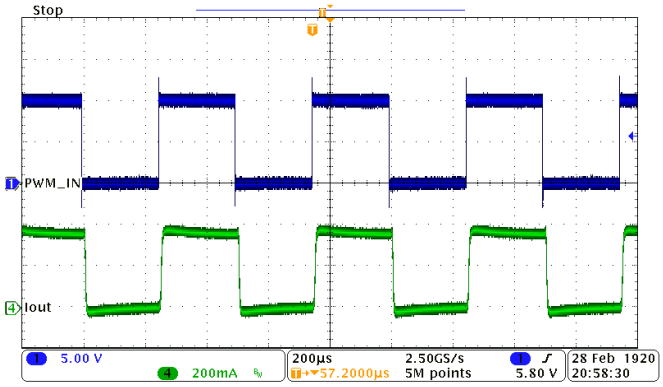


Figure 9. 50% Duty Cycle Waveform

8.2.2 Stoplight and Taillight Application

For many automobiles, the same set of LEDs illuminates both taillights and stop lights. Thus, the LEDs must operate at two different brightness levels, full brightness for the stoplight and 10% to 25% brightness for the taillight. The easiest way to achieve the different brightness is dimming by pulse-width modulation (PWM), which holds the color spectrum of the LED over its whole brightness range. The maximum current that passes through the LED is programmable by sense resistor R_{REF}.

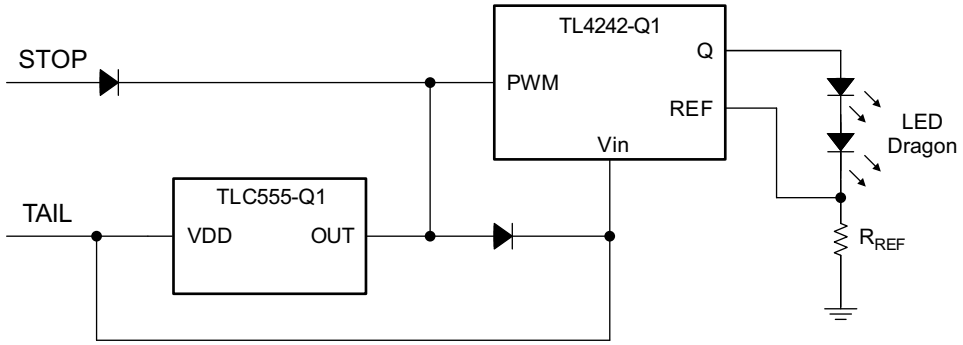


Figure 10. Stoplight and Taillight Application Circuit

8.2.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
R_{REF}	1 Ω

8.2.2.2 Detailed Design Procedure

Obtain the maximum current, I_{Qmax}, that passes through the LEDs by Equation 4:

$$I_{Qmax} = \frac{V_{REF}}{R_{REF}} \quad (4)$$

For example, if R_{REF} equals 1 Ω, as V_{REF} is a fixed value range from 168 mV to 185 mV, I_{Qmax} should be 168 mA to 185 mA.

Figure 10 shows the application circuit of the stoplight and taillight including an automotive-qualified timer, TLC555-Q1, the duty cycle of which is programmable by two external resistors. One can see that driving the STOP signal high pulls the PWM pin constantly high, creating 100% duty cycle. Thus the LEDs operate at full brightness. When the TAIL signal is high, the LEDs operate at 25% brightness because the TLC555-Q1 timer is programmed at a fixed duty cycle of 25%.

8.2.2.3 Application Curves

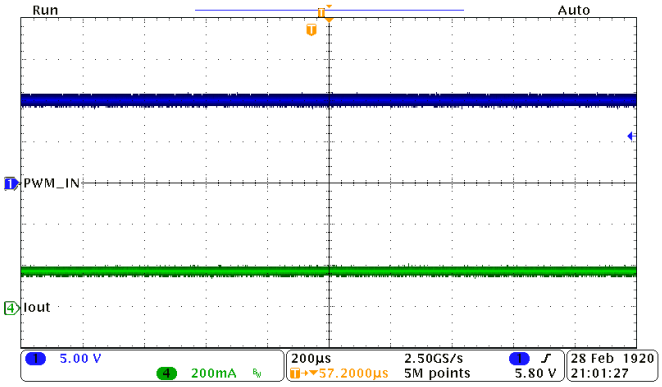


Figure 11. Stoplight Waveform

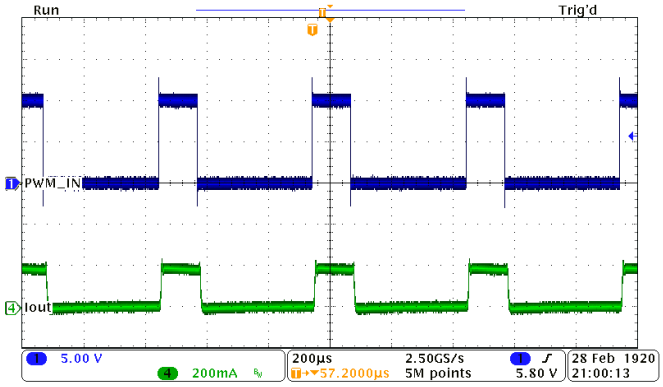


Figure 12. Taillight Waveform

9 Power Supply Recommendations

It is recommended to put a 4.7-µF ceramic capacitor on the input pin. Also a 0.1-µF bypass capacitor can be put at input pin for noise filtering. Input voltage should be between 4.5 V and 42 V.

10 Layout

10.1 Layout Guidelines

In order to prevent thermal shutdown, T_J must be less than 150ºC. If the input voltage is very high, the power dissipation might be large. Currently there is the KTT (TO-263) package which has good thermal impedance, but at the same time, the PCB layout is also very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board, because the major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should be either plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85 percent.

10.2 Layout Example

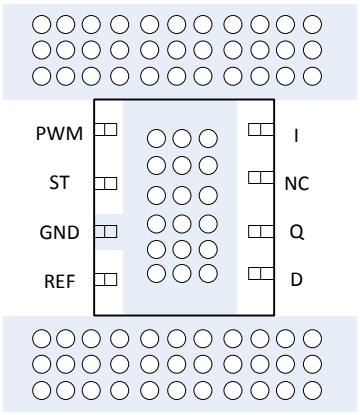


Figure 13. TL4242-Q1 WSON Board Layout Diagram

Layout Example (continued)

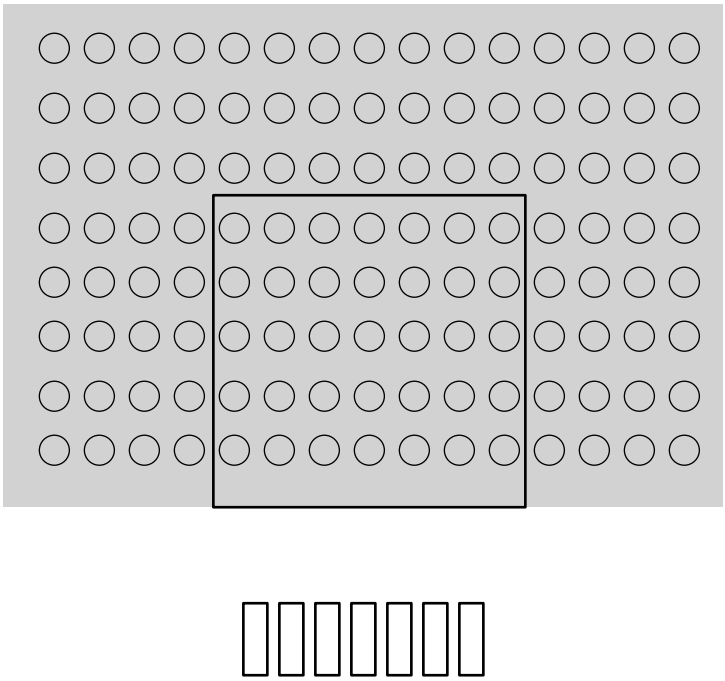


Figure 14. TL4242-Q1 TO-263 Board Layout Diagram

10.3 Thermal Considerations

This device operates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown threshold, the output turns off. When the junction temperature falls below the thermal-shutdown threshold, the output turns on again.

Calculate the power dissipated by the device according to Equation 5:

$$P = (V_I - V_O) \times I_O + V_I \times I_Q \quad (5)$$

In the formula, V_I represents the input voltage of the device, V_O stands for the output voltage, I_O means the output current of the LEDs, and I_Q is the quiescent current dissipated by the device. The very small value of I_Q sometimes allows one to neglect it.

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P \quad (6)$$

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL4242QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	7	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TL4242Q	Samples
TL4242TDRJRQ1	ACTIVE	SON	DRJ	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	4242T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL4242-Q1 :

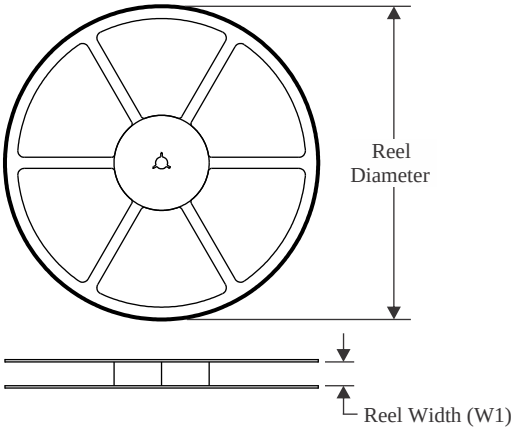
- Catalog: TL4242

NOTE: Qualified Version Definitions:

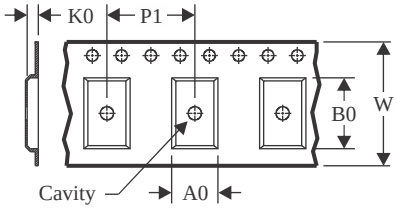
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

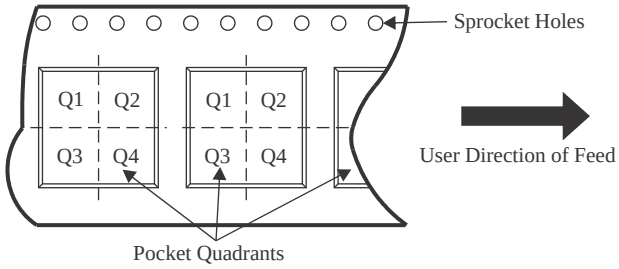


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

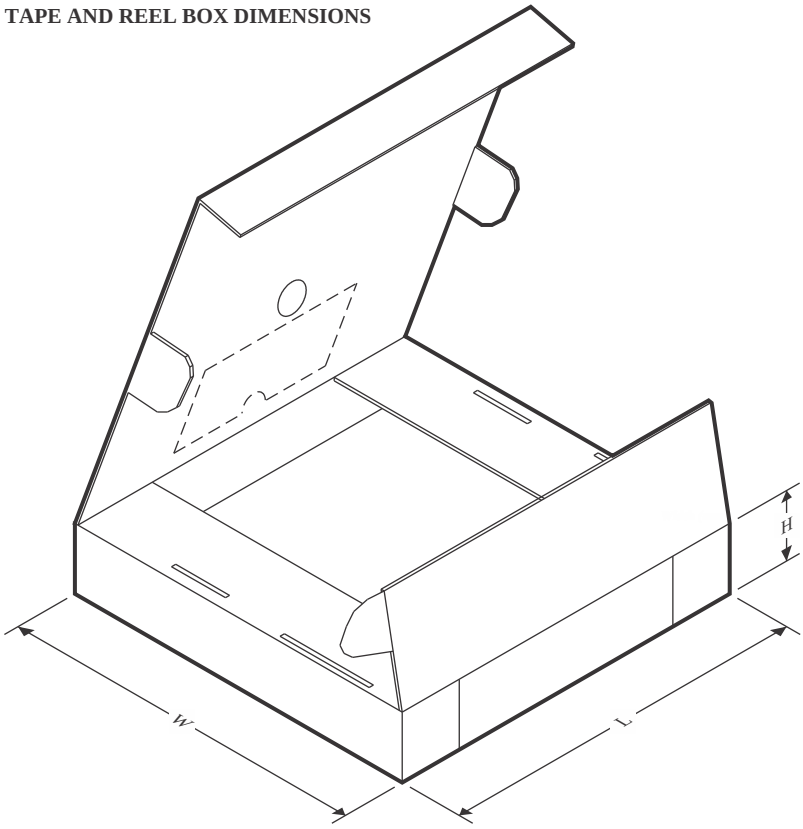
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4242QKTTRQ1	DDPAK/ TO-263	KTT	7	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL4242TDRJRQ1	SON	DRJ	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

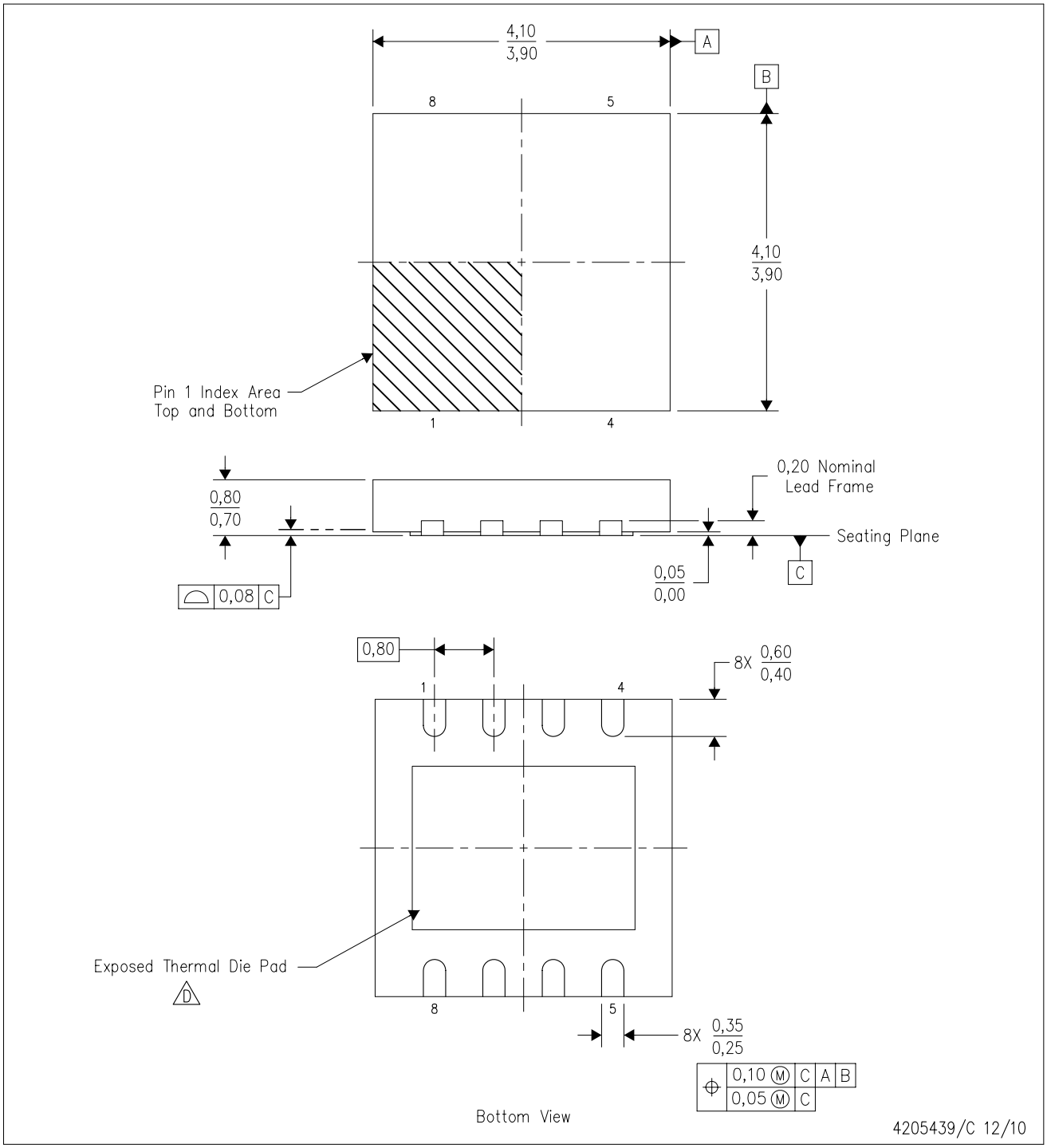
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4242QKTTRQ1	DDPAK/TO-263	KTT	7	500	340.0	340.0	38.0
TL4242TDRJRQ1	SON	DRJ	8	3000	356.0	356.0	35.0

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

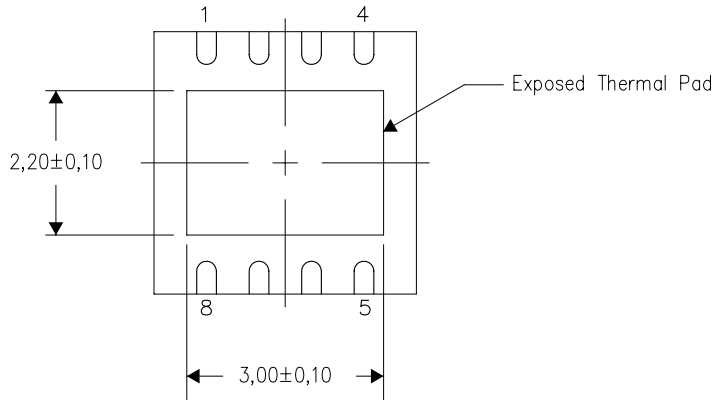
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



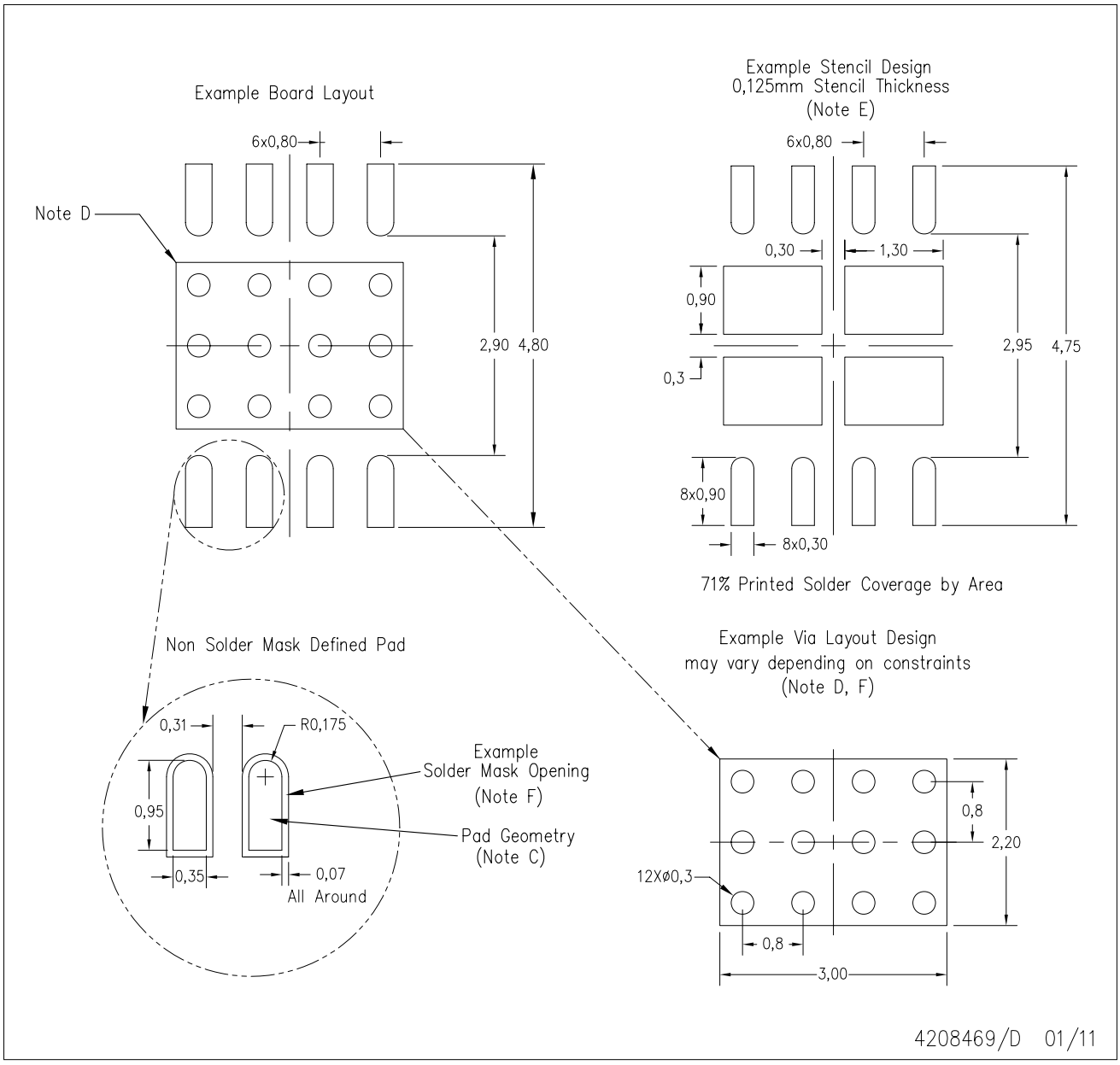
Bottom View

Exposed Thermal Pad Dimensions

4206882/F 01/11

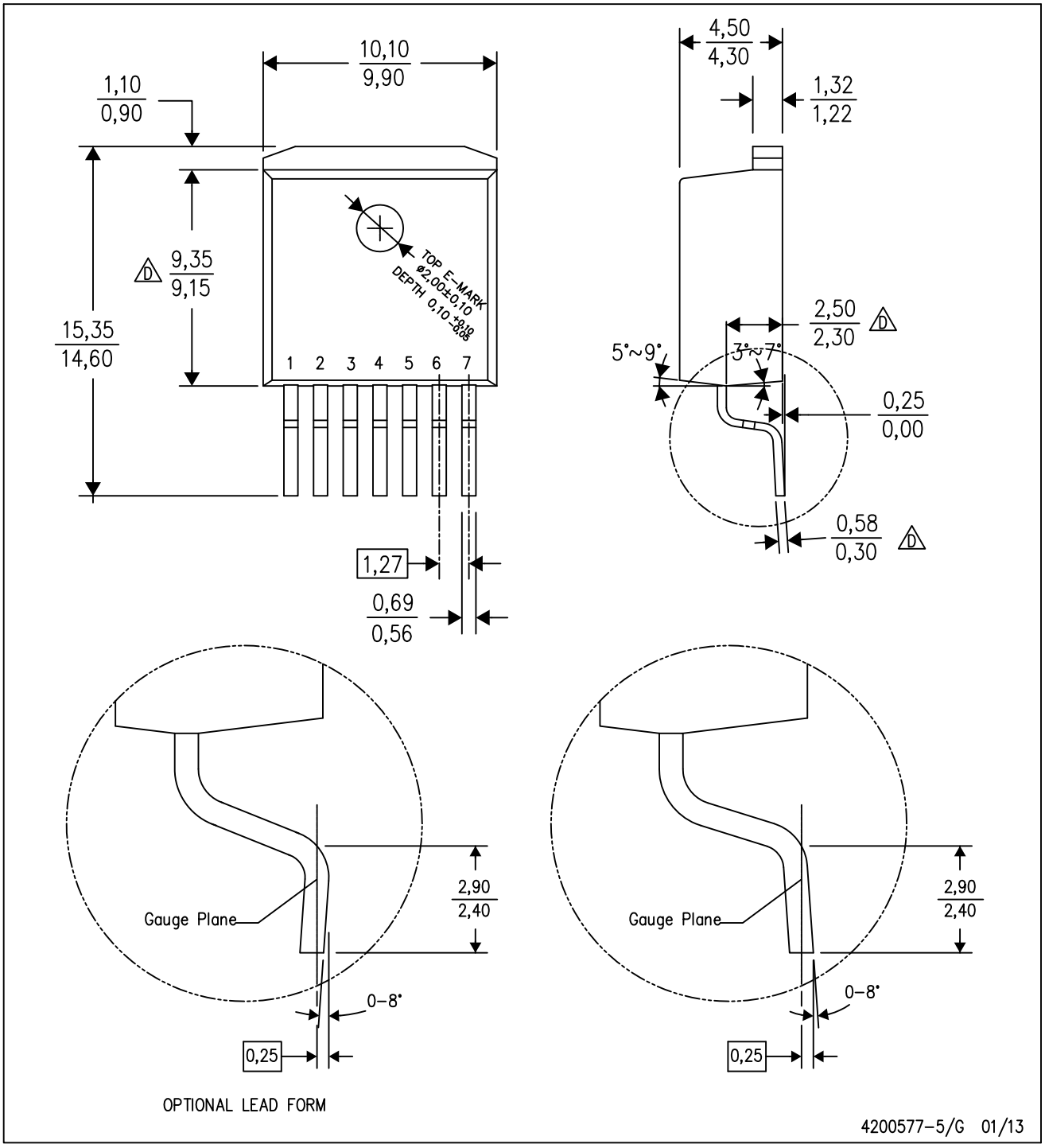
NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



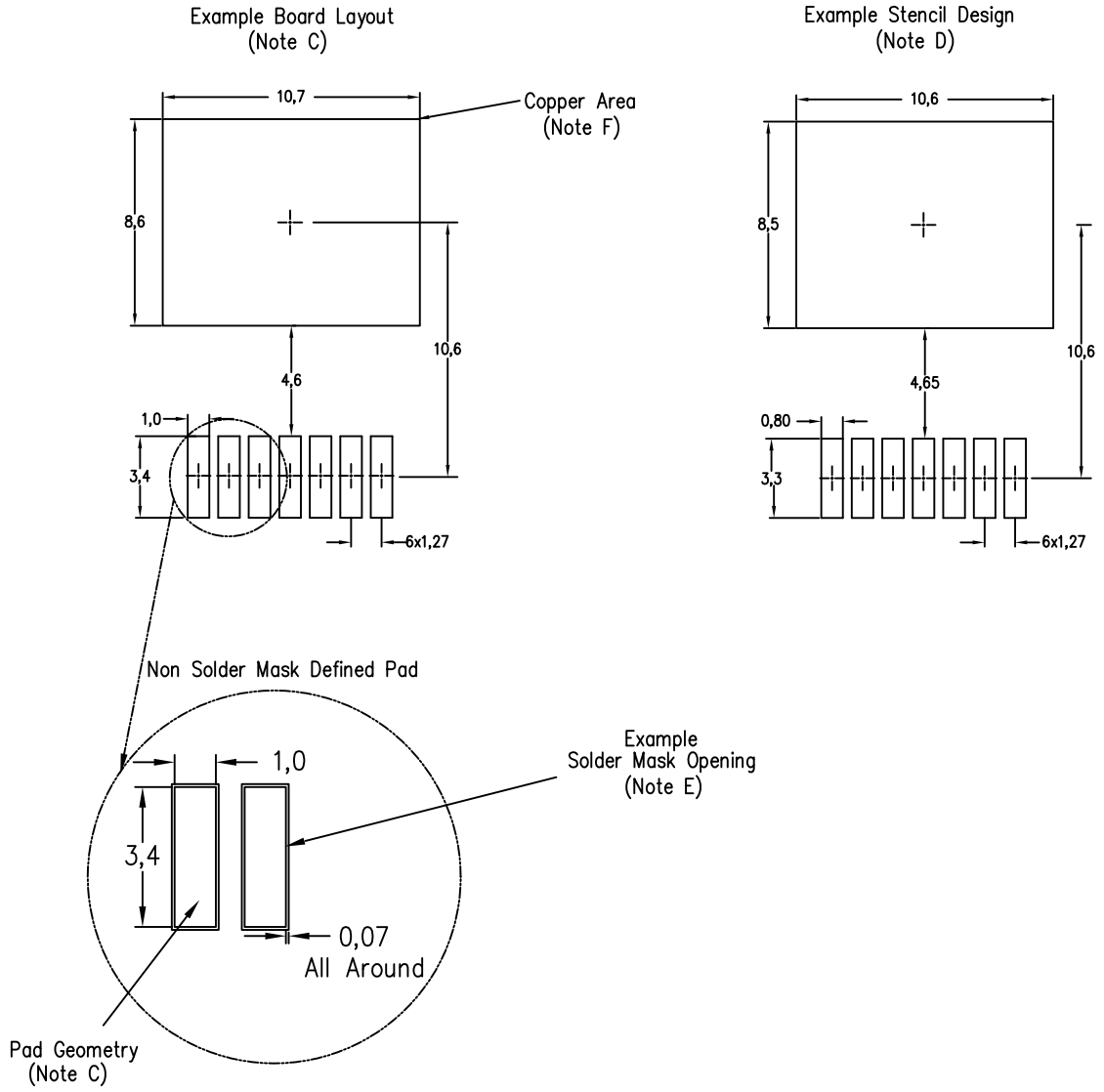
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

KTT (R–PSFM–G7) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0,13 per side.
D. Falls within JEDEC TO–263 AB.

KTT (R–PSFM–G7) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265