# ISL12032 Real Time Clock with 50/60 Hz clock and Crystal Backup

Low Power RTC with Battery Backed SRAM and 50/60 Cycle AC Input and Crystal Back-up

FN6618
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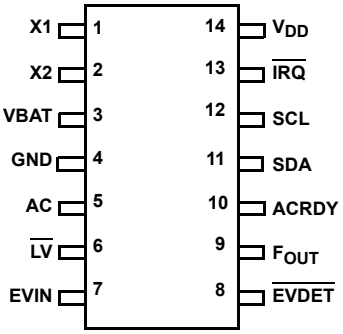
The ISL12032 device is a low power real time clock with 50/60 AC input for timing synchronization. It also has an oscillator utilizing an external crystal for timing back-up, clock/calendar registers, intelligent battery back-up switching, battery voltage monitor, brownout indicator, integrated trickle charger for super capacitor, single periodic or polled alarms, POR supervisory function, and up to 4 Event Detect with time stamp. There are 128 bytes of battery-backed user SRAM.

The oscillator uses a 50/60 cycle sine wave input, backed by an external, low-cost, 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The calendar registers contain the date, month, year, and day of the week. The calendar is accurate through year 2100, with automatic leap year correction and auto daylight savings correction.

## Pinout

**ISL12032**
**(14 LD TSSOP)**
TOP VIEW




## Features

- 50/60 Cycle AC as a Primary Clock Input for RTC Timing
- Redundant Crystal Clock Input Selectable by User
  - Dynamically Switch from AC Clock Input to Crystal in Case of Power Failure
- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, Seconds and Tenths of a Second
  - Day of the Week, Day, Month, and Year
- Auto Daylight Saving Time Correction
  - Programmable Forward and Backward Dates
- Security and Event Functions
  - Event Detection with Time Stamp
  - Stores First and Last Three Event Time Stamps
- Separate $F_{OUT}$ Pin
  - 7 Selectable Frequency Outputs
- Dual Alarms with Hardware and Register Indicators
  - Hardware Single Event or Pulse Interrupt Mode
- Automatic Backup to Battery or Super Capacitor
  - VBAT Operation Down to 1.8V
  - 1.0µA Battery Supply Current
- Two Battery Status Monitors with Selectable Levels
  - Seven Selectable Voltages for Each Level
  - 1st Level, Trip Points from 4.675V to 2.125V
  - 2nd Level, Trip Points from 4.125V to 1.875V
- $V_{DD}$ Power Brownout Monitor
  - Six Selectable Trip Levels, from 4.675V to 2.295V
- Time Stamp during Power-to-Battery and Battery-to-Power Switchover
- Integrated Trickle Charger
  - Four Selectable Charging Rates
- 128 Bytes Battery-Backed User SRAM
- $I^2C$ Interface
  - 400kHz Data Transfer Rate
- Pb-free (RoHS compliant)

## Applications

- Utility Meters
- Control Applications
- Security Related Applications
- Vending Machines
- White Goods
- Consumer Electronics

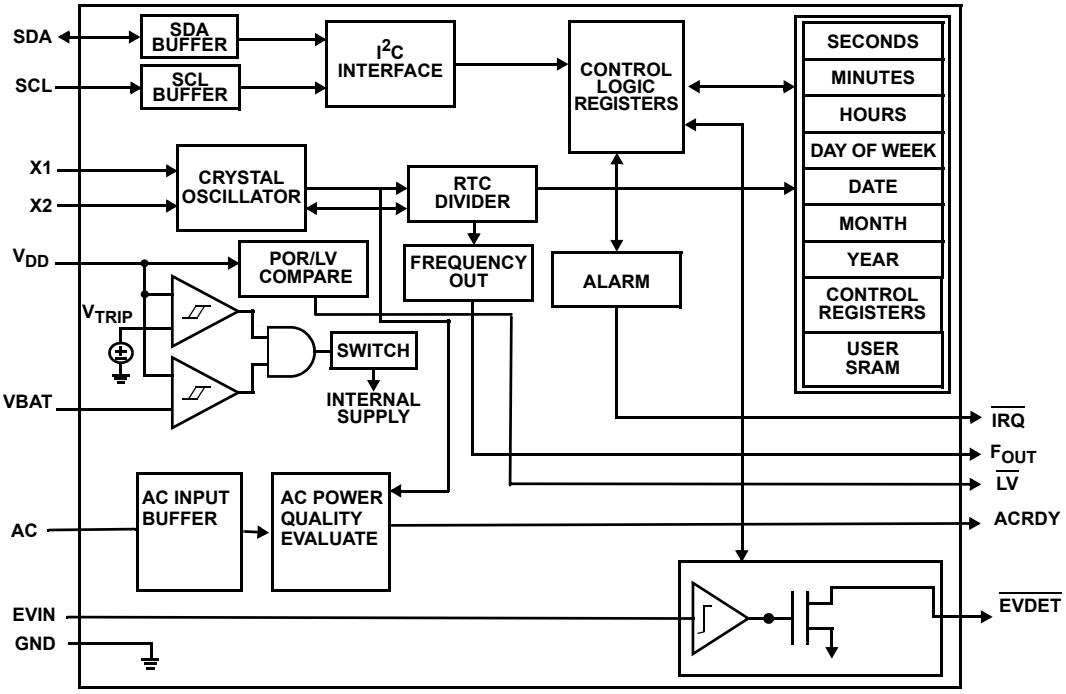
## Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | $V_{DD}$ RANGE | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG DWG # |
|---|---|---|---|---|---|
| ISL12032IVZ | 12032 IVZ | 2.7V to 5.5V | -40 to +85 | 14 Ld TSSOP | M14.173 |

NOTE:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL12032. For more information on MSL please see techbrief TB363.

## Block Diagram



## *Functional Pin Descriptions*

| PIN NUMBER | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | X1 | The input of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X1 also can be driven directly from a 32.768kHz source with no crystal connected. |
| 2 | X2 | The output of an inverting amplifier and is intended to be connected to one pin of an external 32.768kHz quartz crystal. X2 should be left open when X1 is driven from an external source. |
| 3 | VBAT | **Battery Voltage**. This pin provides a backup supply voltage to the device. VBAT supplies power to the device in the event that the $V_{DD}$ supply fails. This pin should be tied to ground if not used. |
| 4 | GND | **Ground**. |
| 5 | AC | **AC Input**. The AC input pin accepts either 50Hz of 60Hz AC $2.5V_{P-P}$ sine wave signal. |
| 6 | $\overline{LV}$ | **Low Voltage** detection output/Brownout Alarm. Open drain active low output. |
| 7 | EVIN | **Event Input** - The EVIN is a logic input pin that is used to detect an externally monitored event. When a high signal is present at the EVIN pin, an “event” is detected. |
| 8 | $\overline{EVDET}$ | **Event Detect Output.** Active when EVIN is triggered. Open Drain active low output. |
| 9 | $F_{OUT}$ | **Frequency Output.** Register selectable frequency clock output. CMOS output levels. |
| 10 | ACRDY | **AC Ready**. Open Drain output. When High, AC input signal is qualified for timing use. |
| 11 | SDA | **Serial Data**. SDA is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR’ed with other open drain or open collector outputs. |
| 12 | SCL | **Serial Clock**. The SCL input is used to clock all serial data into and out of the device. |
| 13 | $\overline{IRQ}$ | **Interrupt Output.** Open Drain active low output. Interrupt output pin to indicate alarm is triggered. |
| 14 | $V_{DD}$ | Power supply. |

## Absolute Maximum Ratings

Voltage on $V_{DD}$, VBAT, SCL, SDA, ACRDY, AC, $\overline{LV}$, $\overline{EVDET}$, EVIN, $\overline{IRQ}$, $F_{OUT}$ pins
(respect to ground) . . . . . -0.3V to 6.0V
Voltage on X1 and X2 pins
(respect to ground) . . . . . -0.3V to 2.5V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3014) . . . . . >2kV
Machine Model . . . . . >200V

## Thermal Information

Thermal Resistance (Typical, Note 4) $\theta_{JA}$ (°C/W)
14 Ld TSSOP . . . . . 110
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

Temperature ($T_A$) . . . . . -40°C to +85°C
Supply Voltage ($V_{DD}$) . . . . . 2.7V to 5.5V
Supply Voltage (VBAT) . . . . . 1.8V to 5.5V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTE:

4. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## DC Operating Characteristics

Specifications apply for: $V_{DD}$ = 2.7V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C**.

| SYMBOL | PARAMETER | CONDITIONS | MIN (Note 13) | TYP (Note 7) | MAX (Note 13) | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Main Power Supply | | **2.7** | | **5.5** | V | |
| VBAT | Battery Supply Voltage | | **1.8** | | **5.5** | V | |
| $I_{DD1}$ | Supply Current | $V_{DD}$ = 5V, SCL, SDA = $V_{DD}$ | | 27 | **60** | µA | 6 |
| | | $V_{DD}$ = 3V, SCL, SDA = $V_{DD}$ | | 16 | **45** | µA | 6 |
| $I_{DD2}$ | Supply Current ($I^2C$ Communications Active) | $V_{DD}$ = 5V | | 43 | **75** | µA | 5, 8 |
| $I_{DD3}$ | Supply Current for Timekeeping at AC Input | $V_{DD}$ = 5.5V at $T_A$ = +25°C, $F_{OUT}$ disabled | | 9.0 | 18.0 | µA | 5, 6 |
| IBAT | Battery Supply Current | VBAT = 5.5V at $T_A$ = +25°C | | 1.0 | 1.8 | µA | 5, 11 |
| | | VBAT = 2.7V | | 0.8 | **1.2** | | 5, 11 |
| | | VBAT = 1.8V | | 0.7 | **1.0** | µA | 5, 11 |
| $IBAT_{LKG}$ | Battery Input Leakage | $V_{DD}$ = 5.5V, VBAT = 1.8V TRKEN = 0 | | | **100** | nA | |
| $I_{LI}$ | Input Leakage Current on SCL | | | | **1** | µA | |
| $I_{LO}$ | I/O Leakage Current on SDA | | | | **1** | µA | |
| $VBAT_M$ | Battery Level Monitor Threshold | $V_{DD}$ = 5.5V, VBAT = 1.8V | **-150** | | **+150** | mV | |
| $V_{PBM}$ | Brownout Level Monitor Threshold | | **-150** | | **+150** | mV | |
| $V_{TRIP}$ | VBAT Mode Threshold | | **2.0** | 2.2 | **2.4** | V | |
| $V_{TRIPHYS}$ | $V_{TRIP}$ Hysteresis | | | 30 | | mV | |
| $VBAT_{HYS}$ | VBAT Hysteresis | | | 50 | | mV | |
| RTRK | Trickle Charge Resistance | $V_{DD}$ = 5.5V, VBAT = 3.0V, TRKR01 = 0, TRKR00 = 0 | | 1300 | | Ω | |
| | | $V_{DD}$ = 5.5V, VBAT = 3.0V, TRKR01 = 0, TRKR00 = 1 | | 2200 | | Ω | |
| | | $V_{DD}$ = 5.5V, VBAT = 3.0V, TRKR01 = 1, TRKR00 = 0 | | 3600 | | Ω | |
| | | $V_{DD}$ = 5.5V, VBAT = 3.0V, TRKR01 = 1, TRKR00 = 1 | | 7800 | | Ω | |
| VTRKTERM | VBAT Charging Termination Point | | | VDD - 50mV | | V | |

**DC Operating Characteristics** Specifications apply for: $V_{DD}$ = 2.7V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| SYMBOL | PARAMETER | CONDITIONS | MIN (Note 13) | TYP (Note 7) | MAX (Note 13) | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| VTRKHYS | Trickle Charge ON-OFF Hysteresis | | | 50 | | mV | |
| **$\overline{IRQ}$/ACRDY/LV/$\overline{EVDET}$ (OPEN DRAIN OUTPUTS)** | | | | | | | |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$ = 5V, $I_{OL}$ = 3mA | | | **0.4** | V | |
| | | $V_{DD}$ = 2.7V, $I_{OL}$ = 1mA | | | **0.4** | V | |
| **$F_{OUT}$ (CMOS OUTPUT)** | | | | | | | |
| $V_{OL}$ | Output Low Voltage | $I_{OH}$ = 1mA | | | **0.3 x $V_{DD}$** | V | |
| $V_{OH}$ | Output High Voltage | | **0.7 x $V_{DD}$** | | | V | |
| **EVIN** | | | | | | | |
| $I_{EVPU}$ | EVIN Pull-up Current | $V_{DD}$ = 5.5V, VBAT = 3.0V | **1.0** | 3.0 | **8.0** | µA | |
| | | $V_{DD}$ = 0V, VBAT = 1.8V | **100** | | **600** | nA | |
| $V_{IL}$ | Input Low Voltage | | | | **0.3 x $V_{DD}$** | V | |
| $V_{IH}$ | Input High Voltage | | **0.7 x $V_{DD}$** | | | V | |
| $I_{EVPD}$ | EVIN Disabled Pull-down Current | $V_{DD}$ = 5.5V | | 200 | | nA | |

**Power-Down Timing** Specifications apply for: $V_{DD}$ = 2.7V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C**.

| SYMBOL | PARAMETER | CONDITIONS | MIN (Note 13) | TYP (Note 7) | MAX (Note 13) | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{DD\ SR-}$ | $V_{DD}$ Negative Slew Rate | | | | **10** | V/ms | 9 |

**$I^2C$ Interface Specifications** Specifications apply for: $V_{DD}$ = 2.7V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C**.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 13) | TYP (Note 7) | MAX (Note 13) | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | SDA and SCL Input Buffer LOW Voltage | | **-0.3** | | **0.3 x $V_{DD}$** | V | |
| $V_{IH}$ | SDA and SCL Input Buffer HIGH Voltage | | **0.7 x $V_{DD}$** | | **$V_{DD}$ + 0.3** | V | |
| Hysteresis | SDA and SCL Input Buffer Hysteresis | | **0.05 x $V_{DD}$** | | | V | |
| $V_{OL}$ | SDA Output Buffer LOW Voltage, Sinking 3mA | $V_{DD}$ = 5V, $I_{OL}$ = 3mA | | | **0.4** | V | |
| $C_{PIN}$ | SDA and SCL Pin Capacitance | $T_A$ = +25°C, f = 1MHz, $V_{DD}$ = 5V, $V_{IN}$ = 0V, $V_{OUT}$ = 0V | | 10 | | pF | |
| $f_{SCL}$ | SCL Frequency | | | | **400** | kHz | |
| $t_{IN}$ | Pulse Width Suppression Time at SDA and SCL Inputs | Any pulse narrower than the max spec is suppressed. | | | **50** | ns | |
| $t_{AA}$ | SCL Falling Edge to SDA Output Data Valid | SCL falling edge crossing 30% of $V_{DD}$, until SDA exits the 30% to 70% of $V_{DD}$ window. | | | **900** | ns | |
| $t_{BUF}$ | Time the Bus Must be Free Before the Start of a New Transmission | SDA crossing 70% of $V_{DD}$ during a STOP condition, to SDA crossing 70% of $V_{DD}$ during the following START condition. | **1300** | | | ns | |

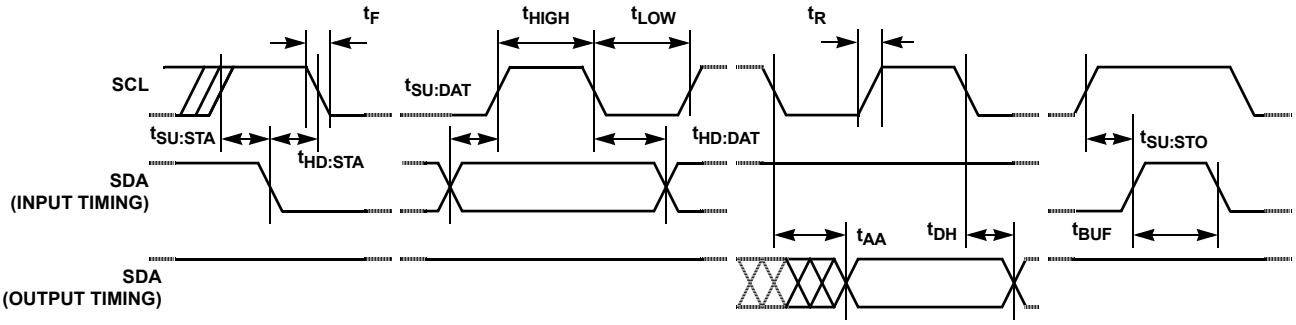
**$I^2C$ Interface Specifications** Specifications apply for: $V_{DD}$ = 2.7V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 13) | TYP (Note 7) | MAX (Note 13) | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $t_{LOW}$ | Clock LOW Time | Measured at the 30% of $V_{DD}$ crossing. | **1300** | | | ns | |
| $t_{HIGH}$ | Clock HIGH Time | Measured at the 70% of $V_{DD}$ crossing. | **600** | | | ns | |
| $t_{SU:STA}$ | START Condition Setup Time | SCL rising edge to SDA falling edge. Both crossing 70% of $V_{DD}$. | **600** | | | ns | |
| $t_{HD:STA}$ | START Condition Hold Time | From SDA falling edge crossing 30% of $V_{DD}$ to SCL falling edge crossing 70% of $V_{DD}$. | **600** | | | ns | |
| $t_{SU:DAT}$ | Input Data Setup Time | From SDA exiting the 30% to 70% of $V_{DD}$ window, to SCL rising edge crossing 30% of $V_{DD}$. | **100** | | | ns | |
| $t_{HD:DAT}$ | Input Data Hold Time | From SCL falling edge crossing 30% of $V_{DD}$ to SDA entering the 30% to 70% of $V_{DD}$ window. | **0** | | **900** | ns | |
| $t_{SU:STO}$ | STOP Condition Setup Time | From SCL rising edge crossing 70% of $V_{DD}$, to SDA rising edge crossing 30% of $V_{DD}$. | **600** | | | ns | |
| $t_{HD:STO}$ | STOP Condition Hold Time | From SDA rising edge to SCL falling edge. Both crossing 70% of $V_{DD}$. | **600** | | | ns | |
| $t_{DH}$ | Output Data Hold Time | From SCL falling edge crossing 30% of $V_{DD}$, until SDA enters the 30% to 70% of $V_{DD}$ window. | **0** | | | ns | |
| $t_R$ | SDA and SCL Rise Time | From 30% to 70% of $V_{DD}$. | **20 + 0.1 x Cb** | | **300** | ns | 10, 12 |
| $t_F$ | SDA and SCL Fall Time | From 70% to 30% of $V_{DD}$. | **20 + 0.1 x Cb** | | **300** | ns | 10, 12 |
| Cb | Capacitive loading of SDA or SCL | Total on-chip and off-chip | **10** | | **400** | pF | 10, 12 |
| $R_{PU}$ | SDA and SCL Bus Pull-up Resistor Off-chip | Maximum is determined by $t_R$ and $t_F$.<br>For Cb = 400pF, max is about 2kΩ.<br>For Cb = 40pF, max is about 15kΩ | **1** | | | kΩ | 10, 12 |

NOTES:

5. $\overline{IRQ}$ and $F_{OUT}$ Inactive.
6. $V_{DD}$ > VBAT +$V_{BATHYS}$
7. Specified at $T_A$ =+25°C.
8. $F_{SCL}$ = 400kHz.
9. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
10. Parameter is not 100% tested.
11. $V_{DD}$ = 0V. $I_{BAT}$ increases at $V_{DD}$ voltages between 0.5V and 1.5V.
12. These are $I^2C$ specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
13. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

## SDA vs SCL Timing




## Symbol Table

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

**EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR $V_{DD}$ = 5V**

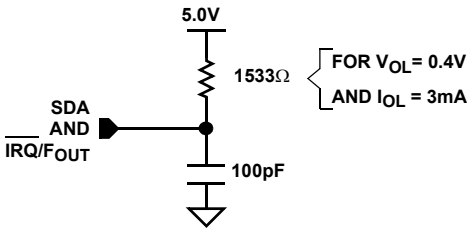



**FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH $V_{DD}$ = 5.0V**

## General Description

The ISL12032 device is a low power real time clock with 50/60 AC input for timing synchronization. It also has an oscillator utilizing an external crystal for timing back-up, clock/calendar registers, intelligent battery back-up switching, battery voltage monitor, brownout indicator, integrated trickle charger for super capacitor, single periodic or polled alarms, POR supervisory function, and up to 4 Event Detect with time stamp. There are 128 bytes of battery-backed user SRAM.

The oscillator uses a 50/60 cycle sine wave input, backed by an external, low-cost, 32.768kHz crystal. The real time clock tracks time with separate registers for hours, minutes, and seconds. The calendar registers contain the date, month, year, and day of the week. The calendar is accurate through year 2100, with automatic leap year correction and auto daylight savings correction.

The ISL12032's alarm can be set to any clock/calendar value for a match. Each alarm's status is available by checking the Status Register. The device also can be configured to provide a hardware interrupt via the $\overline{IRQ}$ pin. There is a repeat mode for the alarms allowing a periodic interrupt every minute, every hour, every day, etc.

The device also offers a backup power input pin. This VBAT pin allows the device to be backed up by battery or Super Capacitor with automatic switchover from $V_{DD}$ to VBAT. The ISL12032 devices are specified for $V_{DD}$ = 2.7V to 5.5V and the clock/calendar portion of the device remains fully operational in battery backup mode down to 1.8V (Standby Mode). The VBAT level is monitored and warnings are reported against preselected levels. The first report is registered when the VBAT level falls below 85% of nominal level, the second level is set for 75% of nominal level. Battery levels are stored in the PWRBAT registers.

The ISL12032 offers a "Brownout" alarm once the $V_{DD}$ falls below a pre-selected trip level. In the ISL12032, this allows the system microcontroller to save vital information to memory before complete power loss. There are six $V_{DD}$ trip levels for the brownout alarm.

The event detection function accepts a normally low logic input, and when triggered will store the time/date information for the event. The first event is stored in the memory until reset; subsequent events are stored on-chip memory and the last 3 events are retained and accessible by performing an indexed register read.

## Pin Descriptions

### X1, X2

The X1 and X2 pins are the input and output, respectively, of an inverting amplifier. An external 32.768kHz quartz crystal is used with the device to supply a backup timebase for the real time clock if there is no AC input. The device also can be driven directly from a 32.768kHz source at pin X1, in which case, pin X2 should be left unconnected. No external load capacitors are needed for the X1 and X2 pins.

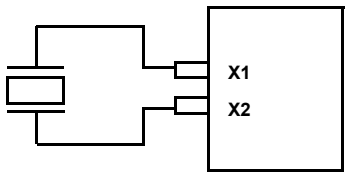



**FIGURE 2. RECOMMENDED CRYSTAL CONNECTION**

### VBAT (Battery Input)

This input provides a backup supply voltage to the device. VBAT supplies power to the device in the event that the VDD supply fails. This pin can be connected to a battery, a Super Capacitor or tied to ground if not used.

### AC (AC Input)

The AC input is the main clock input for the real time clock. It can be either 50Hz or 60Hz, sine wave. The preferred amplitude is $2.5V_{P-P}$, although amplitudes $>0.25V_{DD}$ are acceptable. An AC coupled (series capacitor) sine wave clock waveform is desired as the AC clock input provides DC biasing.

### $\overline{LV}$ (Low Voltage)

This pin indicates the VDD supply is below the programmed level. This signal notifies a host processor that the main supply is low and requests action. It is an open drain active LOW output.

### EVIN (Event Input)

The EVIN pin input detects an externally monitored event. When a HIGH signal is present at the EVIN pin, an "event" is detected.This input may be used for various monitoring functions, such as the opening of a detection switch on a chassis or door. The event detection circuit can be user enabled or disabled (see EVIN bit) and provides the option to be operational in battery backup modes (see EVATB bit). When the event detection is disabled, the EVIN pin is gated OFF. See "Functional Pin Descriptions" on page 3 for more details.

### $\overline{EVDET}$ (Event Detect Output)

The $\overline{EVDET}$ is an open drain output, which will go low when an event is detected at the $\overline{EVIN}$ pin. If the event detection function is enabled, the $\overline{EVDET}$ output will go LOW and stay there until the EVT bit is cleared.

### $\overline{IRQ}$ (Interrupt Output)

This pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active LOW output.

### $F_{OUT}$ (Frequency Output)

This pin outputs a clock signal, which is related to the crystal frequency. The frequency output is user selectable and enabled via the $I^2C$ bus. The options include seven different frequencies or disable. It is a CMOS output.

### Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the backup power supply on the VBAT pin is activated to minimize power consumption.

### Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be OR'ed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz $I^2C$ interface speeds. It is disabled when the backup power supply on the VBAT pin is activated.

### $V_{DD}$, GND

Chip power supply and ground pins. The device will operate with a power supply from $V_{DD}$ = 2.7V to 5.5VDC. A 0.1µF capacitor is recommended on the $V_{DD}$ pin to ground.

## Functional Description

### Power Control Operation

The power control circuit accepts a $V_{DD}$ and a VBAT input. Many types of batteries can be used with Intersil RTC products. For example, 3.0V or 3.6V Lithium batteries are appropriate, and battery sizes are available that can power the ISL12032 for up to 10 years. Another option is to use a Super Capacitor for applications where $V_{DD}$ is interrupted for up to a month. See the "Application Section" on page 24 for more information.

### Normal Mode ($V_{DD}$) to Battery Backup Mode (VBAT)

To transition from the $V_{DD}$ to VBAT mode, both of the following conditions must be met:

**Condition 1:**

$V_{DD} < VBAT - V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

**Condition 2:**

$V_{DD} < V_{TRIP}$
where $V_{TRIP} \approx 2.2V$

### Battery Backup Mode (VBAT) to Normal Mode ($V_{DD}$)

The ISL12032 device will switch from the VBAT to $V_{DD}$ mode when one of the following conditions occurs:

**Condition 1:**

$V_{DD} > VBAT + V_{BATHYS}$
where $V_{BATHYS} \approx 50mV$

**Condition 2:**

$V_{DD} > V_{TRIP} + V_{TRIPHYS}$
where $V_{TRIPHYS} \approx 30mV$

These power control situations are illustrated in Figures 3 and Figure 4.

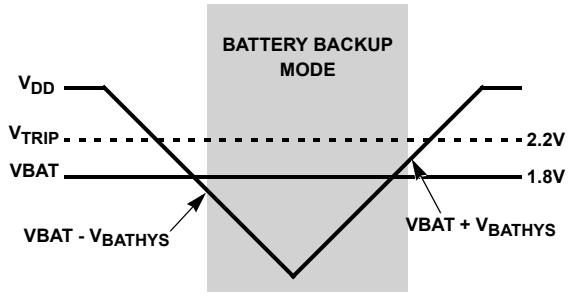



**FIGURE 3. BATTERY SWITCHOVER WHEN VBAT < $V_{TRIP}$**

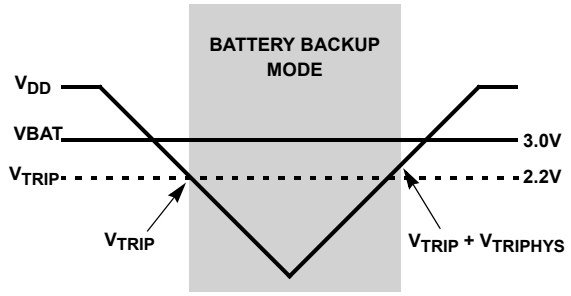



**FIGURE 4. BATTERY SWITCHOVER WHEN VBAT > $V_{TRIP}$**

The $I^2C$ bus is normally deactivated in battery backup mode to reduce power consumption, but can be enabled by setting the $I^2C$BAT bit. All the other inputs and outputs of the ISL12032 are active during battery backup mode unless disabled via the control register.

### Power Failure Detection

The ISL12032 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (both $V_{DD}$ and VBAT very near 0.0VDC). Note that in cases where the VBAT input is at 0.0V and the $V_{DD}$ input dips to <1.8V, then recovers to normal level, the SRAM registers may not retain their values (corrupted bits or bytes may result).

### *Brownout Detection*

The ISL12032 monitors the $V_{DD}$ level continuously and provides a warning if the $V_{DD}$ level drops below prescribed levels. There are six levels that can be selected for the trip level. These values are 85% below popular $V_{DD}$ levels. The LVDD bit in the SRDC register will be set to “1” when Brownout is detected. Note that the $I^2C$ serial bus remains active until the Battery $V_{TRIP}$ level is reached.

### *Battery Level Monitor*

The ISL12032 has a built in warning feature once the VBAT battery level drops first to 85% and then to 75% of the battery’s nominal VBAT level. When the battery voltage falls to between 85% and 75%, the LBAT85 bit is set in the SRDC register. When the level drops below 75%, both LBAT85 and LBAT75 bits are set in the SRDC register. The trip levels for the 85% and 75% levels are set using the PWRBAT register.

The Battery Timestamp Function permits recovering the time/date when $V_{DD}$ power loss occurred. Once the $V_{DD}$ is low enough to enable switchover to the battery, the RTC time/date are written into the TSV2B section. If there are multiple power-down cycles before reading these registers, the first values stored in these registers will be retained and ensuing events will be ignored. These registers will hold the original power-down value until they are cleared by writing “00h” to each register or setting the CLRTS bit to “1”.

The $V_{DD}$ Timestamp Function permits recovering the time/date when $V_{DD}$ recovery occurred. Once the $V_{DD}$ is high enough to enable switchover to $V_{DD}$, the RTC time/date are written into the TSB2V register. If there are multiple power-down cycles before reading these registers, the most recent event is retained in these registers and the previous events will be ignored. These registers will hold the original power-down value until they are cleared by writing “00h” to each register.

## *Real Time Clock Operation*

The Real Time Clock (RTC) maintains an accurate internal representation of tenths of a second, second, minute, hour, day of week, date, month, and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12032 powers up after the loss of both $V_{DD}$ and VBAT, the clock will not begin incrementing until at least one byte is written to the clock register.

## *Alarm Operation*

The alarm mode is enabled via the MSB bit. Single event or interrupt alarm mode is selected via the IM bit. The standard alarm allows for alarms of time, date, day of the week, month, and year. When a time alarm occurs in single event mode, the $\overline{IRQ}$ pin will be pulled low and the corresponding alarm status bit (ALM0 or ALM1) will be set to “1”. The status bits can be written with a “0” to clear, or if the ARST bit is set, a single read of the SRDC status register will clear them.

The pulsed interrupt mode (setting the IM bit to “1”) activates a repetitive or recurring alarm. Hence, once the alarm is set, the device will continue to output a pulse for each occurring match of the alarm and present time. The Alarm pulse will occur as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}$ pin will be pulled LOW for 250ms and the alarm status bit (ALM0 or ALM1) will be set to “1”.

The alarm function is not available during battery backup mode.

### *Frequency Output Mode*

The ISL12032 has the option to provide a clock output signal using the $F_{OUT}$ CMOS output pin. The frequency output mode is set by using the FO bits to select 7 possible output frequency values from 1.0Hz to 32.768kHz, and disable. The frequency output can be enabled/disabled during battery backup mode by setting the FOBATB bit to “0”. When the AC input is qualified (within the parameters of AC qualification) then the Frequency Output for values 50/60Hz and below are derived from the AC input clock. Higher frequency $F_{OUT}$ values are derived from the crystal. If the AC clock input is not qualified, then all $F_{OUT}$ values are derived from the crystal.

### *General Purpose User SRAM*

The ISL12032 provides 128 bytes of user SRAM. The SRAM will continue to operate in battery backup mode. However, it should be noted that the $I^2C$ bus is disabled in battery backup mode unless enabled by the $I^2C$BAT bit.

## *$I^2C$ Serial Interface*

The ISL12032 has an $I^2C$ serial bus interface that provides access to the control and status registers and the user SRAM. The $I^2C$ serial interface is compatible with other industry $I^2C$ serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

The $I^2C$ bus normally operates down to the $V_{DD}$ trip point set in the PWRVDD register. It can also operate in battery backup mode by setting the I2CBAT bit to “1”, in which case operation will be down to VBAT = 1.8V.

## *Register Descriptions*

The battery-backed registers are accessible following an $I^2C$ slave byte of “1101 111x” and reads or writes to addresses [00h:47h]. The defined addresses and default values are described in the Table 1. The battery backed general purpose SRAM has a different slave address (1010 111x), so it is not possible to read/write that section of memory while accessing the registers.

#### REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 10 sections. They are:

1. Real Time Clock (8 bytes): Address 00h to 07h.
2. Status (2 bytes): Address 08h to 09h.
3. Counter (2 bytes): Address Ah to Bh.
4. Control (9 bytes): 0Ch to 14h.
5. Day Light Saving Time (8 bytes): 15h to 1Ch
6. Alarm 0/1 (12 bytes): 1Dh to 28h
7. Time Stamp for Battery Status (5 bytes): Address 29h to 2Dh.
8. Time Stamp for VDD Status (5 bytes): Address 2Eh to 32h.
9. Time Stamp for Event Status (5 bytes): 33h to 37h.

Write capability is allowable into the RTC registers (00h to 07h) only when the WRTC bit (bit 6 of address 0Ch) is set to “1”. Other sections do not need to have the WRTC bit set for write access. A read or write can begin at any address within the section. A write to sections 2 through 9 can be continuous. A write can overlap two or more sections as well.

A register can be read by performing a random read at any address at any time. This returns the contents of that register location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

It is only necessary to set the WRTC bit prior to writing into the RTC registers. All other registers are completely accessible without setting the WRTC bit.

**TABLE 1. REGISTER MEMORY MAP (X indicates writes to these bits have no effect on the device)**

| ADDR | SECTION | REG NAME | BIT | | | | | | | | RANGE | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 00h | RTC | SC | 0 | SC22 | SC21 | SC20 | SC13 | SC12 | SC11 | SC10 | 0 to 59 | 00h |
| 01h | | MN | 0 | MN22 | MN21 | MN20 | MN13 | MN12 | MN11 | MN10 | 0 to 59 | 00h |
| 02h | | HR | MIL | 0 | HR21 | HR20 | HR13 | HR12 | HR11 | HR10 | 0 to 23 | 00h |
| 03h | | DT | 0 | 0 | DT21 | DT20 | DT13 | DT12 | DT11 | DT10 | 1 to 31 | 01h |
| 04h | | MO | 0 | 0 | 0 | MO20 | MO13 | MO12 | MO11 | MO10 | 1 to 12 | 01h |
| 05h | | YR | YR23 | YR22 | YR21 | YR20 | YR13 | YR12 | YR11 | YR10 | 0 to 99 | 00h |
| 06h | | DW | 0 | 0 | 0 | 0 | 0 | DW2 | DW1 | DW0 | 0 to 6 | 00h |
| 07h | | SS | 0 | 0 | 0 | 0 | SS3 | SS2 | SS1 | SS0 | 0 to 9 | 00h |
| 08h | Status | SRDC | BMODE | DSTADJ | ALM1 | ALM0 | LVDD | LBAT85 | LBAT75 | RTCF | N/A | 01h |
| 09h | | SRAC | X | X | X | XOSCF | X | X | ACFAIL | ACRDY | N/A | 00h |
| 0Ah | Counter | ACCNT | AXC7 | AXC6 | AXXC5 | AXC4 | AXC3 | AXC2 | AXC1 | AXC0 | 0 to 127 | 00h |
| 0Bh | | EVTCNT | EVC7 | EVC6 | EVC5 | EVC4 | EVC3 | EVC2 | EVC1 | EVC0 | 0 to 127 | 00h |
| 0Ch | Control | INT | ARST | WRTC | IM | X | X | X | ALE1 | ALE0 | N/A | 01h |
| 0Dh | | FO | X | X | X | FOBATB | X | FO2 | FO1 | FO0 | N/A | 00h |
| 0Eh | | EVIC | X | EVBATB | EVIM | EVEN | EHYS1 | EHYS0 | ESMP1 | ESMP0 | N/A | 00h |
| 0Fh | | EVIX | X | X | X | X | X | 0 | EVIX1 | EVIX0 | N/A | 00h |
| 10h | | TRICK | X | X | X | X | X | TRKEN | TRKRO1 | TRKRO0 | N/A | 00h |
| 11h | | PWRVDD | CLRTS | X | I2CBAT | LVENB | X | VDDTrip2 | VDDTrip1 | VDDTrip0 | N/A | 00h |
| 12h | | PWRBAT | X | BHYS | VB85Tp2 | VB85Tp1 | VB85Tp0 | BV75Tp2 | VB75Tp1 | VB75Tp0 | N/A | 00h |
| 13h | | AC | AC5060 | ACENB | ACRP1 | ACRP0 | ACFP1 | ACFP0 | ACFC1 | ACFC0 | N/A | 00h |
| 14h | | FTR | X | X | X | ACMIN | XDTR3 | XDTR2 | XDTR1 | XDTR0 | N/A | 00h |
| 15h | DSTCR | DstMoFd | DSTE | 0 | 0 | MoFd20 | MoFd13 | MoFd12 | MoFd11 | MoFd10 | 1 to 12 | 04h |
| 16h | | DstDwFd | 0 | DwFdE | WkFd12 | WkFd11 | WkFd10 | DwFd12 | DwFd11 | DwFd10 | 0 to 6 | 00h |
| 17h | | DstDtFd | 0 | 0 | DtFd21 | DtFd20 | DtFd13 | DtFd12 | DtFd11 | DtFd10 | 1 to 31 | 01h |
| 18h | | DstHrFd | HrFdMIL | 0 | HrFd21 | HrFd20 | HrFd13 | HrFd12 | HrFd11 | HrFd10 | 0 to 23 | 02h |
| 19h | | DstMoRv | 0 | 0 | 0 | MoRv20 | MoRv13 | MoRv12 | MoRv11 | MoRv10 | 1 to 12 | 10h |
| 1Ah | | DstDwRv | 0 | DwRvE | WkRv12 | WkRv11 | WkRv10 | DwRv12 | DwRv11 | DwRv10 | 0 to 6 | 00h |
| 1Bh | | DstDtRv | 0 | 0 | DtRv21 | DtRv20 | DtRv13 | DtRv12 | DtRv11 | DtRv10 | 1 to 31 | 01h |
| 1Ch | | DstHrRv | HrRvMIL | 0 | HrRv21 | HrRv20 | HrRv13 | HrRv12 | HrRv11 | HrRv10 | 0 to 23 | 02h |
| 1Dh | Alarm0 | SCA0 | ESCA0 | SCA022 | SCA021 | SCA020 | SCA013 | SCA012 | SCA011 | SCA010 | 0 to 59 | 00h |
| 1Eh | | MNA0 | EMNA0 | MNA021 | MNA020 | MNA013 | MNA012 | MNA011 | MNA011 | MNA010 | 0 to 59 | 00h |
| 1Fh | | HRA0 | EHRA0 | 0 | HRA021 | HRA020 | HRA013 | HRA012 | HRA011 | HRA010 | 0 to 23 | 00h |
| 20h | | DTA0 | EDTA0 | 0 | DTA021 | DTA020 | DTA013 | DTA012 | DTA011 | DTA010 | 1 to 31 | 01h |
| 21h | | MOA0 | EMOA0 | 0 | 0 | MOA020 | MOA013 | MOA012 | MOA011 | MOA010 | 1 to 12 | 01h |
| 22h | | DWA0 | EDWA0 | 0 | 0 | 0 | 0 | DWA02 | DWA01 | DWA00 | 0 to 6 | 00h |

**TABLE 1. REGISTER MEMORY MAP (X indicates writes to these bits have no effect on the device) (Continued)**

| ADDR | SECTION | REG NAME | BIT | | | | | | | | RANGE | DEFAULT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 23h | Alarm1 | SCA1 | ESCA1 | SCA122 | SCA121 | SCA120 | SCA113 | SCA112 | SCA111 | SCA110 | 0 to 59 | 00h |
| 24h | | MNA1 | EMNA1 | MNA122 | MNA121 | MNA120 | MNA113 | MNA112 | MNA111 | MNA110 | 0 to 59 | 00h |
| 25h | | HRA1 | EHRA1 | 0 | HRA121 | HRA120 | HRA113 | HRA112 | HRA111 | HRA110 | 0 to 23 | 00h |
| 26h | | DTA1 | EDTA1 | 0 | DTA121 | DTA120 | DTA113 | DTA112 | DTA111 | DTA110 | 1 to 31 | 01h |
| 27h | | MOA1 | EMOA1 | 0 | 0 | MOA120 | MOA113 | MOA112 | MOA111 | MOA110 | 1 to12 | 01h |
| 28h | | DWA1 | EDWA1 | 0 | 0 | 0 | 0 | DWA12 | DWA11 | DWA10 | 0 to 6 | 00h |
| 29h | TSV2B | SCVB | X | SCBV22 | SCBV21 | SCBV20 | SCVB13 | SCVB12 | SCVB11 | SCVB10 | 0 to 59 | 00h |
| 2Ah | | MNVB | X | MNVB22 | MNVB21 | MNVB20 | MNVB13 | MNVB12 | MNVB11 | MNVB10 | 0 to 59 | 00h |
| 2Bh | | HRVB | MILVB | X | HRVB21 | HRVB20 | HRVB13 | HRVB12 | HRVB11 | HRVB10 | 0 to 23 | 00h |
| 2Ch | | DTVB | X | X | DTVB21 | DTVB20 | DTVB13 | DTVB12 | DTVB11 | DTVB10 | 1 to 31 | 00h |
| 2Dh | | MOVB | X | X | X | MOVB20 | MOVB13 | MOVB12 | MOVB11 | MOVB10 | 1 to 12 | 00h |
| 2Eh | TSB2V | SCBV | X | SCBV22 | SCBV21 | SCBV20 | SCBV13 | SCBV12 | SCBV11 | SCBV10 | 0 to 59 | 00h |
| 2Fh | | MNBV | X | MNBV22 | MNBV21 | MNBV20 | MNBV13 | MNBV12 | MNBV11 | MNBV10 | 0 to 59 | 00h |
| 30h | | HRBV | MILBV | X | HRBV21 | HRBV20 | HRBV13 | HRBV12 | HRBV11 | HRBV10 | 0 to 23 | 00h |
| 31h | | DTBV | X | X | DTBV21 | DTBV20 | DTBV13 | DTBV12 | DTBV11 | DTBV10 | 1 to 31 | 00h |
| 32h | | MOBV | X | X | X | MOBV20 | MOBV13 | MOBV12 | MOBV11 | MOBV10 | 1 to 12 | 00h |
| 33h | TSEVT | SCT | X | SCT22 | SCT21 | SCT20 | SCT13 | SCT12 | SCT111 | SCT10 | 0 to 59 | 00h |
| 34h | | MNT | X | MNT22 | MNT21 | MNT20 | MNT13 | MNT12 | MNT11 | MNT10 | 0 to 59 | 00h |
| 35h | | HRT | MILT | X | HRT21 | HRT20 | HRT13 | HRT12 | HRT11 | HRT10 | 0 to 23 | 00h |
| 36h | | DTT | X | X | DTT21 | DTT20 | DTT13 | DTT12 | DTT11 | DTT10 | 1 to 31 | 00h |
| 37h | | MOT | X | X | X | MOT20 | MOT13 | MOT12 | MOT11 | MOT10 | 1 to 12 | 00h |

## *Real Time Clock Registers*

### *Addresses [00h to 07h]*

#### RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW, SS)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can be either 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, DW (Day of the Week) is 0 to 6, and SS (Sub-Second) is 0 to 9. The Sub-Second register is read-only and will clear to “0” count each time there is a write to a register in the RTC section.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2.... The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

#### 24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

#### LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year and the year 2100 is not. The ISL12032 does not correct for the leap year in the year 2100.

## *Status Registers (SR)*

### *Addresses [08h to 09h]*

The Status Registers consist of the DC and AC status registers (see Tables 2 and 3).

### *Status Register (SRDC)*

The Status Register DC is located in the memory map at address 08h. This is a volatile register that provides status of RTC failure (RTCF), Battery Level Monitor (LBAT85, LBAT75), $V_{DD}$ level monitor (LVDD), Alarm0 or Alarm1 trigger, Daylight Saving Time adjustment, and Battery active mode.

TABLE 2. STATUS REGISTER DC (SRDC)

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 08h | BMODE | DSTADJ | ALM1 | ALM0 | LVDD | LBAT85 | LBAT75 | RTCF |

**BATTERY ACTIVE MODE (BMODE)**

BMODE Indicates that the device is operating from the VBAT input. A “1” indicates Battery Mode and a “0” indicates power from $V_{DD}$ mode. The I2CBAT bit must be set to “1” and the device must be in VBAT mode in order for a valid “1” read from this bit.

**DAYLIGHT SAVING TIME ADJUSTMENT BIT (DSTADJ)**

DSTADJ is the Daylight Saving Time Adjustment Bit. It indicates that daylight saving time adjustment has happened. The bit will be set to “1” when the Forward DST event has occurred. The bit will stay set until the Reverse DST event has happened. The bit will also reset to “0” when the DSTE bit is set to “0” (DST function disabled). The bit can be forced to “1” with by writing “F0h” to the Status Register. The default value for DSTADJ is “0”.

**ALARM BITS (ALM0 AND ALM1)**

These bits announce if an alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

**LOW $V_{DD}$ INDICATOR BIT (LVDD)**

Indicates $V_{DD}$ dropped below the pre-selected trip level. (Brownout Mode). The Trip points for Brownout levels are selected by three bits VDDTrip2, VDDTrip1 and VDDTrip0 in the PWRVDD registers.

**LOW BATTERY INDICATOR 85% BIT (LBAT85)**

Indicates battery level dropped below the pre-selected trip level (85% of battery voltage). The trip point is set by three bits: VB85Tp2, VB85Tp1 and VB85Tp0 in the PWRBAT register.

**LOW BATTERY INDICATOR 75% BIT (LBAT75)**

Indicates battery level dropped below the pre-selected trip level (75% of battery voltage). The trip point is set by three bits: VB75Tp2, VB75Tp1 and VB75Tp0 in the PWRBAT register.

**REAL TIME CLOCK FAIL BIT (RTCF)**

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (internally) when the device powers up after having lost all power (defined as $V_{DD}$ = 0V and VBAT = 0V). The bit is set regardless of whether $V_{DD}$ or VBAT is applied first. The loss of only one of the supplies does not set the RTCF bit to “1”. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

### *Status Register (SRAC)*

TABLE 3. STATUS REGISTER AC (SRAC)

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 09h | X | X | X | XOSCF | X | X | ACFAIL | ACRDY |

The Status Register AC is located in the memory map at address 09h. This is a volatile register that provides status of Crystal Failure (XOSCF), AC Failed (ACFAIL) and AC Ready (ACRDY).

**CRYSTAL OSCILLATOR FAIL BIT (XOSCF)**

Indicates Crystal Oscillator has stopped if XOSCF = 1. When the crystal oscillator has resumed operation, the XOSCF bit is reset to “0”.

**AC FAIL (ACFAIL)**

This bit announces the status of the AC input. If ACFAIL = 1, then the AC input frequency and amplitude qualification check has failed. ACFAIL is reset to “0” when the AC input meets the preset requirements (see “AC (AC Input)” on page 8).

**AC READY (ACRDY)**

This bit announces the status of the AC input. If ACRDY = 1, then the AC input has passed the qualification parameter check (as set by ACFC and ACFP bits) for the time prescribed by ACRP and is used for the RTC clock. When ACRDY = 0 the AC input failed the qualification requirements and the crystal oscillator clock is used for the RTC clock (see “AC (AC Input)” on page 8).

When ACFAIL transitions from “1” to “0” (from failed to pass), then the timer set by ACRP will determine the delay until ACRDY transitions from “0” to “1”. ACRDY will be set to “0” immediately after ACRDY is set to “0” (failed AC input), indicating the crystal oscillator is the RTC clock.

## *Counter Registers*

### *Addresses [0Ah to 0Bh]*

These registers will count the number of times AC failure occurs and the number of times an event occurs. These registers are 8-bits each and will count up to 255.

### *AC COUNT (ACCNT)*

TABLE 4. AC COUNTER REGISTER (ACCNT)

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Ah | AXC7 | AXC6 | AXC5 | AXC4 | AXC3 | AXC2 | AXC1 | AXC0 |

The ACCNT register increments automatically each time the AC input switches to the crystal backup. The register is set to 00h on initial power-up. The maximum count is 255, and will stay at that value until set to zero via an $I^2C$ write.

### *Event Count (EVTCNT)*

**TABLE 5. EVENT COUNTER REGISTER (EVTCNT)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Bh | EVC7 | EVC6 | EVC5 | EVC4 | EVC3 | EVC2 | EVC1 | EVC0 |

The EVTCNT register increments automatically each time an event occurs. The register is set to 00h on initial power-up. The maximum count is 255, and will stay at that value until set to zero via an $I^2C$ write.

Performing a write of 00h to this register will clear the contents of this register and all levels of the TSEVT section. A clear to this register should be done with care. Write event index register zero only selects first event time stamp. Write event count EVNTCNT zero will both clear event counter and all time stamps.

## *Control Registers*

### *Addresses [0Ch to 14h]*

The control registers (INT, FO, EVIC, EVIX, TRICK, PWRVDD, PWRBAT, AC, and FTR) contain all the bits necessary to control the parametric functions on the ISL12032.

### *Interrupt Control Register (INT)*

**TABLE 6. INTERRUPT CONTROL REGISTER (INT)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Ch | ARST | WRTC | IM | X | X | X | ALE1 | ALE0 |

#### AUTOMATIC RESET BIT (ARST)

This bit enables/disables the automatic reset of the ALM0, ALM1, LVDD, LBAT85, and LBAT75 status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the SRDC Register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the ALM0, ALM1, LVDD, LBAT85, and LBAT75 bits.

#### WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Register section. The factory default setting of this bit is “0”. Upon initialization or power-up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle. This bit will remain set until reset to “0” or a complete power-down occurs ($V_{DD}$ = VBAT = 0.0V)

#### ALARM INTERRUPT MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to “1”, the alarms will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}$ pin when the RTC is triggered by either alarm as defined by the Alarm0 section (1Dh to 22h) or the Alarm1 section (23h to 28h). When the IM bit is cleared to “0”, the alarm will operate in standard mode, where the $\overline{IRQ}$ pin will be set LOW until both the ALM0/ALM1 status bits are cleared to “0”.

#### ALARM 1 (ALE 1)

This bit enables the Alarm1 function. When ALE1 = “1”, a match of the RTC section with the Alarm1 section will result is setting the ALM1 status bit to “1” and the $\overline{IRQ}$ output LOW. When set to “0”, the Alarm1 function is disabled.

#### ALARM 0 (ALE 0)

This bit enables the Alarm0 function. When ALE0 = 1, a match of the RTC section with the Alarm1 section will result is setting the ALM0 status bit to “1” and the $\overline{IRQ}$ output LOW. When set to “0”, the Alarm0 function is disabled.

### *Frequency Out Register (FO)*

**TABLE 7. FREQUENCY OUT REGISTER (FO)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Dh | X | X | X | FOBATB | X | FO2 | FO1 | FO0 |

#### FREQUENCY OUTPUT AND INTERRUPT BIT (FOBATB)

This bit enables/disables $F_{OUT}$ during battery backup mode (i.e. VBAT power source active). When the FOBATB is set to “1” the $F_{OUT}$ pin is disabled during battery backup mode. When the FOBATB is cleared to “0”, the $F_{OUT}$ pin is enabled during battery backup mode (default). Note that $F_{OUT}$ is a CMOS output and needs no pull-up resistor. Note also that battery current drain will be higher with $F_{OUT}$ enabled in battery backup mode.

#### FREQUENCY OUT CONTROL BITS (FO <2:0>)

These bits enable/disable the frequency output function and select the output frequency at the $F_{OUT}$ pin. See Table 8 for frequency selection. Note that frequencies from 4096Hz to 32768Hz are derived from the Crystal Oscillator, and the 1.0, 10, and 50/60Hz frequencies are derived from the AC clock input. The exception to this is when the AC input qualification has failed, and the crystal oscillator is used for the 1.0Hz $F_{OUT}$.

**TABLE 8. FREQUENCY SELECTION OF $F_{OUT}$ PIN**

| FREQUENCY, $F_{OUT}$ | UNITS | FO2 | FO1 | FO0 |
|---|---|---|---|---|
| 32768 | Hz | 0 | 0 | 0 |
| 16372 | Hz | 0 | 0 | 1 |
| 8192 | Hz | 0 | 1 | 0 |
| 4096 | Hz | 0 | 1 | 1 |
| 50/60 | Hz | 1 | 0 | 0 |
| 1 | Hz | 1 | 0 | 1 |
| Low | Hz | 1 | 1 | 0 |
| High | Hz | 1 | 1 | 1 |

### *Event Detection Register (EVIC)*

**TABLE 9. EVENT DETECTION REGISTER (EVIC)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Eh | X | EVBATB | EVIM | EVEN | EHYS1 | EHYS0 | ESMP1 | ESMP0 |

#### EVENT OUTPUT IN BATTERY MODE ENABLE BIT (EVBATB)

This bit enables/disables the $\overline{\text{EVDET}}$ pin during battery backup mode (i.e. VBAT pin supply ON). When the EVBATB is set to “1”, the Event Detect Output is disabled in battery backup mode. When the EVBATB is cleared to “0”, the Event Detect output is enabled in battery backup mode. This feature can be used to save power during battery mode.

#### EVENT OUTPUT PULSE MODE (EVIM)

This bit controls the $\overline{\text{EVDET}}$ pin output mode. With EVIM = 0, the output is in normal mode and when an event is triggered, the output will be set LOW until reset. With EVIM = 1, the output is in pulse mode and when an event is triggered, the device will generate a 200ms to 300ms pulse at the $\overline{\text{EVDET}}$ output.

#### EVENT DETECT ENABLE (EVEN)

This bit enables/disables the Event Detect function of the ISL12032. When this bit is set to “1”, the Event Detect is active. When this bit is cleared to “0”, the Event Detect is disabled.

#### EVENT TIME-BASED HYSTERESIS (EHYS1, EHYS0)

These bits set the amount of time-based hysteresis that is present at the EVIN pin for deglitching the input signal. The settings vary from 0ms (hysteresis OFF) to 31.25ms (delay of 31.25ms to check for change of state at the EVIN pin). The Hysteresis function and the Event Input Sampling function work independently.

**TABLE 10. EVENT TIME-BASED HYSTERESIS**

| EHSYS1 | EHSYS0 | TIME (ms) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 3.9 |
| 1 | 0 | 16.625 |
| 1 | 1 | 31.25 |

#### EVENT INPUT SAMPLING RATE (ESMP)

These bits set the frequency of sampling of the Event Input (EVIN). The settings include from 1/4Hz (one sample per 4s) to 2Hz (twice a second), 1Hz, or continuous sampling (Always ON). The less frequent the sampling, the lower the current drain, which can affect battery current drain and battery life.

**TABLE 11. EVENT INPUT SAMPLING RATE**

| ESMP1 | ESMP2 | SAMPLING RATE |
|---|---|---|
| 0 | 0 | Always ON |
| 0 | 1 | 2 Hz |

**TABLE 11. EVENT INPUT SAMPLING RATE**

| ESMP1 | ESMP2 | SAMPLING RATE |
|---|---|---|
| 1 | 0 | 1 Hz |
| 1 | 1 | 1/4 Hz |

### *Event Index Register (EVIX)*

**TABLE 12. EVENT INDEX REGISTER (EVIX)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0Fh | X | X | X | X | X | X | EVIX1 | EVIX0 |

The Event Index Register provides the index for locating an individual event that has been stored. The Event recording function allows recalling up to 4 events, although the Event counting register will count up to 255 events. The 0th location corresponds to the first event, and the 1st through 3rd locations correspond to the most recent events, with the 3rd location (11b) representing the latest event. Therefore, setting EVIX to 03h location and reading the TSEVT section will access the timestamp information for the most recent (latest) event. Setting this register to another value will allow reading the corresponding event from the TSEVT section.

#### EVENT BIT (EVIX <1:0>)

These bits are the Event Counter Register index bits. EVIX1 is the MSB and EVIX0 is the LSB.

### *Trickle Charge Register (TRICK)*

**TABLE 13. TRICKLE CHARGE REGISTER (TRICK)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 10h | X | X | X | X | X | TRKEN | TRKRO1 | TRKRO0 |

The trickle charge function allows charging current to flow from the $V_{DD}$ supply to the VBAT pin through a selectable current limiting resistor. Disabling the trickle charge function removes this connection and isolates the battery from the $V_{DD}$ supply in the case charging is not necessary or harmful (as in the case with a lithium coin cell battery). Note that there is no charging diode in series with the trickle charge resistor, but a switch network that adds a small series resistance to the charging resistance.

#### TRICKLE CHARGE BIT (TRKEN)

This bit enables/disables the trickle charge capability for the backup battery supply. Setting this bit to “1” will enable the trickle charge. Resetting this bit to “0” will disable the trickle charge function and isolate the battery from the $V_{DD}$ supply.

#### TRICKLE CHARGE RESISTOR (TRKRO<1:0>)

These bits allow the user to change the trickle charge resistor settings according to the maximum current desired for the battery or super capacitor charging.

$$I_{MAX} = \frac{V_{DD} - V_{BAT}}{R_{OUT}} \quad \text{(EQ. 1)}$$

Where the $R_{OUT}$ is the selected resistor between $V_{DD}$ and VBAT. Table 14 gives the typical resistor values for $V_{DD}$ = 5V and VBAT = 3.0V. Note that the resistor value changes with $V_{DD}$ input voltage and VBAT voltage, as well as with temperature.

**TABLE 14. RESISTOR SELECTION REGISTER**

| TRKRO1 | TRKRO0 | Rtrk | UNITS |
|---|---|---|---|
| 0 | 0 | 1300 | Ω |
| 0 | 1 | 2200 | Ω |
| 1 | 0 | 3600 | Ω |
| 1 | 1 | 7800 | Ω |

## *Power Supply Control Register (PWRVDD)*

**TABLE 15. POWER SUPPLY CONTROL REGISTER (PWRVDD)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 11h | CLRTS | X | I2CBAT | LVENB | X | VDD Trip2 | VDD Trip1 | VDD Trip0 |

### CLEAR TIME STAMP BIT (CLRTS)

This bit clears both the Time Stamp $V_{DD}$ to Battery (TSV2B) and Time Stamp Battery to $V_{DD}$ (TSB2V) sections. The default setting is “0” which allows normal operation. Setting CLRTS = 1 performs the clear timestamp register function at the conclusion of a successful write operation.

### $I^2C$ IN BATTERY MODE (I2CBAT)

This bit allows $I^2C$ operation in battery backup mode (VBAT powered) when set to “1”. When reset to “0”, the $I^2C$ operation is disabled in battery mode, which results in the lowest $I_{DD}$ current.

Note that when the $I^2C$ operation is desired in VBAT mode, the SCL and SDA pull-ups must go to the VBAT source for proper communications. This will result in additional VBAT current drain (on top of the increased device VBAT current) during serial communications.

### $V_{DD}$ BROWNOUT TRIP VOLTAGE (VDDTRIP <2:0>)

These bits set the 6 trip levels for the $V_{DD}$ alarm and VBAT switchover. The LVDD bit in the SRDC is set to “1” when $V_{DD}$ drops below this preset level. See Table 16.

**TABLE 16. VDD TRIP LEVELS**

| $V_{DD}$Trip2 | $V_{DD}$Trip1 | $V_{DD}$Trip0 | TRIP VOLTAGE (V) |
|---|---|---|---|
| 0 | 0 | 0 | 2.295 |
| 0 | 0 | 1 | 2.550 |
| 0 | 1 | 0 | 2.805 |
| 0 | 1 | 1 | 3.060 |
| 1 | 0 | 0 | 4.250 |

**TABLE 16. VDD TRIP LEVELS**

| $V_{DD}$Trip2 | $V_{DD}$Trip1 | $V_{DD}$Trip0 | TRIP VOLTAGE (V) |
|---|---|---|---|
| 1 | 0 | 1 | 4.675 |

## *Battery Voltage Warning Register (PWRVBAT)*

This register controls the trip points for the two VBAT warnings, with levels set to approximately 85% and 75% of the nominal battery level.

**TABLE 17. BATTERY VOLTAGE WARNING REGISTER (PWRVBAT)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 12h | X | BHYS | VB85Tp2 | VB85Tp1 | VB85Tp0 | VB75Tp2 | VB75Tp1 | VB75Tp0 |

### VBAT HYSTERESIS (BHYS)

This bit enables/disables the hysteresis voltage for the $V_{DD}$/VBAT switchover. When set to “1”, hysteresis is enabled and switching to VBAT occurs at approximately 50mV below the $V_{DD}$ Trip point (set by VDDTrip<2:0>). Switching from VBAT to $V_{DD}$ power will occur at approximately 50mV above the $V_{DD}$ trip point.

When set to “0”, there is no hysteresis and switchover will occur at exactly the VDD trip point. Note that for slow moving $V_{DD}$ power-down and power-up signals there can be some extra switching cycles without hysteresis.

### BATTERY LEVEL MONITOR TRIP BITS (VB85TP <2:0>)

Three bits selects the first alarm (85% of Nominal VBAT) level for the battery voltage monitor. There are total of 7 levels that could be selected for the first warning. Any of the levels could be selected as the first warning with no reference as to nominal VBAT voltage level. See Table 18 for typical values.

**TABLE 18. VB85T VBAT WARNING LEVELS**

| VB85Tp2 | VB85Tp1 | VB85Tp0 | BATTERY ALARM TRIP LEVEL (V) |
|---|---|---|---|
| 0 | 0 | 0 | 2.125 |
| 0 | 0 | 1 | 2.295 |
| 0 | 1 | 0 | 2.550 |
| 0 | 1 | 1 | 2.805 |
| 1 | 0 | 0 | 3.060 |
| 1 | 0 | 1 | 4.250 |
| 1 | 1 | 0 | 4.675 |

### BATTERY LEVEL MONITOR TRIP BITS (VB75TP <2:0>)

Three bits selects the second warning (75% of Nominal VBAT) level for the battery voltage monitor. There are total of 7 levels that could be selected for the second monitor. Any of the levels could be selected as the second alarm with no reference as to nominal VBAT voltage level. See Table 19 for typical values.

**TABLE 19. VB75T VBAT WARNING LEVELS**

| VB75Tp2 | VB75Tp1 | VB75Tp0 | BATTERY ALARM TRIP LEVEL (V) |
|---|---|---|---|
| 0 | 0 | 0 | 1.875 |
| 0 | 0 | 1 | 2.025 |
| 0 | 1 | 0 | 2.250 |
| 0 | 1 | 1 | 2.475 |
| 1 | 0 | 0 | 2.700 |
| 1 | 0 | 1 | 3.750 |
| 1 | 1 | 0 | 4.125 |

## *AC Register (AC)*

This register sets the performance screening for the AC input.

**TABLE 20. AC REGISTER**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 13h | AC5060 | ACENB | ACRP1 | ACRP0 | ACFP1 | ACFP0 | ACFC1 | ACFC0 |

### AC 50/60HZ INPUT SELECT (AC5060)

This bit selects either 50Hz or 60Hz powerline AC clock input frequency. Setting this bit to “0” selects a 60Hz input (default). Setting this bit to “1” selects a 50Hz input.

### AC ENABLE (ACENB)

This bit will enable/disable the AC clock input. Setting this bit to “0” will enable the AC clock input (default). Setting this bit to “1” will disable the AC clock input. When the AC input is disabled, the crystal oscillator becomes the sole source for RTC and $F_{OUT}$ clocking.

### AC RECOVERY PERIOD (ACRP<1:0>)

This bit sets the AC clock input validation recovery period. After the AC input fails validation (ACFAIL = 1), a predefined period is used to test the frequency and voltage of the AC clock input. The range is from 2s to 16s.

**TABLE 21. AC RECOVERY PERIOD**

| ACRP1 | ACRP0 | RECOVERY TIME |
|---|---|---|
| 0 | 0 | 2s |
| 0 | 1 | 4s |
| 1 | 0 | 8s |
| 1 | 1 | 16s |

### AC FAILURE CYCLES (ACFP<1:0>)

These two bits determine how many AC cycles are used for the AC clock qualification, or to disable the AC clock qualification. The range is from 1 AC cycle to 12 AC cycles or disable, and is also dependent on the AC5060 bit setting (see Table 22). The qualification logic will count the number of crystal cycles in the chosen AC period, and if the count is outside the window set by ACFC bits then the ACFAIL signal is set to “1”.

For example, if 10 cycles are chosen for 50Hz input, then during those 10 cycles there would need to be exactly 6554 crystal cycles. That number is subtracted from the actual count during the 10 AC cycles and the absolute value is compared to the error value set by ACFC. If the error were 10 crystal cycles and ACFC were set to 11b, then the allowable error would be 20 crystal cycles and the ACFAIL would be “0”, or qualification has passed. If the actual error count were 22 cycles then the ACFAIL would be set to “1”, qualification has failed.

**TABLE 22. AC FAILURE CYCLES**

| CYCLE USED for COUNT | | | |
|---|---|---|---|
| AC5060 = 0 | AC5060=1 | ACFP1 | ACFP0 |
| (Disabled) | | 0 | 0 |
| 1 | 1 | 0 | 1 |
| 6 | 5 | 1 | 0 |
| 12 | 10 | 1 | 1 |

### AC/CRYSTAL FREQUENCY FAILURE CRITERION (ACFC<1:0>)

These two bits determine the number of crystal cycles used for the error budget for the AC qualification (see Table 24). Two of the choices are for a fixed ppm criterion of 1 or 2 crystal cycles in just one AC cycle (independent of the ACFP setting). The other choices are for 1 or 2 crystal cycles per AC cycle, but includes the total number of cycles set by the ACFP.

Using the example given for the ACFP bits previously mentioned:

AC5060 = 1 (50Hz)

ACFC = 11b (2 crystal cycles/AC cycle)

ACFP = 11b (10 total AC cycles)

So the resulting crystal cycle count must be within:

±(10 AC cycles x 2 crystal cycles/AC cycle) or

± 20 total crystal cycles (error budget) as shown in Table 23.

**TABLE 23. AC/CRYSTAL FREQUENCY FAILURE CRITERION**

| ACFC1 | ACFC0 | CRITERION | TOTAL XTAL CYCLE ERROR BUDGET |
|---|---|---|---|
| 0 | 0 | 1 crystal cycle per AC cycle | ACFP x 1 |
| 0 | 1 | 2 crystal cycle per AC cycle | ACFP x 2 |
| 1 | 0 | 1 crystal cycle in all AC cycles | 1 |
| 1 | 1 | 2 crystal cycles in all AC cycles | 2 |

### *Fine Trim Compensation Register (FTR)*

This register (Table 24) provides control of the crystal oscillator clock compensation and the AC clock input minimum level detect.

**TABLE 24. FINE TRIM COMPENSATION REGISTER**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 14h | X | X | X | ACMIN | XDTR3 | XDTR2 | XDTR1 | XDTR0 |

#### AC MINIMUM (ACMIN)

This bit determines the minimum peak-to-peak voltage level for the AC clock input as a percentage of the existing $V_{DD}$ supply. ACMIN = 0 sets the minimum level to 5% x $V_{DD}$. ACMIN = 1 sets the minimum level to 10% x $V_{DD}$.

#### DIGITAL TRIM REGISTER (XDTR<3:0>)

The digital trim register bits control the amount of trim used to adjust for the crystal clock error. This trim is accomplished by adding or subtracting the 32kHz clock in the clock counter chain to adjust the RTC clock. Calibration can be done by monitoring the $F_{OUT}$ pin with a frequency counter with the frequency output set to 1.0Hz, with no AC input.

**TABLE 25. XDTR FREQUENCY COMPENSATION**

| XDTR3 | XDTR2 | XDTR1 | XDTR0 | FREQUENCY COMPENSATION (ppm) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 10 |
| 0 | 0 | 1 | 0 | 20 |
| 0 | 0 | 1 | 1 | 30 |
| 0 | 1 | 0 | 0 | 40 |
| 0 | 1 | 0 | 1 | 50 |
| 0 | 1 | 1 | 0 | 60 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | -10 |
| 1 | 0 | 1 | 0 | -20 |
| 1 | 0 | 1 | 1 | -30 |
| 1 | 1 | 0 | 0 | -40 |
| 1 | 1 | 0 | 1 | -50 |
| 1 | 1 | 1 | 0 | -60 |
| 1 | 1 | 1 | 1 | 0 |

### *DST Control Registers (DSTCR)*

8 bytes of control registers have been assigned for the Daylight Savings Time (DST) functions. DST beginning (set Forward) time is controlled by the registers DstMoFd, DstDwFd, DstDtFd, and DstHrFd. DST ending time (set Backward or Reverse) is controlled by DstMoRv, DstDwRv, DstDtRv and DstHrRv.

Tables 26 and 27 describe the structure and functions of the DSTCR.

#### DST FORWARD REGISTERS (15H TO 18H)

DSTE is the DST Enabling Bit located in bit 7 of register 15h (DstMoFdxx). Set DSTE = 1 will enable the DSTE function. Upon powering up for the first time (including battery), the DSTE bit defaults to “0”.

DST forward is controlled by the following DST Registers:

DstMoFd sets the Month that DST starts. The default value for the DST begin month is April (04h).

DstDwFd sets the Day of the Week that DST starts. DstDwFdE sets the priority of the Day of the Week over the Date. For DstDwFdE = 1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for the DST Forward Day of the Week is Sunday (00h).

DstDtfd controls which Date DST begins. The default value for DST forward date is on the first date of the month (01h). DstDtFd is only effective if DstDwFdE = 0.

**TABLE 26. DST FORWARD REGISTERS**

| ADDRESS | FUNCTION | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| **15h** | **Month Forward** | DSTE | 0 | 0 | MoFd20 | MoFd13 | MoFd12 | MoFd11 | MoFd10 |
| **16h** | **Day Forward** | 0 | DwFdE | WkFd12 | WkFd11 | WkFd10 | DwFd12 | DwFd11 | DwFd10 |
| **17h** | **Date Forward** | 0 | 0 | DtFd21 | DtFd20 | DtFd13 | DtFd12 | DtFd11 | DtFd10 |
| **18h** | **Hour Forward** | HrFdMIL | 0 | HrFd21 | HrFd20 | HrFd13 | HrFd12 | HrFd11 | HrFd10 |

**TABLE 27. DST REVERSE REGISTERS**

| ADDRESS | NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| **19h** | **Month Reverse** | 0 | 0 | 0 | MoRv20 | MoRv13 | MoRv12 | MoRv11 | MoRv10 |
| **1Ah** | **Day Reverse** | 0 | DwRvE | WkRv12 | WkRv11 | WkRv10 | DwRv12 | DwRv11 | DwRv10 |
| **1Bh** | **Date Reverse** | 0 | 0 | DtRv21 | DtRv20 | DtRv13 | DtRv12 | DtRv11 | DtRv10 |
| **1Ch** | **Hour Reverse** | HrRvMIL | 0 | HrRv21 | HrRv20 | HrRv13 | HrRv12 | HrRv11 | HrRv10 |

DstHrFd controls the hour that DST begins. It includes the MIL bit, which is in the corresponding RTC register. The RTC hour and DstHrFd registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value for DST hour is 2:00AM (02h). The time is advanced from 2:00:00AM to 3:00:00AM for this setting.

**DST REVERSE REGISTERS (19H TO 1CH)**

DST end (reverse) is controlled by the following DST Registers.

DstMoRv sets the Month that DST ends. The default value for the DST end month is October (10h).

DstDwRv controls the Day of the Week that DST should end. The DwRvE bit sets the priority of the Day of the Week over the Date. For DwRvE = 1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for DST DwRv end is Sunday (00h).

DstDtRv controls which Date DST ends. The default value for DST Date Reverse is on the first date of the month. The DstDtRv is only effective if the DwRvE = 0.

DstHrRv controls the hour that DST ends. It includes the MIL bit, which is in the corresponding RTC register. The RTC hour and DstHrRv registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value sets the DST end at 2:00AM. The time is set back from 2:00:00AM to 1:00:00AM for this setting.

### *ALARM Registers (1Dh to 28h)*

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode:

**Single Event Mode** is enabled by setting either ALE0 or ALE1 to 1, then setting bit 7 on any of the Alarm registers (ESCA... EDWA) to “1”, and setting the IM bit to “0”. This mode permits a one-time match between the Alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to “1” and the $\overline{IRQ}$ output will be pulled LOW and will remain LOW until the ALM bit is reset. This can be done manually or by using the auto-reset feature. Since the $\overline{IRQ}$ output is shared by both alarms, they both need to be reset in order for the $\overline{IRQ}$ output to go HIGH.

**Interrupt Mode** is enabled by setting either ALE0 or ALE1 to 1, then setting bit 7 on any of the Alarm registers (ESCA... EDWA) to “1”, and setting the IM bit to “1”. Setting the IM bit to 1 puts both ALM0 and ALM1 into Interrupt mode. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs (either AL0 or AL1). This means that once the interrupt mode alarm is set, it will continue to alarm until it is reset.

To clear a single event alarm, the corresponding ALM0 or ALM1 bit in the SRDC register must be set to “0” with a write. Note that if the ARST bit is set to “1” (address 0Ch, bit 7), the ALM0 and ALM1 bits will automatically be cleared when the status register is read.

The $\overline{IRQ}$ output will be set by an alarm match for either ALM0 or ALM1.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

**Example 1**

- Alarm set with single interrupt (IM = ”0”)
- A single alarm will occur on January 1 at 11:30am.
- Set Alarm registers as follows:

| ALARM REGISTER | BIT | | | | | | | | | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX | |
| SCA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Seconds disabled |
| MNA0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h | Minutes set to 30, enabled |
| HRA0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 91h | Hours set to 11, enabled |
| DTA0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81h | Date set to 1, enabled |
| MOA0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81h | Month set to 1, enabled |
| DWA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Day of week disabled |

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30 a.m. on January 1 (after seconds changes from 59 to 00) by setting the ALM0 bit in the status register to “1” and also bringing the $\overline{IRQ}$ output LOW.

**Example 2**

- Pulsed interrupt once per minute (IM = ”1”)
- Interrupts at one minute intervals when the seconds register is at 30 seconds.
- Set Alarm registers as follows:

| ALARM REGISTER | BIT | | | | | | | | | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | HEX | |
| SCA0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h | Seconds set to 30, enabled |
| MNA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Minutes disabled |
| HRA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Hours disabled |
| DTA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Date disabled |
| MOA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Month disabled |
| DWA0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h | Day of week disabled |

Once the registers are set, the following waveform will be seen at $\overline{IRQ}$:

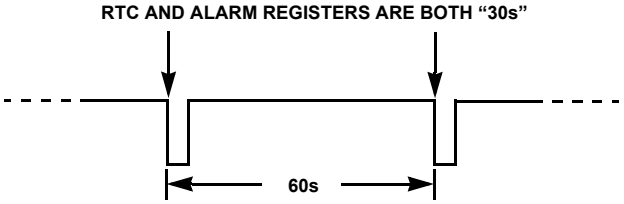



**FIGURE 5. $\overline{IRQ}$ WAVEFORM**

Note that the status register ALM0 bit will be set each time the alarm is triggered, but does not need to be read or cleared.

### *Time Stamp $V_{DD}$ to Battery Registers (TSV2B)*

The TSV2B section bytes are identical to the RTC register section, except they do not extend beyond the Month. The Time Stamp captures the FIRST $V_{DD}$ to Battery Voltage transition time, and will not update upon subsequent events, until cleared (only the first event is captured before clearing). Set CLRTS = 1 to clear this register (Addr 11h, PWRVDD register).

### *Time Stamp Battery to $V_{DD}$ Registers (TSB2V)*

The Time Stamp Battery to $V_{DD}$ section bytes are identical to the RTC section bytes, except they do not extend beyond Month. The Time Stamp captures the LAST transition of VBAT to $V_{DD}$ (only the last power up event of a series of power up/down events is retained). Set CLRTS = 1 to clear this register (Addr 11h, PWRVDD register).

### *Time Stamp Event Registers (TSEVT)*

The TSEVT section bytes are identical to the RTC section bytes, except they do not extend beyond the Month. The Time Stamp captures the first event and the most recent three events. The first event Time Stamp will not update until cleared. All 4 Time Stamps are all cleared to “0” when writing the event counter (0Bh) is set to “0”.

**Note:** The time stamp registers are cleared to all “0”, including the month and day, which is different from the RTC and alarm registers (those registers default to 01h). This is the indicator that no time stamping has occurred since the last clear or initial power-up. Once a time stamp occurs, there will be a non-zero time stamp.

## *User Memory Registers (accessed by using Slave Address 1010111x)*

### *Addresses [00h to 7Fh]*

These registers are 128 bytes of battery-backed user SRAM. Writes to this section do not need to be proceeded by setting the WRTC bit.

## *$I^2C$ Serial Interface*

The ISL12032 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12032 operates as a slave device in all applications.

All communication over the $I^2C$ interface is conducted by sending the MSB of each byte of data first.

### *Protocol Conventions*

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 6). On power-up of the ISL12032, the SDA pin is in the input mode.

All $I^2C$ interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12032 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 6). A START condition is ignored during the power-up sequence.

All $I^2C$ interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 6). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 7).

The ISL12032 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12032 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

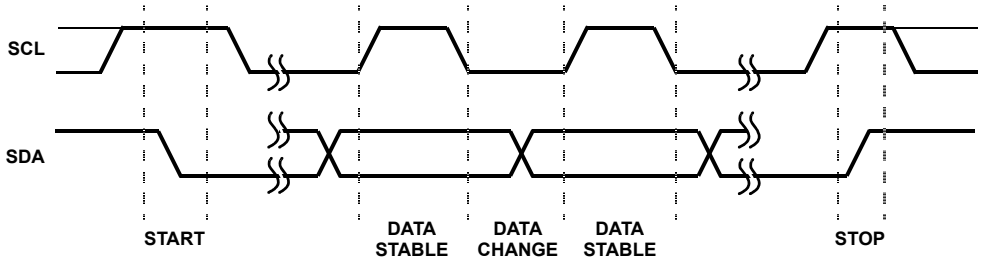



FIGURE 6. VALID DATA CHANGES, START AND STOP CONDITIONS

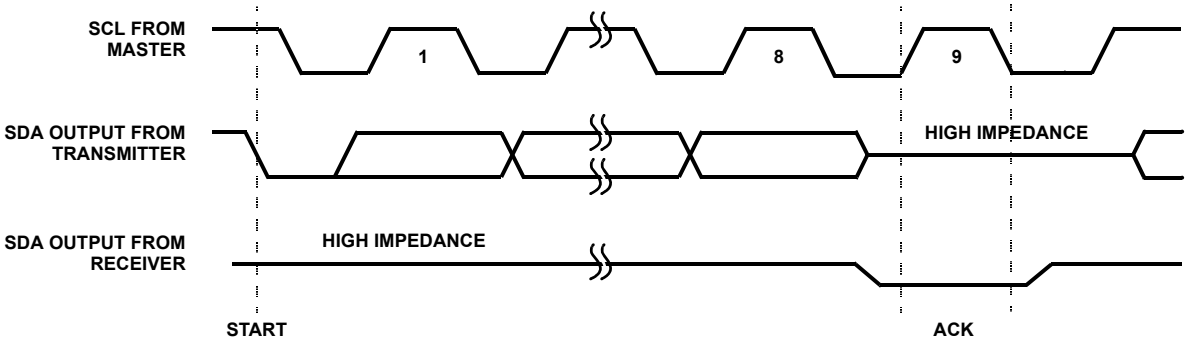



FIGURE 7. ACKNOWLEDGE RESPONSE FROM RECEIVER

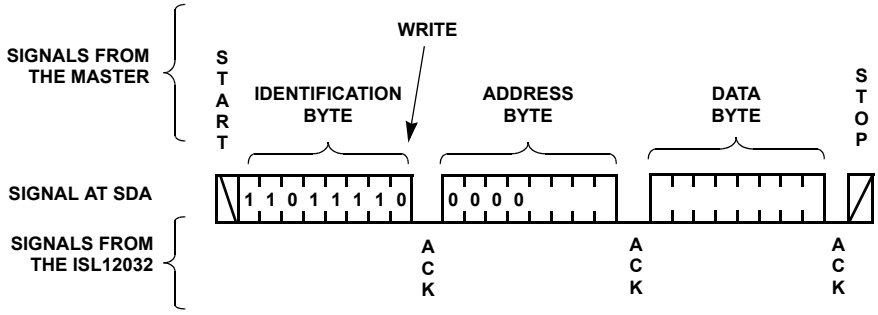



FIGURE 8. BYTE WRITE SEQUENCE (SLAVE ADDRESS FOR CSR SHOWN)

## Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are “1101111b” for the RTC registers and “1010111b” for the User SRAM.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected. A “0” selects a write operation (refer to Figure 9).

After loading the entire Slave Address Byte from the SDA bus, the ISL12032 compares the device identifier and device select bits with “1101111b” or “1010111b”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power up the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the 1 Word Address Byte as shown in Figure 9.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Control/Status Registers, the slave byte must be “1101111x” in both places.

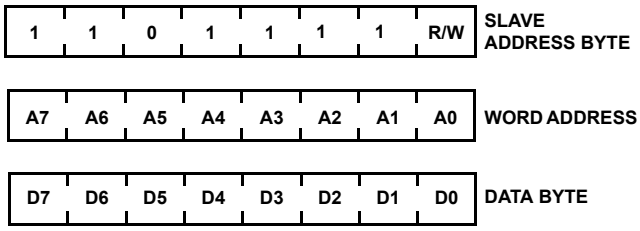



**FIGURE 9. SLAVE ADDRESS, WORD ADDRESS, AND DATA BYTES**

## Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12032 responds with an ACK. At this time, the $I^2C$ interface enters a standby state.

A multiple byte operation within a page is permitted. The Address Byte must have the start address, and the data bytes are sent in sequence after the address byte, with the ISL12032 sending an ACK after each byte. The page write is terminated with a STOP condition from the master. The pages within the ISL12032 do not support wrapping around for page read or write operations.

## Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 10). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL12032 responds with an ACK. Then the ISL12032 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 10).

The Data Bytes are from the memory location indicated by an internal pointer. This pointers initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the last memory location in a section or page, the master should issue a STOP. Bytes that are read at addresses higher than the last address in a section may be erroneous.

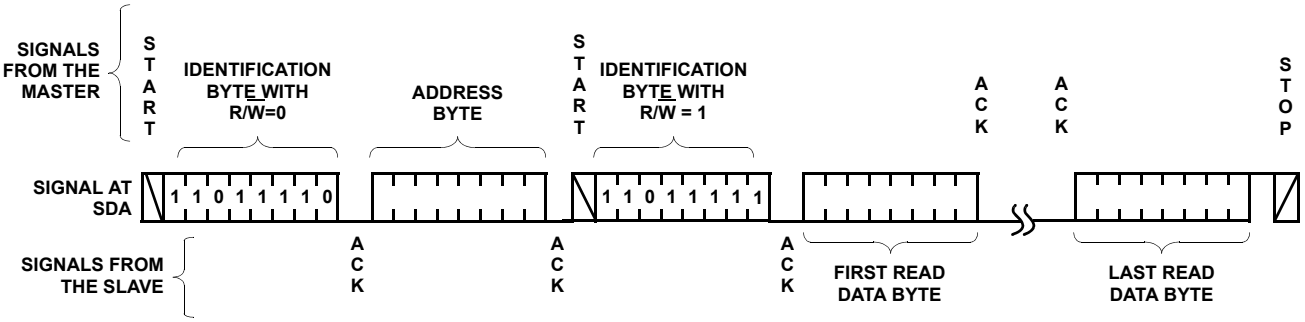



**FIGURE 10. READ SEQUENCE (CSR SLAVE ADDRESS SHOWN)**

## Application Section

### Oscillator Crystal Requirements

The ISL12032 uses a standard 32.768kHz crystal. Either through hole or surface mount crystals can be used. Table 28 lists some recommended surface mount crystals and the parameters of each. This list is not exhaustive and other surface mount devices can be used with the ISL12032 if their specifications are very similar to the devices listed. The crystal should have a required parallel load capacitance of 12.5pF and an equivalent series resistance of less than 50kΩ. The crystal's temperature range specification should match the application. Many crystals are rated for -10°C to +60°C (especially through hole and tuning fork types), so an appropriate crystal should be selected if extended temperature range is required.

**TABLE 28. SUGGESTED SURFACE MOUNT CRYSTALS**

| MANUFACTURER | PART NUMBER |
|---|---|
| Citizen | CM200S |
| Epson | MC-405, MC-406 |
| Raltron | RSM-200S |
| SaRonix | 32S12 |
| Ecliptek | ECPSM29T-32.768K |
| ECS | ECX-306 |
| Fox | FSM-327 |

### Layout Considerations

The crystal input at X1 has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and ensure accurate clocking.

Two main precautions for crystal PC board layout should be followed:

1. Do not run the serial bus lines or any high speed logic lines in the vicinity of the crystal. These logic level lines can induce noise in the oscillator circuit to cause misclocking.
2. Add a ground trace around the crystal with one end terminated at the chip ground. This will provide termination for emitted noise in the vicinity of the RTC device.

In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins and the crystal, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $F_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well. The traces for the VBAT

and $V_{DD}$ pins can be treated as a ground, and should be routed around the crystal.

### AC Input Circuits

The AC input ideally will have a $2.5V_{P-P}$ sine wave at the input, so this is the target for any signal conditioning circuitry for the 50/60Hz waveform. Note that the peak-to-peak amplitude can range from $1V_{P-P}$ up to $V_{DD}$, although it is best to keep the max signal level just below $V_{DD}$. The AC input provides DC offset so AC coupling with a series capacitor is advised.

If the AC power supply has a transformer, the secondary output can be used for clocking with a resistor divider and series AC coupling capacitor. A sample circuit is shown in Figure 12. Values for $R_1/R_2$ are chosen depending on the peak-to-peak range on the secondary voltage in order to match the input of the ISL12032. $C_{IN}$ can be sized to pass up to 300Hz or so, and in most cases, 0.47µF should be the selected value for a ±20% tolerance device.

The AC input to the IS12032 can be damaged if subjected to a normal AC waveform when $V_{DD}$ is powered down. this can happen in circuits where there is a local LDO or power switch for placing circuitry in standby, while the AC main is still switched ON. Figure 11 shows a modified version of the Figure 12 circuit, which uses an emitter follower to essentially turn off the AC input waveform if the $V_{DD}$ supply goes down.

### Using the ISL12032 with No AC Input

Some applications may need all the features of the ISL12032 but do not have access to the power line AC clock, or do not need the accuracy provided by that clock. In these cases there is no problem using the crystal oscillator as the primary clock source for the device.

The user must simply set the ACENB bit in register 13h to "1", which disables the AC input pin and forces the device to use the crystal oscillator exclusively for the RTC and $F_{OUT}$ clock source. Setting this bit to "1" also will cause the ACRDY bit in the SRAC register to be set to "1", indicating that there can be no fault with the AC input clock since it is not used.

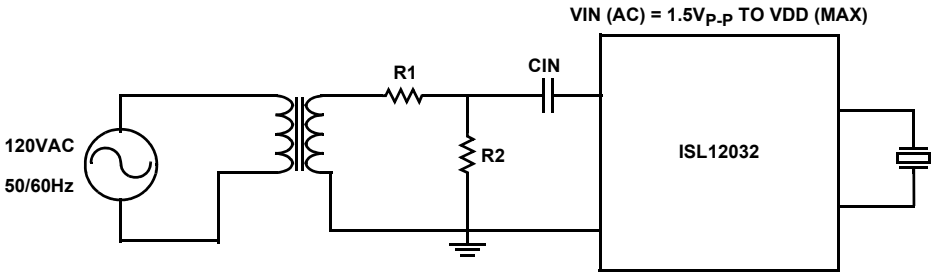



FIGURE 11. AC INPUT USING A TRANSFORMER SECONDARY

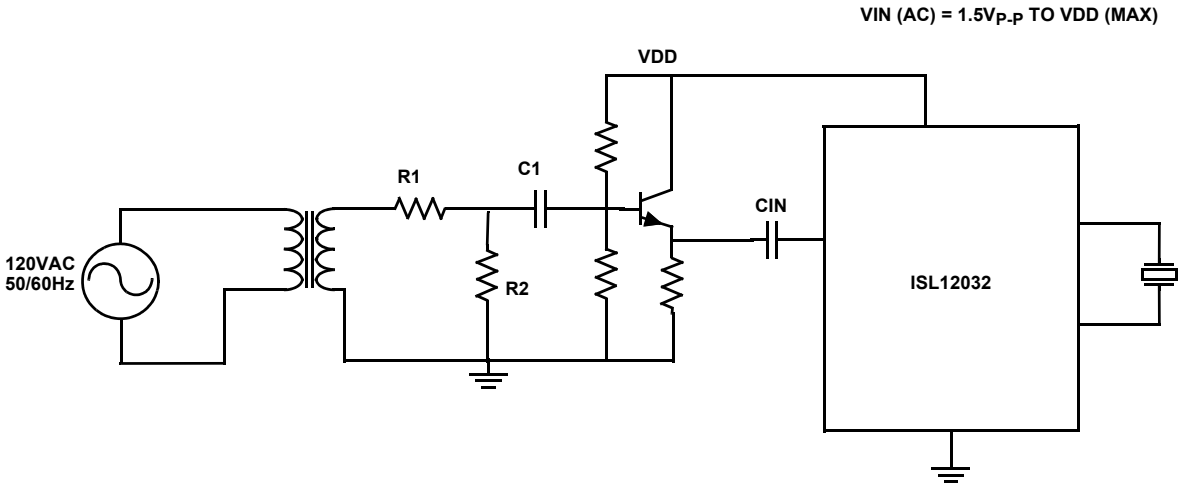



FIGURE 12. USING THE $V_{DD}$ SUPPLY TO GATE THE AC INPUT

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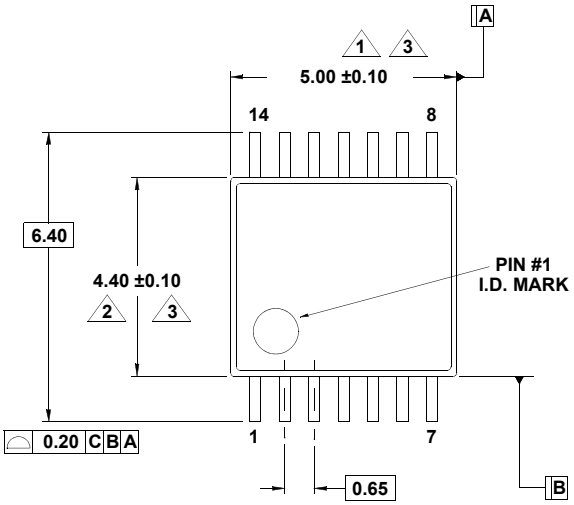
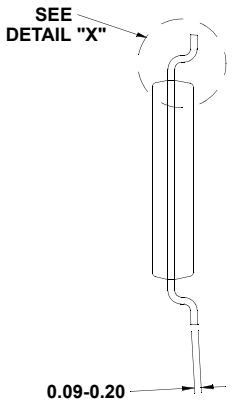
# Package Outline Drawing

## M14.173

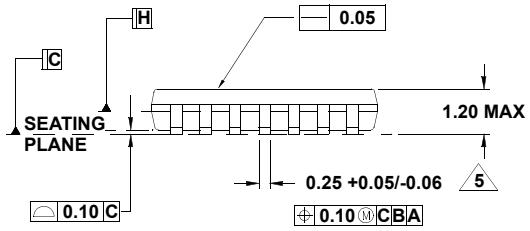
**14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)**
**Rev 3, 10/09**



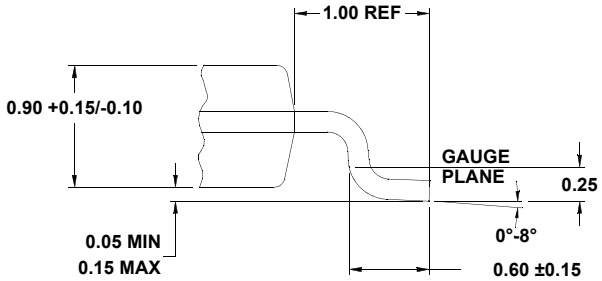

TOP VIEW



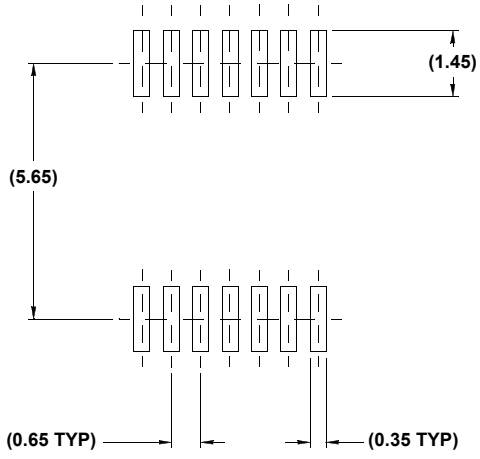

END VIEW




SIDE VIEW




DETAIL "X"




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.