

NCV4264-2

Linear Regulator, Low Dropout, Low I_Q

The NCV4264-2 is functionally and pin for pin compatible with NCV4264 with a lower quiescent current consumption. Its output stage supplies 100 mA with $\pm 2.0\%$ output voltage accuracy.

Maximum dropout voltage is 500 mV at 100 mA load current.

It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

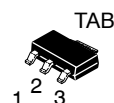
Features

- 3.3 V and 5.0 V Fixed Output
- $\pm 2.0\%$ Output Accuracy, Over Full Temperature Range
- 60 μ A Maximum Quiescent Current at I_{OUT} = 100 μ A
- 500 mV Maximum Dropout Voltage at 100 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
 - ◆ -42 V Reverse Voltage
 - ◆ Short Circuit/Overcurrent
 - ◆ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This is a Pb-Free Device

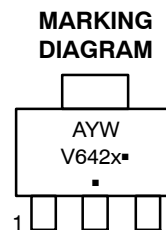


ON Semiconductor®

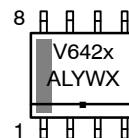
www.onsemi.com



SOT-223
ST SUFFIX
CASE 318E



SOIC-8 Fused
CASE 751



x = 5 (5.0 V Version)
3 (3.3 V Version)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

(SOT-223)		(SOIC-8 Fused)	
PIN	FUNCTION	PIN	FUNCTION
1	V _{IN}	1	NC
2, TAB	GND	2,	V _{IN}
3	V _{OUT}	3	GND
		4.	V _{OUT}
		5-8.	NC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NCV4264-2

THERMAL RESISTANCE

Parameter	Symbol	Min	Max	Unit
Junction-to-Ambient	$R_{\theta JA}$	-	99 (Note 4) 145	°C/W
Junction-to-Case	$R_{\theta JC}$	-	17 -	

ELECTRICAL CHARACTERISTICS ($V_{IN} = 13.5\text{ V}$, $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 5.0 V Version	V_{OUT}	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 5) $6.0\text{ V} \leq V_{IN} \leq 28\text{ V}$	4.900	5.000	5.100	V
Output Voltage 3.3 V Version	V_{OUT}	$5.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 5) $4.5\text{ V} \leq V_{IN} \leq 28\text{ V}$	3.234	3.300	3.366	V
Output Voltage 3.3 V Version	V_{OUT}	$I_{OUT} = 5\text{ mA}$, $V_{IN} = 4\text{ V}$ (Note 7)	3.234	3.300	3.366	V
Line Regulation 5.0 V Version	ΔV_{OUT} vs. V_{IN}	$I_{OUT} = 5.0\text{ mA}$ $6.0\text{ V} \leq V_{IN} \leq 28\text{ V}$	-30	5.0	+30	mV
Line Regulation 3.3 V Version	ΔV_{OUT} vs. V_{IN}	$I_{OUT} = 5.0\text{ mA}$ $4.5\text{ V} \leq V_{IN} \leq 28\text{ V}$	-30	5.0	+30	mV
Load Regulation	ΔV_{OUT} vs. I_{OUT}	$1.0\text{ mA} \leq I_{OUT} \leq 100\text{ mA}$ (Note 5)	-40	5.0	+40	mV
Dropout Voltage – 5.0 V Version	$V_{IN} - V_{OUT}$	$I_{OUT} = 100\text{ mA}$ (Notes 5 & 6)	-	270	500	mV
Dropout Voltage – 3.3 V Version	$V_{IN} - V_{OUT}$	$I_{OUT} = 100\text{ mA}$ (Notes 5 & 8)	-	-	1,266	V
Quiescent Current	I_q	$I_{OUT} = 100\text{ }\mu\text{A}$ $T_J = 25^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $T_J = -40^\circ\text{C}$ to 150°C	-	33 33 33	55 60 70	μA
Active Ground Current	$I_{G(ON)}$	$I_{OUT} = 50\text{ mA}$ (Note 5)	-	1.5	4.0	mA
Power Supply Rejection	PSRR	$V_{RIPPLE} = 0.5\text{ V}_{P-P}$, $F = 100\text{ Hz}$	-	67	-	dB
Output Capacitor for Stability 5.0 V Version	C_{OUT} ESR	$I_{OUT} = 0.1\text{ mA}$ to 100 mA (Notes 5 & 7)	10 -	- -	- 9.0	μF Ω
Output Capacitor for Stability 3.3 V Version	C_{OUT} ESR	$I_{OUT} = 0.1\text{ mA}$ to 100 mA (Notes 5 & 7)	22 -	- -	- 16	μF Ω

PROTECTION

Current Limit	$I_{OUT(LIM)}$	$V_{OUT} = 4.5\text{ V}$ (5.0 V Version) (Note 5) $V_{OUT} = 3.0\text{ V}$ (3.3 V Version) (Note 5)	150 150	- -	500 500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	$V_{OUT} = 0\text{ V}$ (Note 5)	40	-	500	mA
Thermal Shutdown Threshold	T_{TSD}	(Note 7)	150	-	200	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. 1 oz., 100 mm² copper area.

5. Use pulse loading to limit power dissipation.

6. Dropout voltage = $(V_{IN} - V_{OUT})$, measured when the output voltage has dropped 100 mV relative to the nominal value obtained with $V_{IN} = 13.5\text{ V}$.

7. Not tested in production. Limits are guaranteed by design.

8. $V_{DO} = V_{IN} - V_{OUT}$. For output voltage set to < 4.5 V, V_{DO} will be constrained by the minimum input voltage.

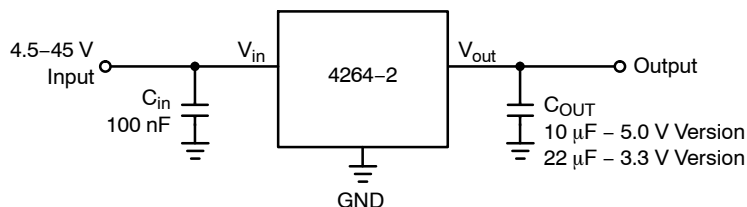


Figure 2. Applications Circuit

TYPICAL CHARACTERISTIC CURVES – 5 V Version

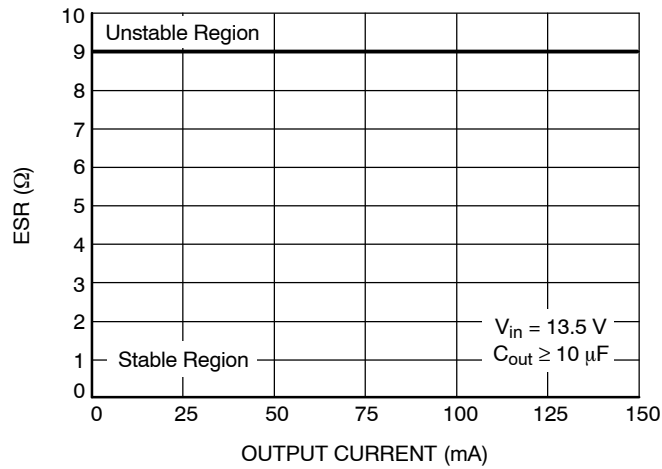


Figure 3. ESR Stability vs. Output Current (5 V Version)

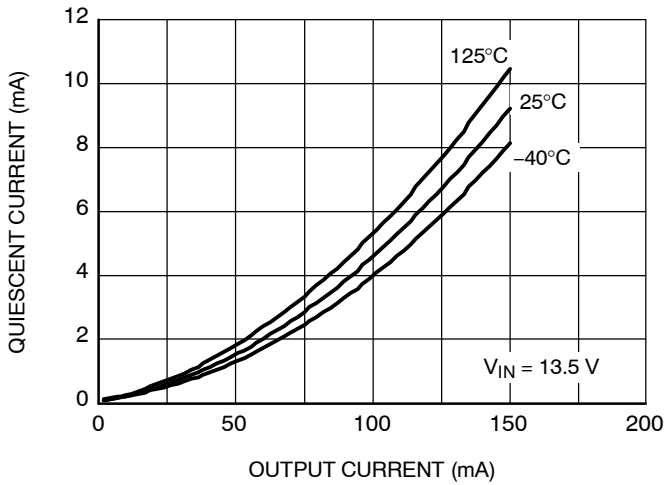


Figure 4. Quiescent Current vs. Output Current (5 V Version)

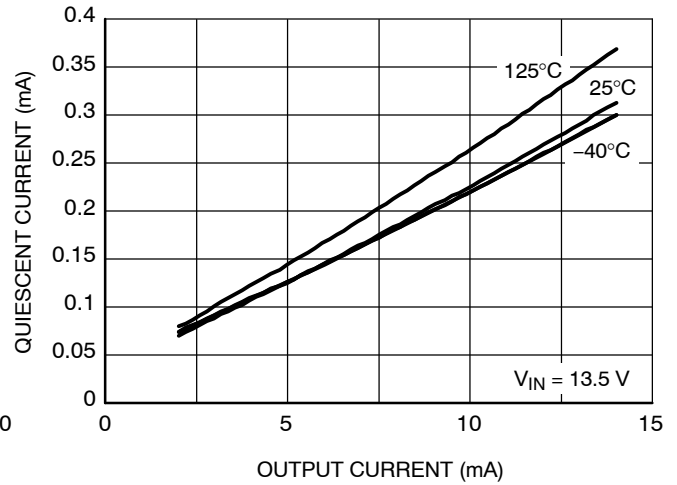


Figure 5. Quiescent Current vs. Output Current (Light Load) (5 V Version)

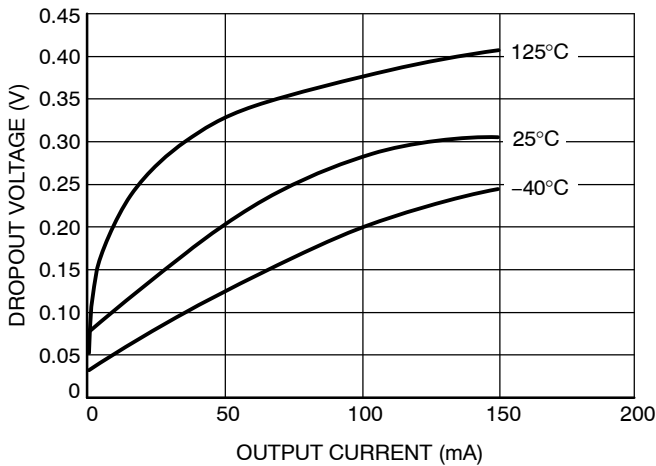


Figure 6. Dropout Voltage vs. Output Current (5 V Version)

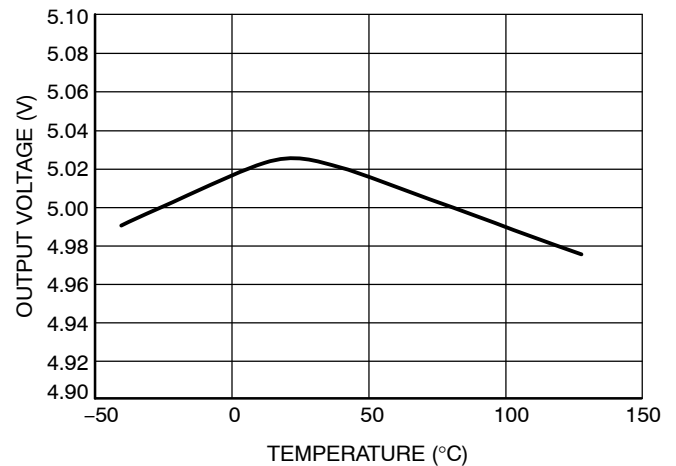


Figure 7. Output Voltage vs. Temperature (5 V Version)

TYPICAL CHARACTERISTIC CURVES – 5 V Version

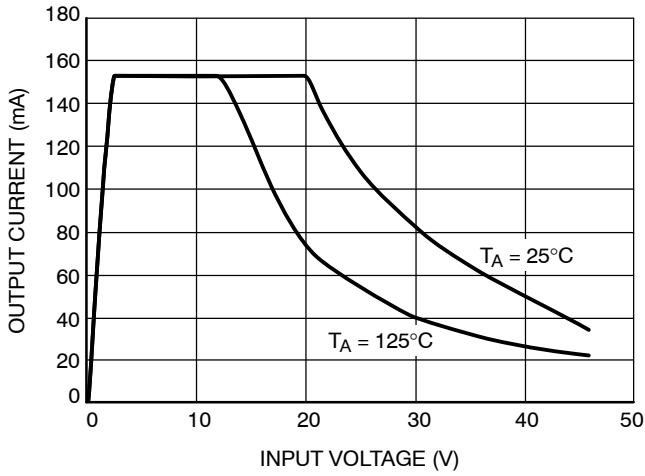


Figure 8. Output Current vs. Input Voltage (5 V Version)

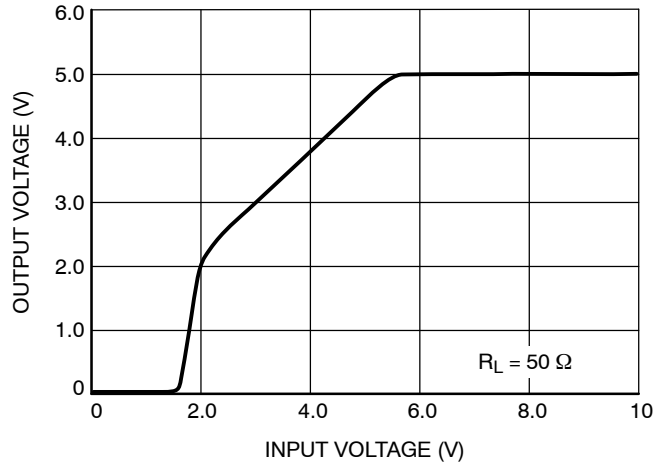


Figure 9. Output Voltage vs. Input Voltage (5 V Version)

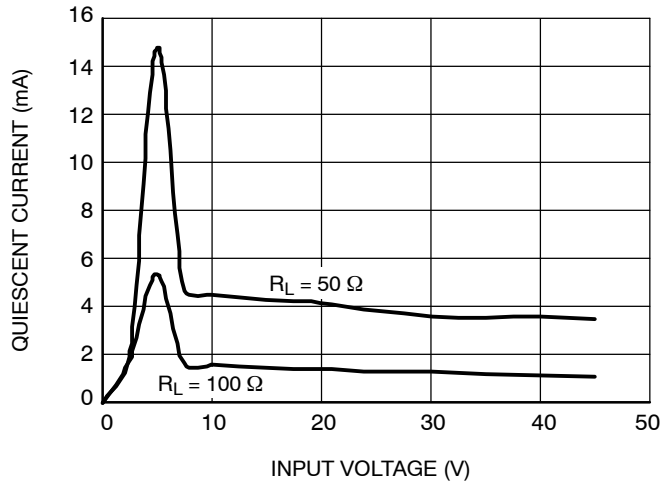


Figure 10. Quiescent Current vs. Input Voltage (5 V Version)

TYPICAL CHARACTERISTIC CURVES – 3.3 V Version

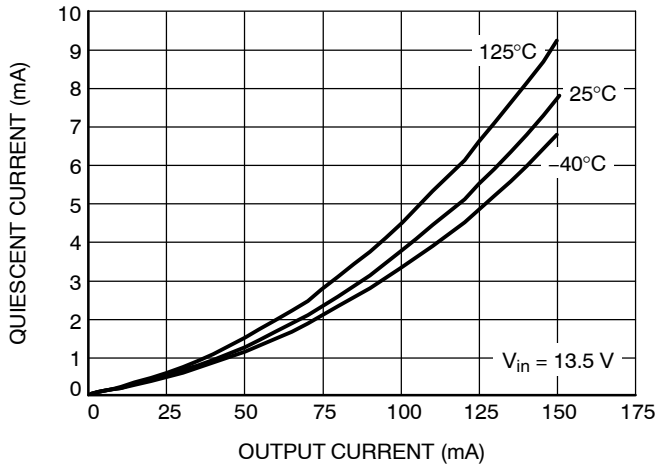


Figure 11. Quiescent Current vs. Output Current (3.3 V Version)

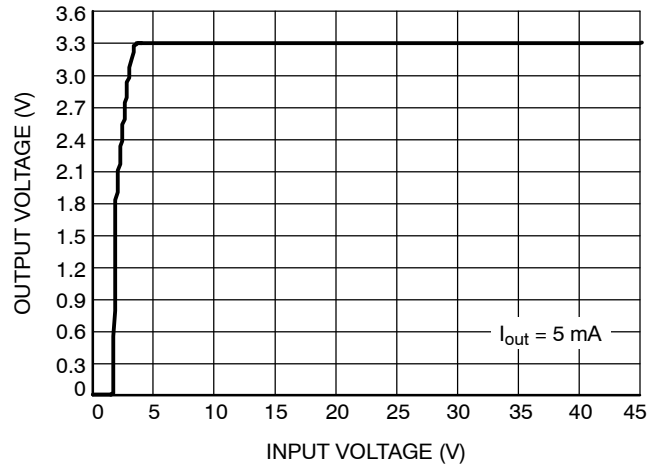


Figure 12. Output Voltage vs. Input Voltage (3.3 V Version)

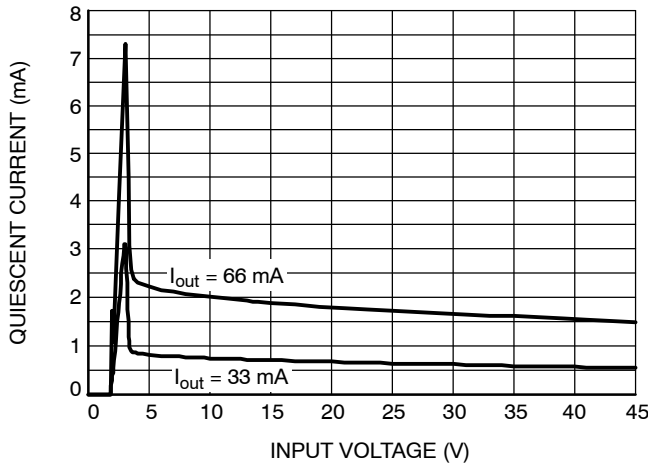


Figure 13. Quiescent Current vs. Input Voltage (3.3 V Version)

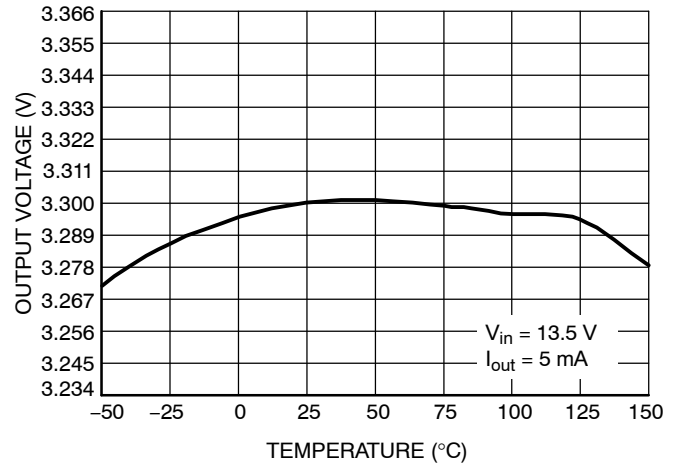


Figure 14. Output Voltage vs. Temperature (3.3 V Version)

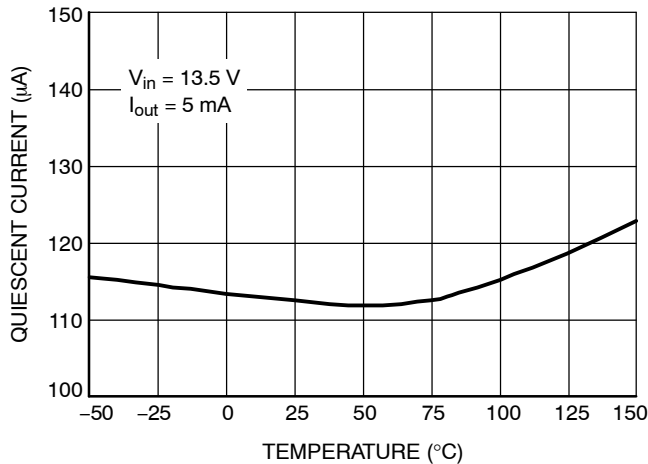


Figure 15. Quiescent Current vs. Temperature (3.3 V Version)

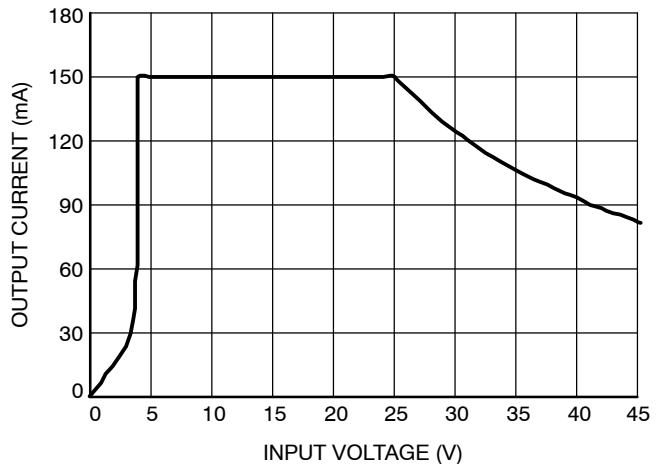
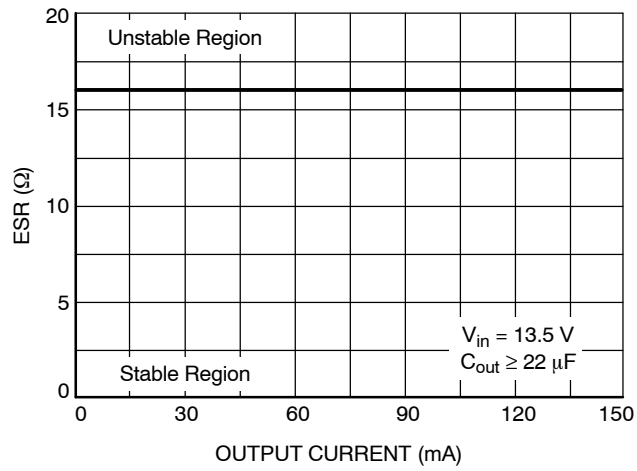


Figure 16. Output Current vs. Input Voltage (3.3 V Version)

NCV4264-2

TYPICAL CHARACTERISTIC CURVES – 3.3 V Version



**Figure 17. ESR Stability vs. Output Current
(3.3 V Version)**

Circuit Description

The NCV4264-2 is functionally and pin for pin compatible with NCV4264 with a lower quiescent current consumption. Its output stage supplies 100 mA with ±2.0% output voltage accuracy.

Maximum dropout voltage is 500 mV at 100 mA load current. It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{OUT}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature-stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor C_{I1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{I2}. The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values of C_Q ≥ 10 μF, with an ESR ≤ 9 Ω for the 5.0 V Version, and C_Q ≥ 22 μF with an ESR ≤ 16 Ω for the 3.3 V Version within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 2) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] * I_{OUT(max)} + V_{IN(max)} * I_q \tag{eq. 1}$$

Where:

V_{IN(max)} is the maximum input voltage,

V_{OUT(min)} is the minimum output voltage,

I_{OUT(max)} is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at I_{OUT(max)}. Once the value of P_{D(max)} is known, the maximum permissible value of R_{θJA} can be calculated:

$$R_{\theta JA} = \frac{(150^\circ C - T_A)}{P_D} \tag{eq. 2}$$

The value of R_{θJA} can then be compared with those in the package section of the data sheet. Those packages with R_{θJA}'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of R_{θJA}:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \tag{eq. 3}$$

Where:

R_{θJC} = the junction-to-case thermal resistance,

R_{θCS} = the case-to-heat sink thermal resistance, and

R_{θSA} = the heat sink-to-ambient thermal resistance.

R_{θJA} appears in the package section of the data sheet. Like R_{θJA}, it too is a function of package type. R_{θCS} and R_{θSA} are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

NCV4264-2

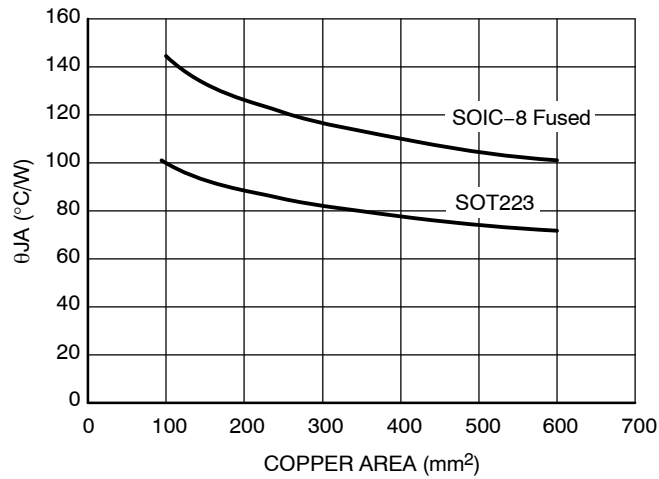


Figure 18. θ_{JA} vs. Copper Spreader Area

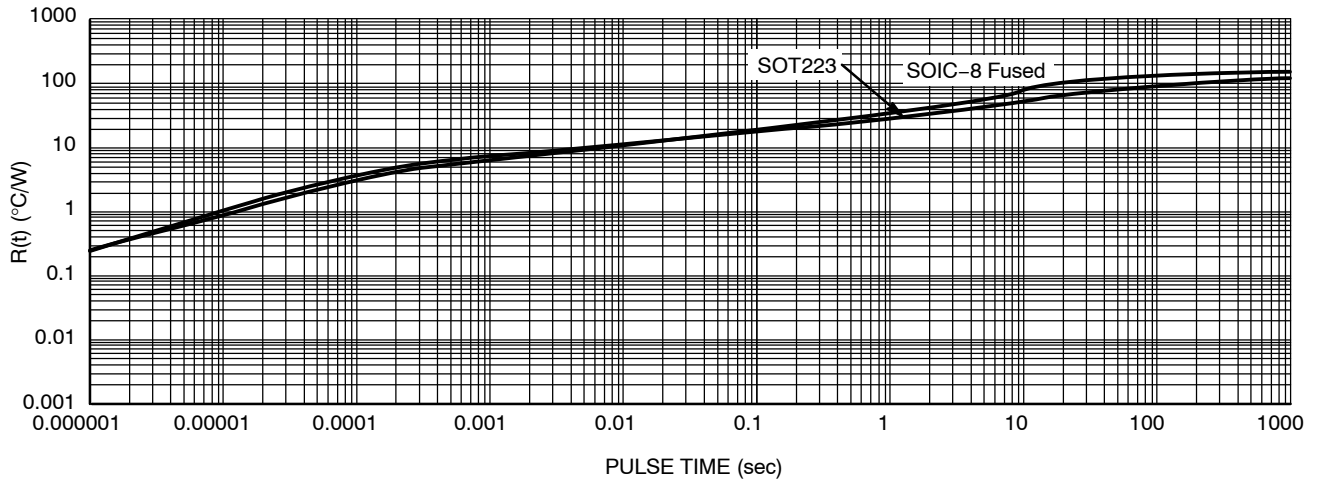


Figure 19. $R(t)$ vs. Pulse Time

ORDERING INFORMATION

Device*	Package	Shipping†
NCV4264-2ST50T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV4264-2ST33T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV4264-2D33R2G	SOIC-8 Fused (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

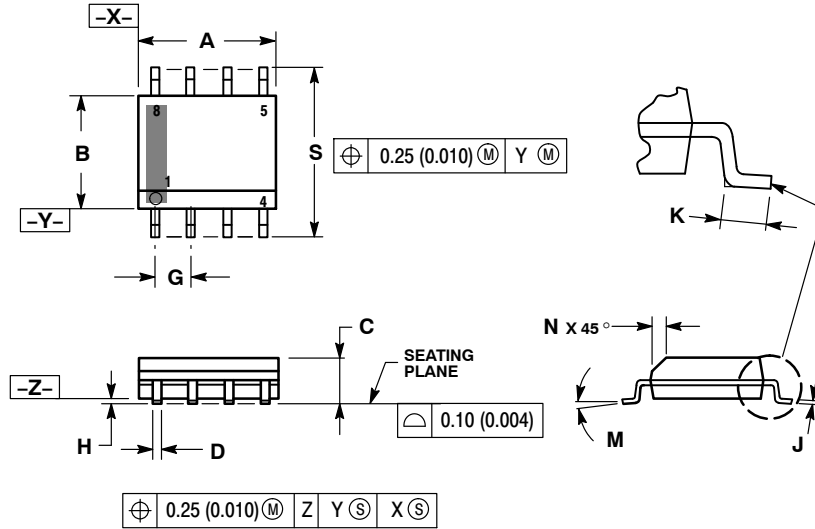
ON Semiconductor®



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

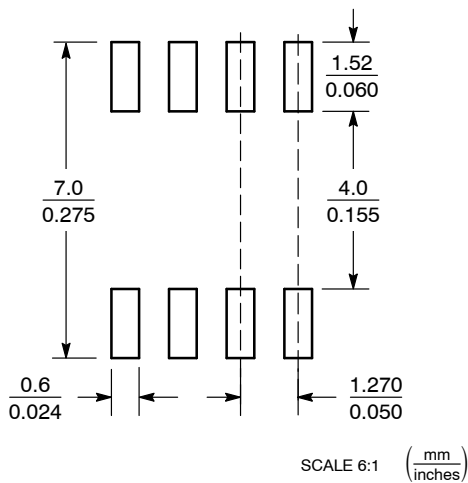
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

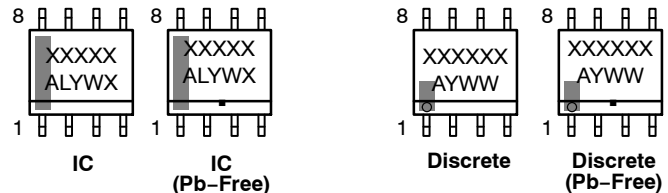
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|--|---|---|---|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

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