CPC5610/CPC5611

LITELINK™ II Silicon Data Access Arrangement (DAA) IC

Features

- Full-duplex data and voice transmission
- Transformerless telephone line isolation interface
- Operates at all modem speeds, including V.90 (56K)
- 3.3 or 5 V power supply operation
- Half-wave ring detector (CPC5610) or full-wave ring detector (CPC5611)
- Caller ID signal reception
- Small 32-pin SOIC plastic package
- Printed-circuit board space and cost savings
- Meets PC Card (PCMCIA) height requirements
- Easy interface with modem ICs and voice CODECs
- Worldwide dial-up telephone network compatibility
- Supplied application circuit complies with the requirements of TIA/EIA/IS-968 (FCC part 68), UL1950, UL60950, EN60950, IEC60950, EN55022B, CISPR22B, EN55024, and TBR-21
- CPC5610 and CPC5611 comply with UL1577
- TTL compatible logic inputs and outputs
- Line-side circuit powered from telephone line

Applications

- Satellite and cable set-top boxes
- V.90 (and other standard) modems
- Fax machines
- Voicemail systems
- Computer telephony
- PBXs
- Telephony gateways
- Embedded modems for such applications as POS terminals, automated banking, remote metering, vending machines, security, and surveillance

Description

Clare CPC5610 and CPC5611 LITELINKs are silicon data access arrangement (DAA) ICs used in data and voice communication applications to make connections to the public switched telephone network (PSTN). LITELINK uses on-chip optical components and a few inexpensive external components to form a complete voice or high-speed data telephone line interface.

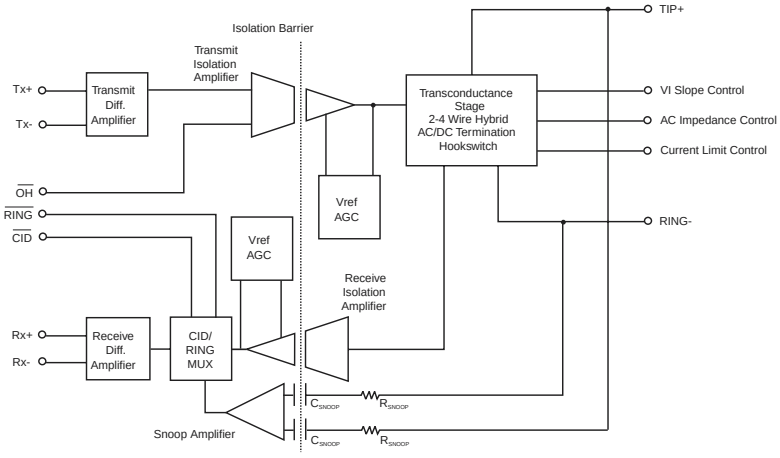
LITELINK eliminates the need for the large isolation transformers or capacitors as used in other DAA configurations. It incorporates the required high-voltage isolation barrier in the surface-mount SOIC package.

The CPC5610 (half-wave ring detect) and CPC5611 (full-wave ring detect) build upon Clare's existing LITELINK line, with improved performance and 3.3 V operation.

Ordering Information

Part Number	Description
CPC5610A	32-pin surface mount DAA with half-wave ring detect, tubed
CPC5610ATR	32-pin surface mount DAA with half-wave ring detect, tape and reel
CPC5611A	32-pin surface mount DAA with full-wave ring detect, tubed
CPC5611ATR	32-pin surface mount DAA with full-wave ring detect, tape and reel

Figure 1. CPC5610/CPC5611 Block Diagram



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1. Electrical Specifications

1.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Isolation Voltage	1500	-	V_{RMS}
Continuous Tip to Ring Current (R_{ZDC} = 5.2Ω)		150	mA
Total Package Power Dissipation		1	W
Operating temperature	0	+85	°C
Storage temperature	-40	+125	°C
Soldering temperature	-	+220	°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

1.2 Performance

Parameter	Minimum	Typical	Maximum	Unit	Conditions
DC Characteristics					
Operating Voltage V_{DD}	3.0	-	5.50	V	Host side
Operating Current I_{DD}	-	-	10	mA	Host side
Operating Voltage V_{DDL}	2.8	-	3.2	V	Line side, derived from tip and ring
Operating Current I_{DDL}	-	10.5	12	mA	Line side, drawn from tip and ring while off-hook
On-hook Characteristics					
Metallic DC Resistance	10	-	-	MΩ	Tip to ring, 100 Vdc applied
Longitudinal DC Resistance	10	-	-	MΩ	150 Vdc applied from tip and ring to Earth ground
Ring Signal Detect Level	5	-	-	V_{RMS}	68 Hz ring signal applied to tip and ring
Ring Signal Detect Level	28	-	-	V_{RMS}	15 Hz ring signal applied across tip and ring
Snoop Circuit Frequency Response	166	-	>4000	Hz	-3 dB corner frequency @ 166 Hz
Snoop Circuit CMRR	-	-40	-	dB	120 V_{RMS} 60 Hz common mode signal across tip and ring
Ringer Equivalence	-	0.1B	-	REN	
Longitudinal Balance	60	-	-	dB	Per FCC part 68.3
Off-Hook Characteristics					
AC Impedance	-	600	-	Ω	Tip to ring, using resistive termination application circuit
Longitudinal Balance	40	-	-	dB	Per FCC part 68.3
Return Loss	-	26	-	dB	Into 600 Ω at 1800 Hz
Transmit and Receive Characteristics					
Frequency Response	30	-	4000	Hz	-3 dB corner frequency 30 Hz
Trans-Hybrid Loss	-	36	-	dB	Into 600 Ω at 1800 Hz, with C18
Transmit and Receive Insertion Loss	-1	0	1	dB	30 Hz to 4 kHz
Average In-band Noise	-	-120	-	dBm/Hz	4 kHz flat bandwidth
Harmonic Distortion	-	-80	-	dB	-3 dBm, 600 Hz, 2nd harmonic

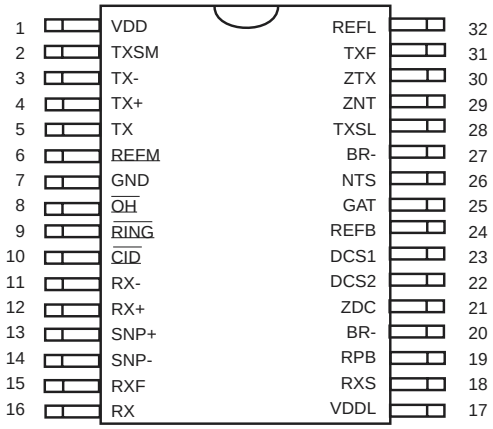
Parameter	Minimum	Typical	Maximum	Unit	Conditions
Transmit Level	-	0	2.2	V_{P-P}	Single-tone sine wave. Or 0 dBm into 600 Ω
Receive Level	-	-	2.2	V_{P-P}	Single-tone sine wave. Or 0 dBm into 600 Ω
RX+/RX- Output Drive Current	-	-	0.5	mA	Sink and source
TX+/TX- Input Impedance	60	90	120	kΩ	
Isolation Characteristics					
Isolation Voltage	1500	-	-	V_{RMS}	Line side to host side
Surge Rise Time	2000	-	-	V/μS	No damage via tip and ring
$\overline{OH}$ and $\overline{CID}$ Control Logic Inputs					
Input Threshold Voltage	0.8	-	2.0	V	
High Level Input Current	-120	-	0	μA	$V_{IN} \leq V_{DD}$
Low Level Input Current	-	-	-120	μA	V_{IN}=GND
$\overline{RING}$ Output Logic Levels					
Output High Voltage	V_{DD} -0.4	-	-	V	I_{OUT} = -400 μA
Output Low Voltage	-	-	0.4	V	I_{OUT} = 1 mA

Specifications subject to change without notice. All performance characteristics based on the use of Clare, Inc. application circuits. Functional operation of the device at conditions beyond those specified here is not implied. Specification conditions: V_{DD} = 5V, temperature = 25 °C, unless otherwise indicated.

1.3 Pin Description

Pin	Name	Function
1	VDD	Host (CPE) side power supply
2	TXSM	Transmit summing junction
3	TX-	Negative differential transmit signal to DAA from host
4	TX+	Positive differential transmit signal to DAA from host
5	TX	Transmit differential amplifier output
6	REFM	Internal voltage reference
7	GND	Host (CPE) side analog ground
8	$\overline{OH}$	Assert logic low for off-hook operation
9	$\overline{RING}$	Indicates ring signal, pulsed high to low
10	$\overline{CID}$	Assert logic low while on hook to place CID information on RX pins.
11	RX-	Negative differential analog signal received from the telephone line. Must be AC coupled with 0.1 µF.
12	RX+	Positive differential analog signal received from the telephone line. Must be AC coupled with 0.1 µF.
13	SNP+	Positive differential snoop input
14	SNP-	Negative differential snoop input
15	RXF	Receive photodiode amplifier output
16	RX	Receive photodiode summing junction
17	VDDL	Power supply for line side, regulated from tip and ring.
18	RXS	Receive isolation amp summing junction
19	RPB	Receive LED pre-bias current set
20	BR-	Bridge rectifier return
21	ZDC	Electronic inductor and DC current limit
22	DCS2	DC feedback output
23	DCS1	V to I slope control
24	REFB	0.625 Vdc reference
25	GAT	External MOSFET gate control
26	NTS	Receive signal input
27	BR-	Bridge rectifier return
28	TXSL	Transmit photodiode summing junction
29	ZNT	Receiver impedance set
30	ZTX	Transmit transconductance gain set
31	TXF	Transmit photodiode amplifier output
32	REFL	1.25 Vdc reference

Figure 2. Pinout



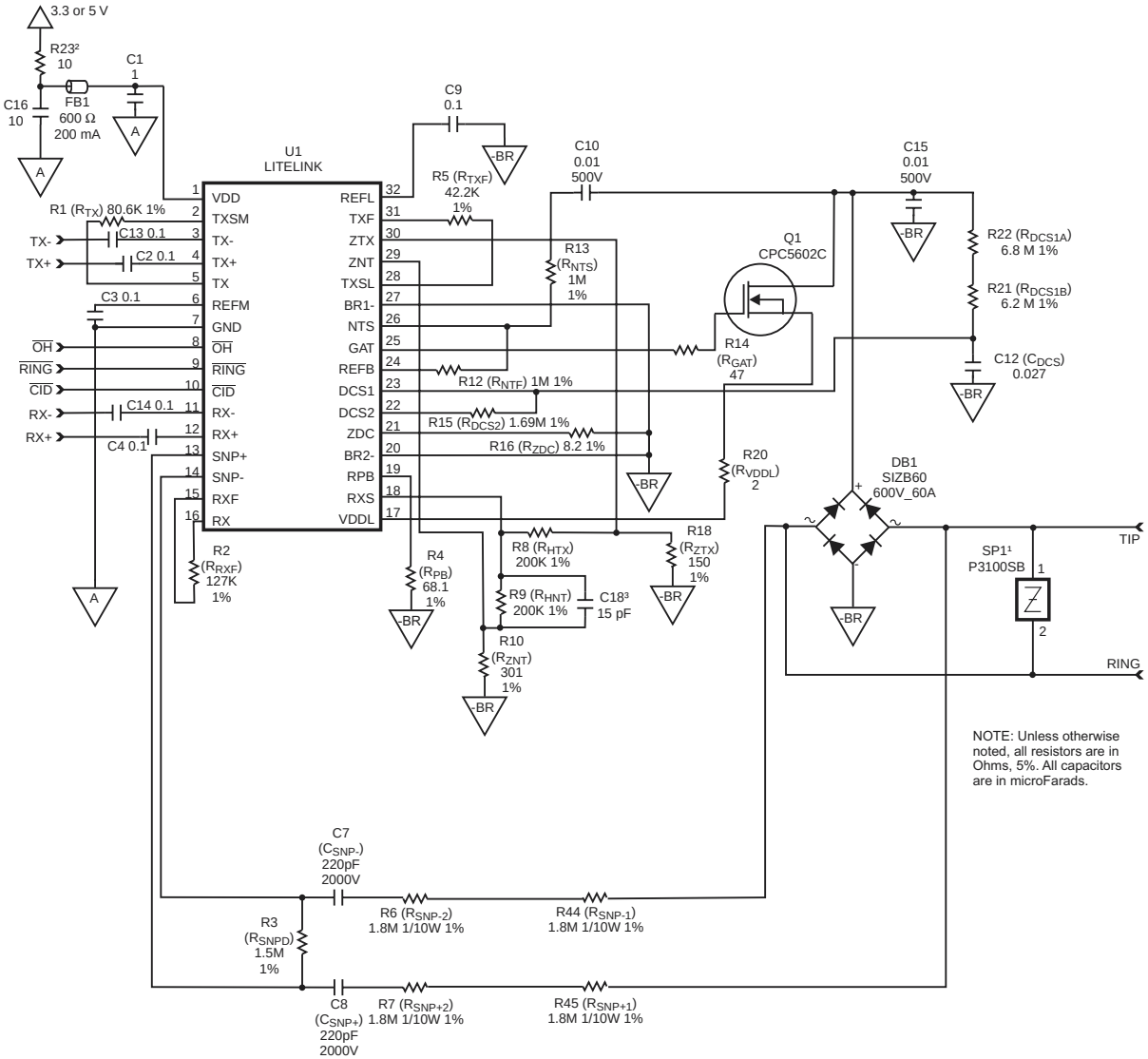
2. Application Circuits

LITELINK can be used with telephone networks worldwide. Some public telephone networks, notably in North America and Japan require resistive line temrination. Other telephone networks in Europe and elsewhere require reactive line termination.

The application circuits below address both line termination models. The reactive termination application circuit **(see Section 2.2 on page 8)** describes a TBR-21 implementation. This circuit can be adapted easily for other reactive termination needs. Worldwide application of LITELINK is described more fully in Clare application note AN-147, **Worldwide Application of LITELINK**.

2.1 Resistive Termination Application Circuit

Figure 3. Resistive Termination Application Circuit Schematic



[1]*This design was tested and found to comply with FCC Part 68 with this part. Other compliance requirements may require a different part.*

[2]*Higher-noise power supplies may require substitution of a 220 µH inductor, Toko 380HB-2215 or similar. See the Power Quality section of Clare application note AN-146,* ***Guidelines for Effective LITELINK Designs*** *for more information.*

[3]*Optional for enhanced trans-hybrid loss, see* ***"Trans-Hybrid Loss" on page 16.***

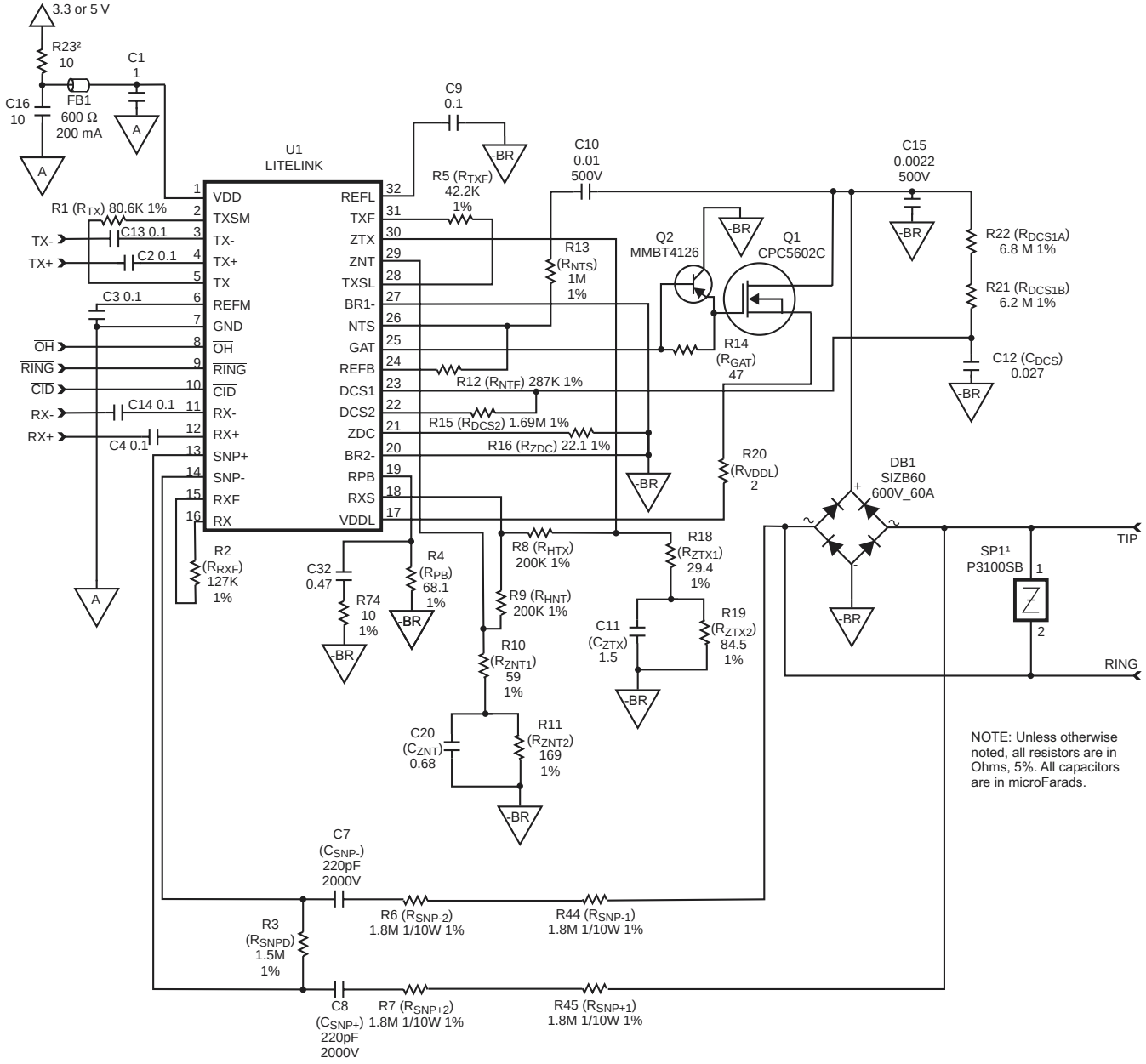
2.1.1 Resistive Termination Application Circuit Part List

Quantity	Reference Designator	Description	Suppliers
1	C1	1 µF, 16 V, ±10%	Panasonic, AVX, Novacap, Murata, SMEC, etc.
6	C2, C3, C4, C9, C13, C14	0.1 µF, 16 V, ±10%	
2	C7, C8[1]	220 pF, 2 kV, ±5%	
2	C10, C15[1]	0.01 µF, 500 V, ±10%	
1	C12	0.027 µF, 16 V, ±10%	
1	C16	10 µF, 16 V, ±10%	
1	C18 (optional)	15 pF, 16V, ±10%	
1	R1	80.6 kΩ, 1/16 W, ±1%	Panasonic, Electro Films, FMI, Vishay, etc.
1	R2	127 kΩ, 1/16 W, ±1%	
1	R3	1.5 MΩ, 1/16 W, ±1%	
1	R4	68.1 Ω, 1/16 W, ±1%	
1	R5	42.2 kΩ, 1/16 W, ±1%	
4	R6, R7, R44, R45[1]	1.8 MΩ, 1/10 W, ±1%	
2	R8, R9	200 kΩ, 1/16 W, ±1%	
1	R10	301 Ω, 1/16 W, ±1%	
2	R12, R13	1 MΩ, 1/16 W, ±1%	
1	R14	47 Ω, 1/16 W, ±5%	
1	R15	1.69 MΩ, 1/16 W, ±1%	
1	R16	8.2 Ω, 1/16 W, ±1%	
1	R18	150 Ω, 1/16 W, ±1%	
1	R20	2 Ω, 1/16 W, ±5%	
1	R21	6.2 MΩ, 1/16 W, ±1%	
1	R22	6.8 MΩ, 1/16 W, ±1%	
1	R23	10 Ω, 1/16 W, ±5%, or 220 µH inductor	
1	FB1	600 Ω, 200 mA ferrite bead	Murata BLM11A601S or similar
1	DB1	SIZB60, 600 V, 60 A bridge rectifier	Shindengen, Diodes, Inc.
1	SP1	350 V, 100 A Sidactor	Teccor, ST Microelectronics, TI
1	Q1	CPC5602 FET	Clare
1	U1	CPC5610 LITELINK	

[1] *Through-hole components offer significant cost savings over SMT.*

2.2 Reactive Termination Application Circuit

Figure 4. Reactive Termination Application Circuit Schematic



[1]*This design was tested and found to comply with FCC Part 68 with this part. Other compliance requirements may require a different part.*

[2]*Higher-noise power supplies may require substitution of a 220 µH inductor, Toko 380HB-2215 or similar. See the Power Quality section of Clare application note AN-146,* ***Guidelines for Effective LITELINK Designs*** *for more information.*

2.2.1 Reactive Termination Application Circuit Part List

Quantity	Reference Designator	Description	Supplier
1	C1	1 µF, 16 V, ±10%	Panasonic, AVX, Novacap, Murata, SMEC, etc.
6	C2, C3, C4, C9, C13, C14	0.1 µF, 16 V, ±10%	
1	C5	0.47 µF, 16 V, ±10%	
2	C7, C8[1]	220 pF, 2 kV, ±5%	
2	C10[1]	0.01 µF, 500 V, ±10%	
1	C11	1.5 µF, 16 V, ±10%	
1	C12	0.027 µF, 16 V, ±10%	
1	C15[1]	0.0022 µF, 500 V, ±10%	
1	C16	10 µF, 16 V, ±10%	
1	C20	0.68 µF, 16 V, ±10%	
1	C32	0.47 µF, 16 V, ±10%	
1	R1	80.6 kΩ, 1/16 W, ±1%	Panasonic, Electro Films, FMI, Vishay, etc.
1	R2	127 kΩ, 1/16 W, ±1%	
1	R3	1.5 MΩ, 1/16 W, ±1%	
1	R4	68.1 Ω, 1/16 W, ±1%	
1	R5	42.2 kΩ, 1/16 W, ±1%	
4	R6, R7, R44, R45[1]	1.8 MΩ, 1/10 W, ±1%	
2	R8, R9	200 kΩ, 1/16 W, ±1%	
1	R10	59 Ω, 1/16 W, ±1%	
1	R11	169 Ω, 1/16 W, ±1%	
1	R12	287 kΩ, 1/16 W, ±1%	
1	R13	1 MΩ, 1/16 W, ±1%	
1	R14	47 Ω, 1/16 W, ±5%	
1	R15	1.69 MΩ, 1/16 W, ±1%	
1	R16	22.1 Ω, 1/16 W, ±1%	
1	R18	29.4 Ω, 1/16 W, ±1%	
1	R19	84.5 Ω, 1/16 W, ±1%	
1	R20	2 Ω, 1/16 W, ±5%	
1	R21	6.2 MΩ, 1/16 W, ±1%	
1	R22	6.8 MΩ, 1/16 W, ±1%	
1	R23	10 Ω, 1/16 W, ±5%, or 220 µH inductor	
1	R74	10 Ω, 1/16 W, ±1%	
1	FB1	600 Ω, 200 mA ferrite bead	Murata BLM11A601S or similar
1	DB1	SIZB60, 600 V, 60 A bridge rectifier	Shindengen, Diodes, Inc.
1	SP1	350 V, 100 A Sidactor	Teccor, ST Microelectronics, TI
1	Q1	CPC5602 FET	Clare
1	Q2	MMBT4126	Fairchild
1	U1	CPC5610 LITELINK	Clare

[1] *Through-hole components offer significant cost savings over SMT.*

3. Using LITELINK

As a full-featured telephone line interface, LITELINK performs the following functions:

- DC termination
- AC impedance control
- V/I slope control
- 2-wire to 4-wire conversion (hybrid)
- Current limiting
- Ring detection
- Caller ID signal reception
- Switch hook

LITELINK can accommodate specific application features without sacrificing basic functionality and performance. Application features include, but are not limited to:

- High gain (+3 dBm) operation
- Pulse dialing
- Ground start
- Loop start
- Parallel telephone off-hook detection (911 feature)
- Battery reversal
- Line presence
- World-wide programmable operation

This section of the data sheet describes LITELINK operation in standard configuration for usual operation. Clare offers additional application information online **(see Section 5 on page 14)**. These include information on the following topics:

- Circuit isolation considerations
- Optimizing LITELINK performance
- Data Access Arrangement architecture
- LITELINK circuit descriptions
- Surge protection
- EMI considerations

Other specific application materials are also referenced in this section as appropriate.

3.1 Switch Hook Control (On-hook and Off-hook States)

LITELINK operates in one of two conditions, on-hook and off-hook. In the on-hook condition the telephone line is available for calls. In the off-hook condition the telephone line is engaged. Use the $\overline{OH}$ control input to place LITELINK in one of these two states. With $\overline{OH}$ high, LITELINK is on-hook and ready to make or receive a call. The snoop circuit is enabled. Assert $\overline{OH}$ low to place LITELINK in the off-hook state. In the off-hook state, loop current flows through LITELINK and the system is answering or placing a call.

3.2 On-hook Operation

The LITELINK application circuit leakage current is less than 10 µA with 100 V across ring and tip, equivalent to greater than 10 MΩ on-hook resistance.

3.2.1 Ring Signal Detection via the Snoop Circuit

In the on-hook state ($\overline{OH}$ and $\overline{CID}$ not asserted), an internal multiplexer turns on the snoop circuit. This circuit monitors the telephone line for two conditions; an incoming ring signal, and caller ID data bursts.

Refer to the application schematic diagram **(see Figure 3 on page 6)**. C7 (C_{SNP-}) and C8 (C_{SNP+}) provide a high-voltage isolation barrier between the telephone line and SNP- and SNP+ on the LITELINK while coupling AC signals to the snoop amplifier. The snoop circuit “snoops” the telephone line continuously while drawing no current. In the LITELINK, ringing signals are compared to a threshold. The comparator output forms the $\overline{RING}$ signal output from LITELINK. This signal must be qualified by the host system as a valid ringing signal. A low level on $\overline{RING}$ indicates that the LITELINK ring signal threshold has been exceeded.

For the CPC5610 (with the half-wave ring detector), the frequency of the $\overline{RING}$ output follows the frequency of the ringing signal from the central office (CO), typically 20 Hz. The $\overline{RING}$ output of the CPC5611 (with the full-wave ring detector) is twice the ringing signal frequency.

Hysteresis is employed in the LITELINK ring detector circuit to provide noise immunity. The setup of the ring detector comparator causes $\overline{RING}$ output pulses to remain low for most of the ringing signal half-cycle. The $\overline{RING}$ output returns high for the entire negative half-cycle of the ringing signal for the CPC5610. For the CPC5611, the $\overline{RING}$ output returns high for a short period near the zero-crossing of the ringing signal before returning low during the positive half-cycle. For both the CPC5610 and CPC5611, the $\overline{RING}$ output remains high between ringing signal bursts.

The ring detection threshold depends on the values of R3 (R_{SNPD}), R6 (R_{SNP-}), R7 (R_{SNP+}), C7 (C_{SNP-}), and C8 (C_{SNP+}). The values for these components shown in the typical application circuits are recommended for

typical operation. The ring detection threshold can be changed according to the following formula:

$$V_{RINGPK} = \left(\frac{750mV}{R_3}\right)\sqrt{\left[(2R_6 + R_3)^2 + \frac{1}{(\pi f_{RING} C_7)^2}\right]}$$

Clare Application Note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold** is a spreadsheet for trying different component values in this circuit. Changing the ring detection threshold will also change the caller ID gain and the timing of the polarity reversal detection pulse, if used.

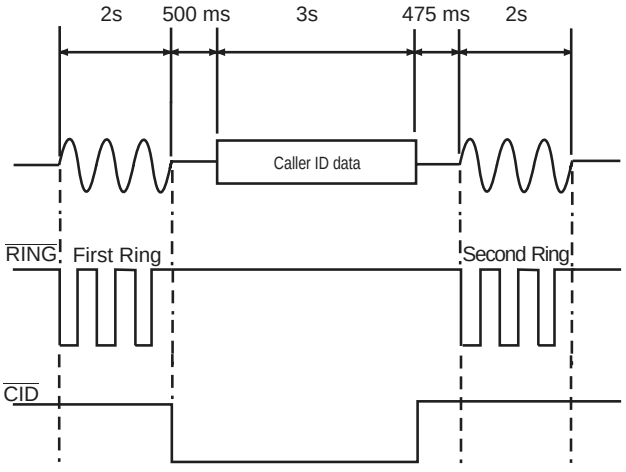
3.2.2 Polarity Reversal Detection with CPC5611

The full-wave ring detector in the CPC5611 makes it possible to detect tip and ring polarity reversal using the $\overline{\text{RING}}$ output. When the polarity of tip and ring reverses, a pulse on $\overline{\text{RING}}$ indicates the event. Your host system must be able to discriminate this single pulse of approximately 1 msec (using the recommended snoop circuit external components) from a valid ringing signal.

3.2.3 On-hook Caller ID Signal Processing

On-hook caller ID (CID) signals are processed by LITELINK by coupling the CID data burst through the snoop circuit to the LITELINK RX outputs under control of the $\overline{\text{CID}}$ pin. In North America, CID data signals are typically sent between the first and second ringing signal.

Figure 5. On-hook Caller ID Signal Timing in North America for CPC5610 (with Half-wave Ring Detect)



Signal levels not to scale

In North American applications, follow these steps to receive on-hook caller ID data via the LITELINK RX outputs:

1. Detect the first ringing signal outputs on $\overline{\text{RING}}$.
2. Assert $\overline{\text{CID}}$ low.
3. Process the CID data from the RX outputs.
4. De-assert $\overline{\text{CID}}$ (high or floating).

Note: Taking LITELINK off-hook (via the $\overline{\text{OH}}$ pin) disconnects the snoop path from both the receive outputs and the $\overline{\text{RING}}$ output, regardless of the state of the $\overline{\text{CID}}$ pin.

CID gain from tip and ring to RX+ and RX- is determined by:

$$GAIN_{CID}(dB) = 20\log\left[\frac{6R_3}{\sqrt{\left[(2R_6 + R_3)^2 + \frac{1}{(\pi f C_7)^2}\right]}}\right]$$

where f is the frequency of the CID data signal.

The recommended components in the application circuit yield a gain 0.27 dB at 200 Hz. Clare Application Note AN-117 **Customize Caller ID Gain and Ring Detect Voltage Threshold** is a spreadsheet for trying different component values in this circuit. Changing the CID gain will also change the ring detection threshold and the timing of the polarity reversal detection pulse, if used.

For single-ended snoop circuit output of 0 dBm, set the total resistance across the series resistors (R6/R44 and R7/R45) to 1.4 MΩ.

3.3 Off-Hook Operation

3.3.1 Receive Signal Path

Signals to and from the telephone network appear on the tip and ring connections of the application circuit. Receive signals are extracted from transmit signals by the LITELINK two-wire to four-wire hybrid. Next, the receive signal is converted to infrared light by the receive photodiode amplifier and receive path LED. The intensity of the light is modulated by the receive signal and coupled across the electrical isolation barrier by a reflective dome.

On the host equipment side of the barrier, the receive signal is converted by a photodiode into a photocur-

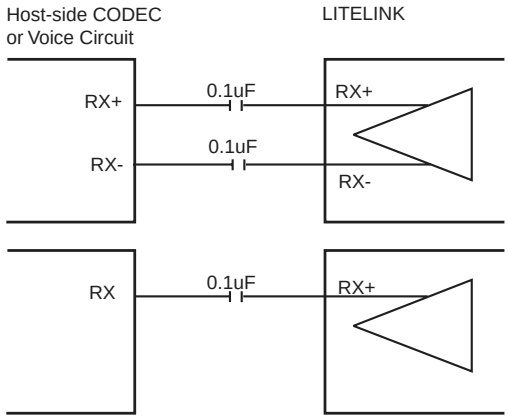
rent. The photocurrent, a linear representation of the receive signal, is amplified and converted to a differential voltage output on RX+ and RX-.

Variations in gain are controlled to within ±1 dB by an on-chip automatic gain control (AGC) circuit, which sets the output of the photoamplifier to unity gain.

To accommodate single-supply operation, LITELINK includes a small DC bias on the RX outputs of 1.0 Vdc. Most applications should AC couple the RX outputs as shown in Figure 6.

LITELINK may be used for differential or single-ended output as shown in Figure 6. Single-ended use will produce 6 dB less signal output amplitude. Do not exceed 0 dBm into 600 Ω (2.2 V_{P-P}) signal input.

Figure 6. Differential and Single-ended Receive Path Connections to LITELINK

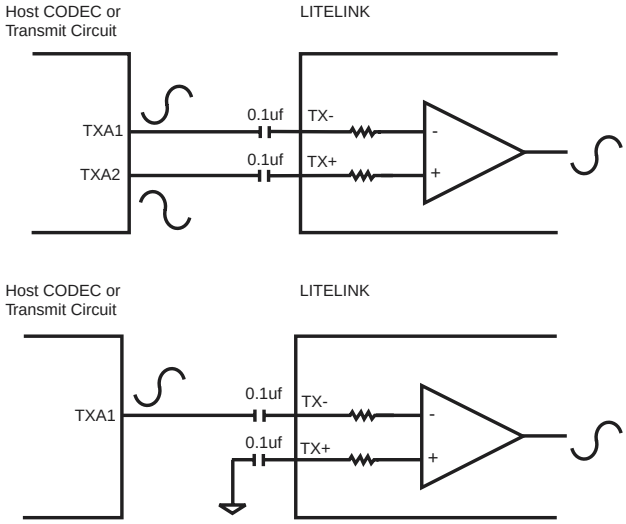


3.3.2 Transmit Signal Path

Connect transmit signals from the host equipment to the TX+ and TX- pins of LITELINK. Do not exceed a signal level of 0 dBm in 600 Ω (or 2.2 V_{P-P}). Differential transmit signals are converted to single-ended signals in LITELINK. The signal is coupled to the transmit photodiode amplifier in a similar manner to the receive path.

The output of the photodiode amplifier is coupled to a voltage-to-current converter via a transconductance stage where the transmit signal modulates the telephone line loop current. As in the receive path, gain is set to unity automatically, limiting insertion loss to 0, ±1 dB.

Figure 7. Differential and Single-ended Transmit Path Connections to LITELINK



3.4 DC Characteristics

The CPC5610 and CPC5611 are designed for worldwide application regarding DC characteristics, including use under the requirements of TBR-21. The ZDC, DCS1, and DCS2 pins control the VI slope characteristics of LITELINK. Selecting appropriate resistor values for R_{ZDC} (R16) and R_{DCS} (R15) in the provided application circuits assure compliance with DC requirements.

3.4.1 Resistive Termination Applications

LITELINK includes a telephone line current limit feature that is selectable by selecting the desired value for R_{ZDC} (R16) using the following formula:

$$I_{CL}Amps = \frac{1V}{R_{ZDC}} + 0.011A$$

Clare recommends using 8.2 Ω for R_{ZDC} in North America and Japan, limiting telephone line current to 133 mA.

3.4.2 Reactive Termination Applications

TBR-21 sets the telephone line current limit at 60 mA. To meet this requirement, set R_{ZDC} (R16) to 22.1 Ω.

See Clare application note AN-146 **Guidelines for Effective LITELINK Designs** for information on FET heat sinking in this application.

3.5 AC Characteristics

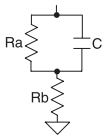
3.5.1 Resistive Termination Applications

North American and Japanese telephone line AC termination requirements are met with a resistive 600 Ω AC termination. Receive termination is applied to the LITELINK ZNT pin (pin 29) as a 301 Ω resistor, R_{ZNT} (R10). A 150 Ω resistor, R18 (R_{ZTX}), applied to the LITELINK ZTX pin (pin 30) sets the correct transmit gain and impedance.

3.5.2 Reactive Termination Applications

Many areas use a single-pole complex impedance to model the telephone network transmission line characteristic impedance as shown in the table below.

Line Impedance Model

		TBR-21	Australian
	Ra	750	820
	Rb	270	220
	C	150 nF	120 nF

Matching a complex impedance requires the use of complex networks on ZNT and ZTX. In order to accommodate high power levels, it is necessary to modify the transmit and receive gain characteristics of your LITELINK implementation. The complex network on the ZTX pin increases transmit gain by 7 dB. A 7 dB pad may be inserted before the TX+ and TX- pins to provide overall unity gain. Similarly, with a complex network, the ratio of R12 (R_{NTF}) and R13 (R_{NTS}) must be modified from 1:1 to 1:.287, which introduces a 7 dB loss in the receive path from tip and ring to ZNT.

4. Regulatory Information

LITELINK can be used to build products that comply with the requirements of TIA/EIA/IS-968 (formerly FCC part 68), FCC part 15B, TBR-21, EN60950, UL1950, EN55022B, IEC950/IEC60950, CISPR22B, EN55024, and many other standards. LITELINK complies with the requirements of UL1577. LITELINK provides supplementary isolation. Metallic surge requirements are met through the inclusion of a Sidactor in the application circuit. Longitudinal surge protection is provided by LITELINK's optical-across-the-barrier technology and the use of high-voltage components in the application circuit as needed.

The information provided in this document is intended to inform the equipment designer but it is not sufficient to assure proper system design or regulatory compliance. Since it is the equipment manufacturer's responsibility to have their equipment properly designed to conform to all relevant regulations, designers using LITELINK are advised to carefully verify that their end-product design complies with all applicable safety, EMC, and other relevant standards and regulations. Semiconductor components are not rated to withstand electrical overstress or electro-static discharges resulting from inadequate protection measures at the board or system level.

5. LITELINK Design Resources

5.1 Clare, Inc. Design Resources

The Clare, Inc. web site has a wealth of information useful for designing with LITELINK, including application notes and reference designs that already meet all applicable regulatory requirements. LITELINK data sheets also contains additional application and design information. See the following links:

LITELINK datasheets and reference designs

Application note AN-107 **LOCxx Series - Isolated Amplifier Design Principles**

Application note AN-114 **ITC117P**

Application note AN-117 **Customize Caller-ID Gain and Ring Detect Voltage Threshold for CPC5610/11**

Application note AN-140, **Understanding LITELINK**

Application note AN-141, **Enhanced Pulse Dialing with LITELINK**

Application note AN-143, **Loop Reversal Detection with LITELINK**

Application note AN-146, **Guidelines for Effective LITELINK Designs**

Application note AN-147, **Worldwide Application of LITELINK**

Application note AN-149, **Increased LITELINK II Transmit Power**

Application note AN-150, **Ground-start Supervision Circuit Using IAA110**

5.2 Third Party Design Resources

The following also contain information useful for DAA designs. All of the books are available on **amazon.com**.

Understanding Telephone Electronics, Stephen J. Bigelow, et. al., Butterworth-Heinemann; ISBN: 0750671750

Newton's Telecom Dictionary, Harry Newton, CMP Books; ISBN: 1578200695

Photodiode Amplifiers: Op Amp Solutions, Jerald Graeme, McGraw-Hill Professional Publishing; ISBN: 007024247X

Teccor, Inc. Surge Protection Products

United States Code of Federal Regulations, CFR 47 Part 68.3

6. LITELINK Performance

The following graphs show LITELINK performance using the North American application circuit shown in this data sheet.

Figure 8. Receive Frequency Response at RX

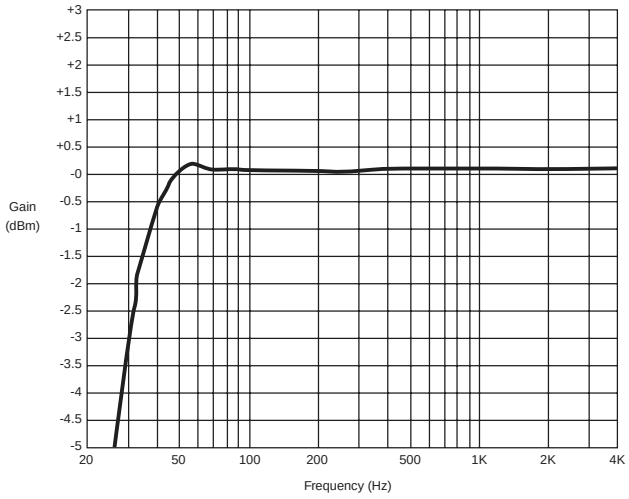


Figure 9. Transmit Frequency Response at TX

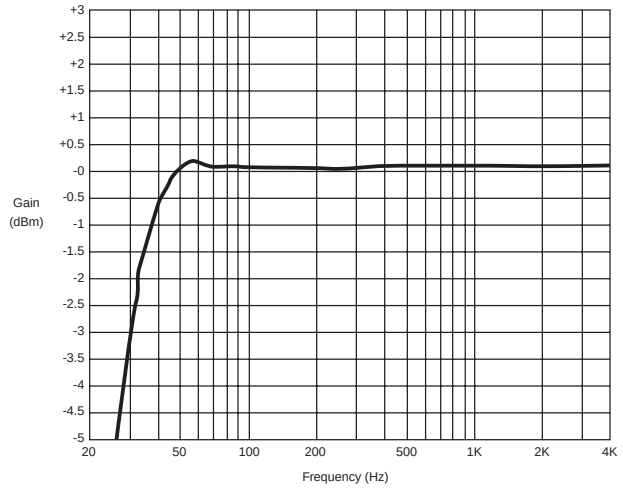


Figure 10. Receive THD on RX

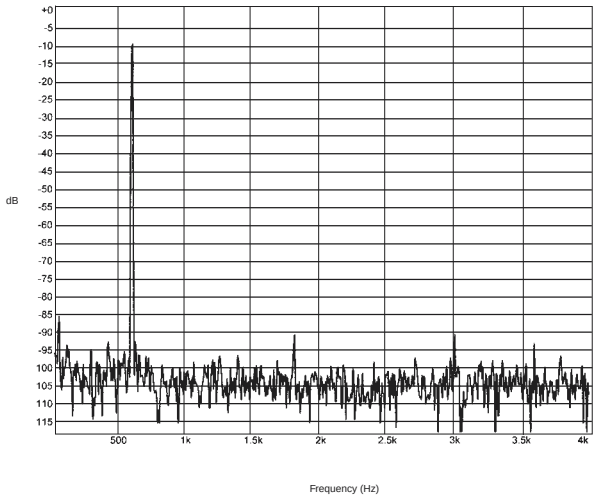


Figure 11. Transmit THD on Tip and Ring

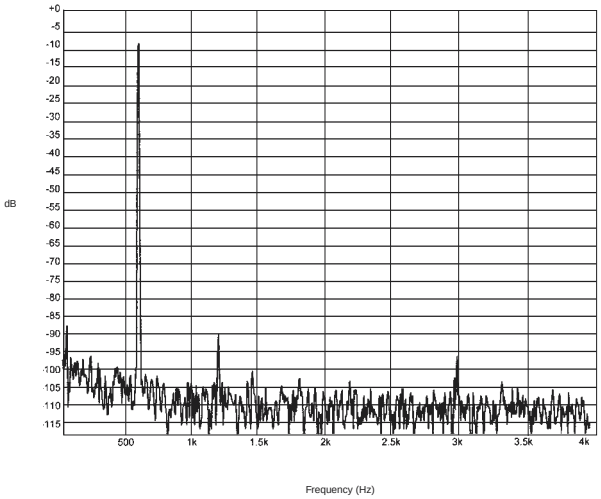


Figure 12. Trans-Hybrid Loss

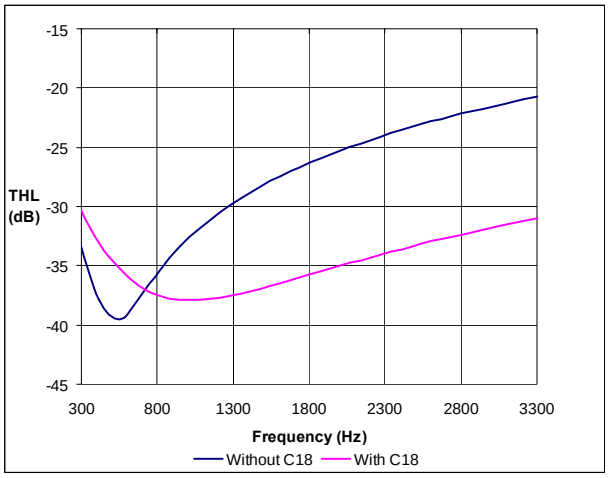


Figure 13. Return Loss

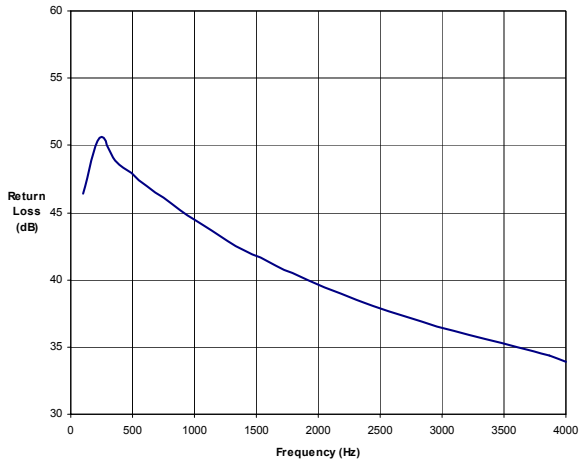


Figure 14. Snoop Circuit Frequency Response

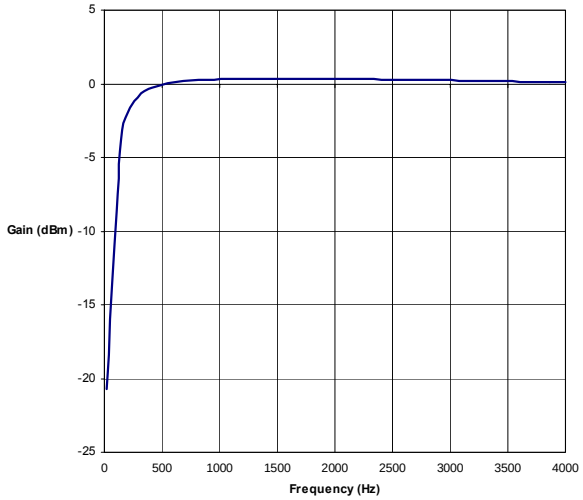


Figure 15. Snoop Circuit THD + N

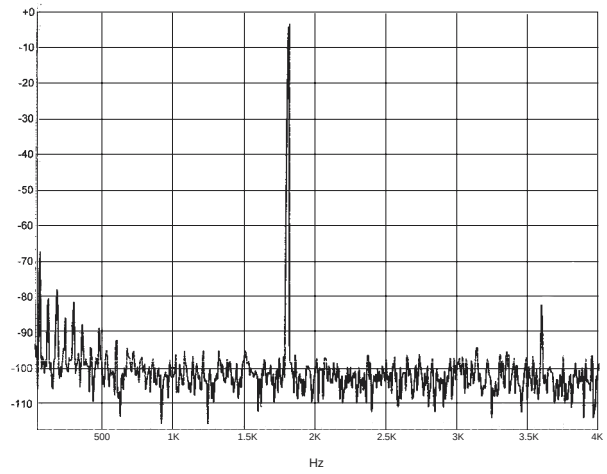
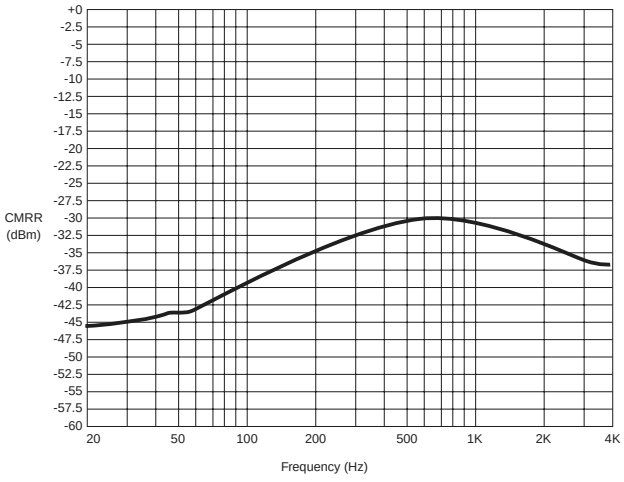


Figure 16. Snoop Circuit Common Mode Rejection



7. Manufacturing Information

7.1 Mechanical Dimensions

Figure 17. Dimensions

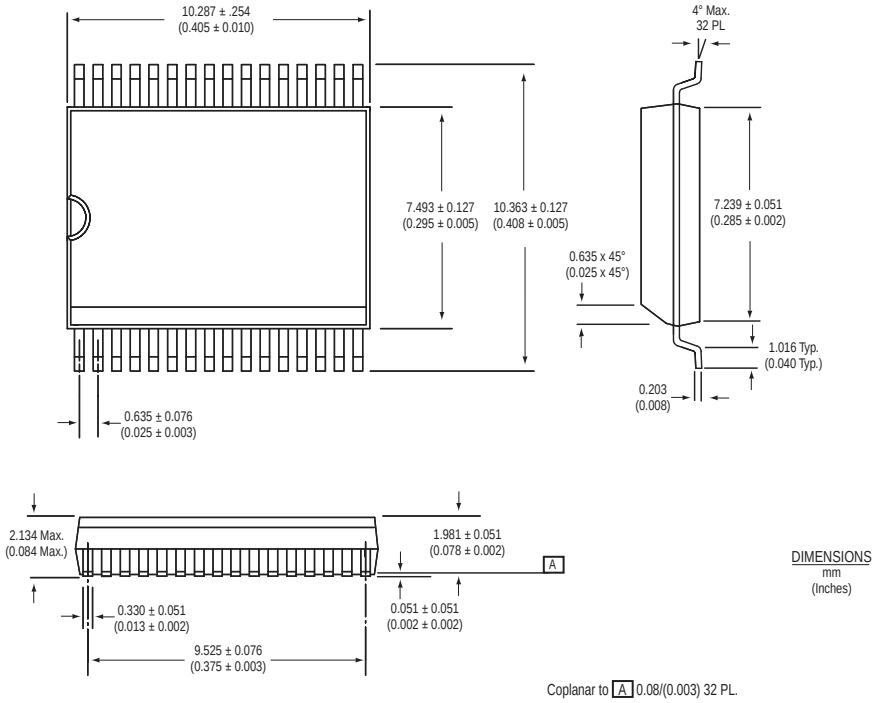
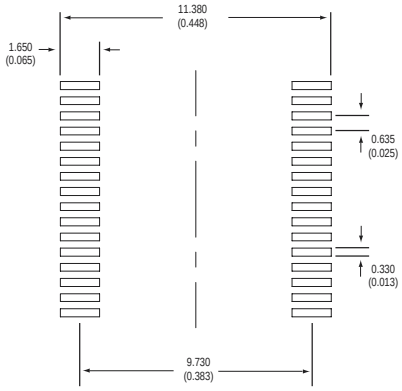
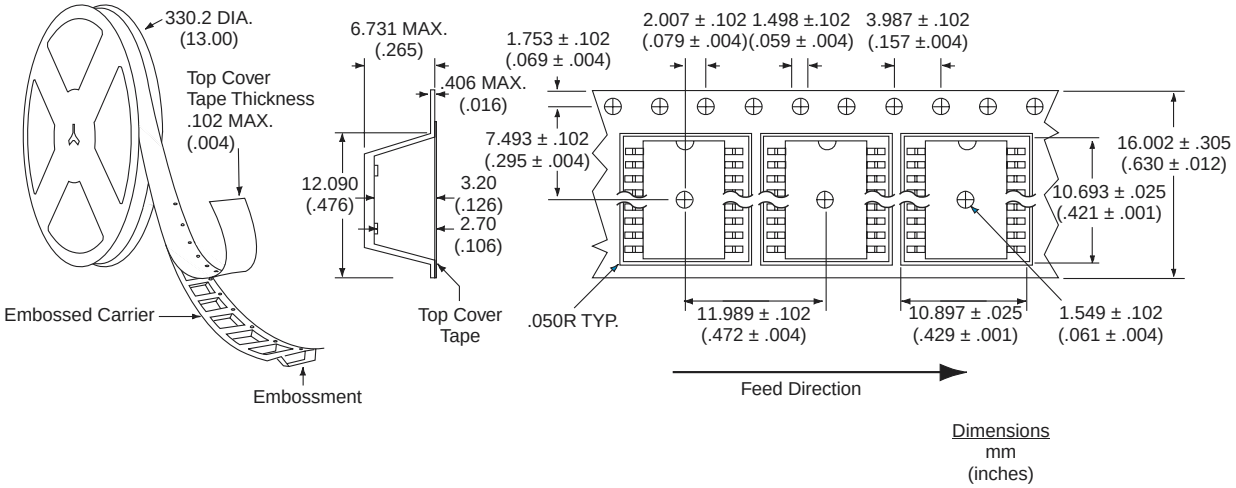


Figure 18. Recommended Printed Circuit Board Layout



7.2 Tape and Reel Packaging

Figure 19. Tape and Reel Dimensions



7.3 Soldering

7.3.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity of LITELINK using IPC/JEDEC standard J-STD-020A. Moisture uptake from atmospheric humidity occurs by diffusion. During the solder reflow process, in which the component is attached to the PCB, the whole body of the component is exposed to high process temperatures. The combination of moisture uptake and high reflow soldering temperatures may lead to moisture induced delamination and cracking of the component. To prevent this, this component must be handled in accordance with IPC/JEDEC standard J-STD-020A per the labeled moisture sensitivity level (MSL), level 3.

7.3.2 Reflow Profile

The maximum ramp rates, dwell times, and temperatures of the assembly reflow profile should not exceed those specified in IPC/JEDEC standard J-STD-020A, which were used to determine the moisture sensitivity level of this component.

7.4 Washing

Clare does not recommend ultrasonic cleaning of this part.

For additional information please visit www.clare.com

Specification: DS-CPC5610/CPC5611-R9.0

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