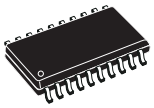
TDA7449

Digital tone control audio processor

Datasheet - production data



SO20

Features

- Input multiplexer
  - Two stereo inputs
  - Selectable input gain for optimal adaptation to different sources
- One stereo output
- Treble and bass control in 2.0 db steps
- Volume control in 1.0 db steps
- Two speaker attenuators:
  - Two independent speaker controls in 1.0 db steps to facilitate balance
  - Independent mute function
- All functions are programmable via serial bus

Description

The TDA7449 is a volume tone (bass and treble) balance (left/right) processor for quality audio applications in TV systems. Selectable input gain is provided. A serial bus controls all functions.

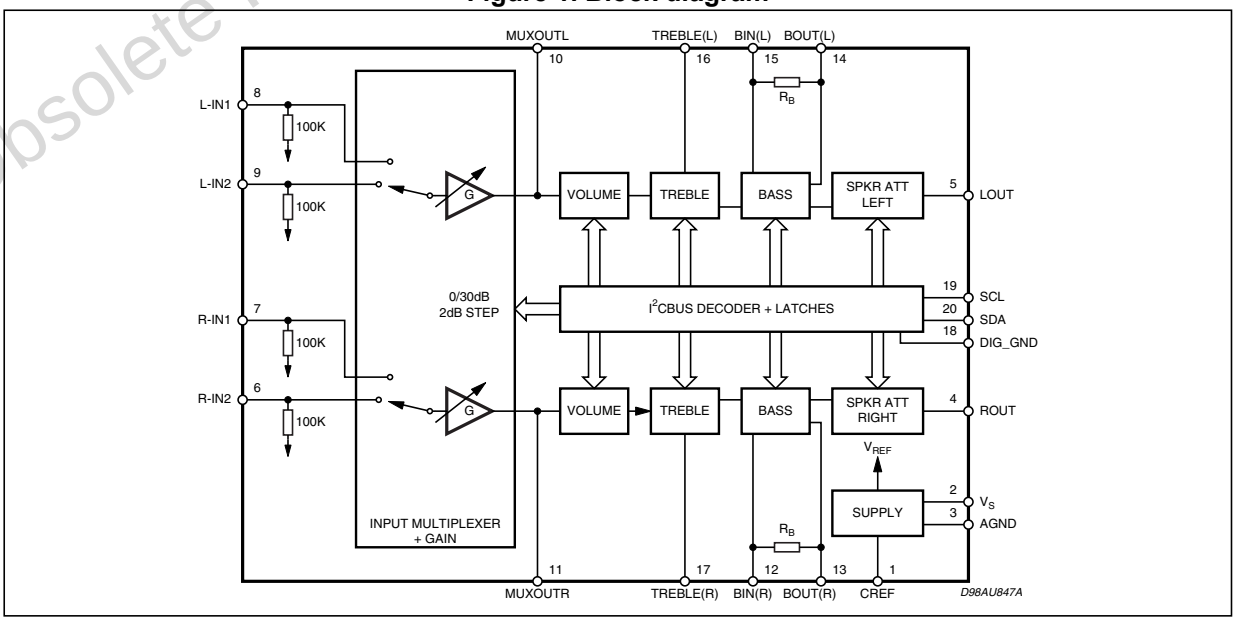
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Bipolar/CMOS technology used allows obtaining low distortion, low noise and DC stepping.

Table 1. Device summary

Order code	Package	Packing
TDA7449D13TR	SO20	Tape and reel

Figure 1. Block diagram



Contents

1 Overview

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature	0 to 70	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Figure 2. Pin connections

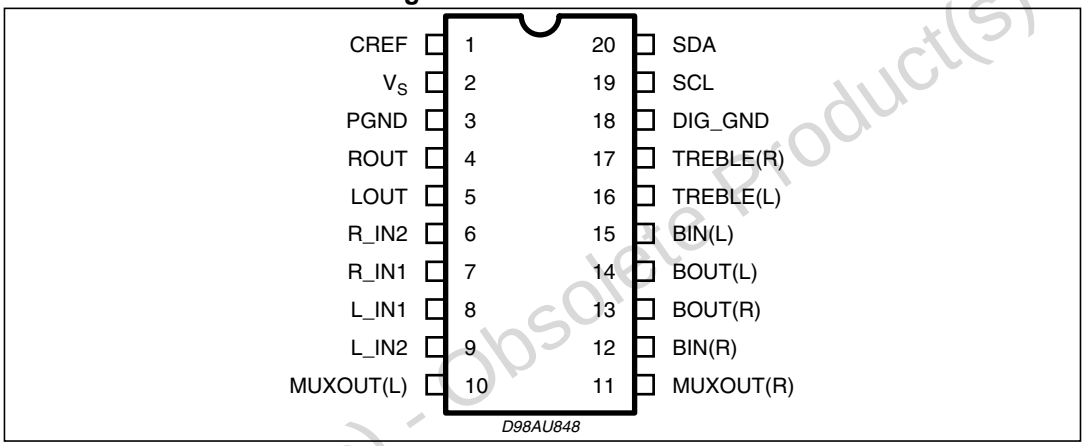


Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	Thermal resistance junction pins	85	°C/W

Table 4. Quick reference data

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply voltage	6	9	10.2	V
V_{CL}	Max input signal handling	2			V_{RMS}
THD	Total harmonic distortion V = 0.1 Vrms f = 1 kHz		0.01	0.1	%
S/N	Signal-to-noise ratio V_{out} = 1 Vrms (mode = OFF)		106		dB
S_C	Channel separation f = 1 KHz		90		dB
	Input gain (2 dB step)	0		30	dB
	Volume control (1 dB step)	-47		0	dB
	Treble control (2 dB step)	-14		14	dB
	Bass control (2 dB step)	-14		14	dB
	Balance control 1 dB step	-79		0	dB
	Mute attenuation		100		dB

2 Electrical characteristics and test circuit

Table 5. Electrical characteristics (refer to the test circuit T_{amb} = 25 °C, V_S = 9 V, R_L= 10 kΩ, R_G = 600 Ω, all controls flat (G = 0 dB), unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply						
V_S	Supply voltage		6	9	10.2	V
I_S	Supply current			7		mA
SVR	Ripple rejection		60	90		dB
Input stage						
R_{IN}	Input resistance			100		kΩ
V_{CL}	Clipping level	THD = 0.3%	2	2.5		Vrms
S_{IN}	Input separation	The selected input is grounded through a 2.2 µ capacitor	80	100		dB
G_{inmin}	Minimum input gain		-1	0	1	dB
G_{inman}	Maximum input gain			30		dB
G_{step}	Step resolution			2		dB
Volume control						
C_{RANGE}	Control range		45	47	49	dB
A_{VMAX}	Max. attenuation		45	47	49	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error	A_V = 0 to -24 dB	-1.0	0	1.0	dB
		A_V = -24 to -47 dB	-1.5	0	1.5	dB
E_T	Tracking error	A_V = 0 to -24 dB		0	1	dB
		A_V = -24 to -47 dB		0	2	dB
V_{DC}	DC step	adjacent attenuation steps		0	3	mV
		from 0 dB to A_V max		0.5		mV
A_{mute}	Mute attenuation		80	100		dB
Bass control (1)						
Gb	Control range	Max. boost/cut	+12.0	+14.0	+16.0	dB
B_{STEP}	Step resolution		1	2	3	dB
R_B	Internal feedback resistance		18.75	25	31.25	KΩ
Treble control (1)						
Gt	Control range	Max. boost/cut	+13.0	+14.0	+15.0	dB
T_{STEP}	Step resolution		1	2	3	dB

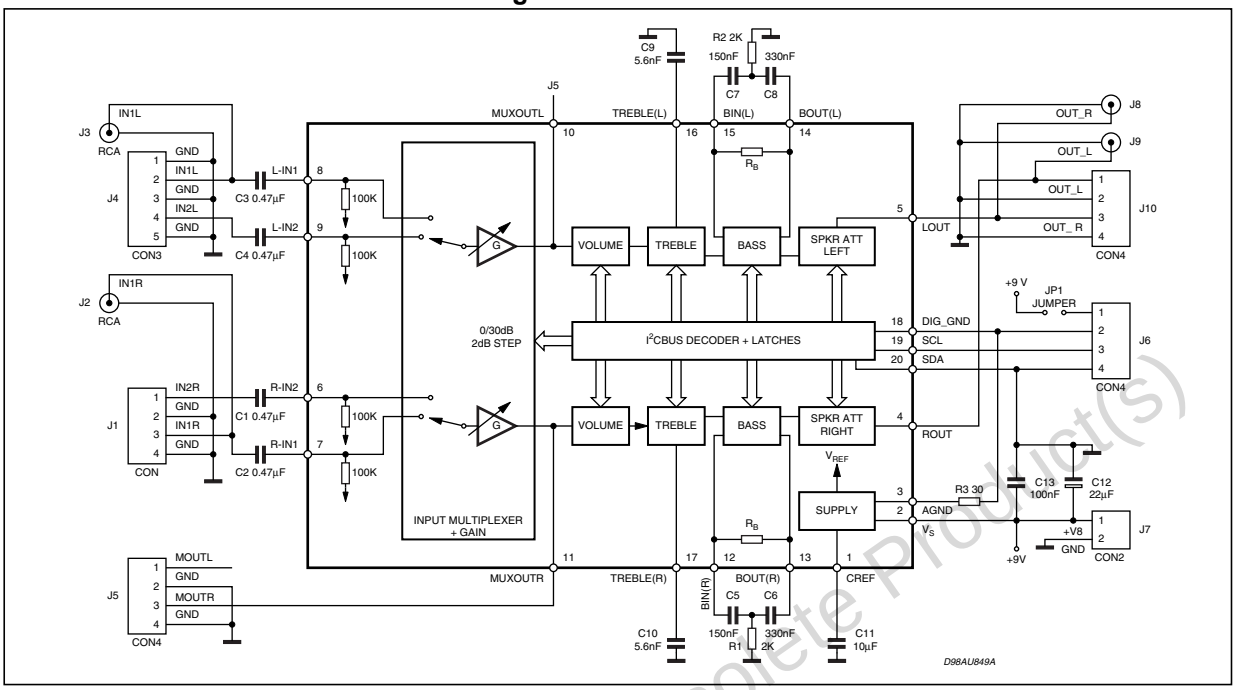
Table 5. Electrical characteristics (refer to the test circuit T_{amb} = 25 °C, V_S = 9 V, R_L= 10 kΩ, R_G = 600 Ω, all controls flat (G = 0 dB), unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Speaker attenuators						
C_{RANGE}	Control range			76		dB
S_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error	A_V = 0 to -20 dB	-1.5	0	1.5	dB
		A_V = -20 to -56 dB	-2	0	2	dB
V_{DC}	DC Step	adjacent attenuation steps		0	3	mV
A_{mute}	Mute attenuation		80	100		dB
Audio outputs						
V_{CLIP}	Clipping level	d = 0.3%	2.1	2.6		V_{RMS}
R_L	Output load resistance		2			kΩ
R_O	Output impedance		10	40	70	W
V_{DC}	DC voltage level			3.8		V
General						
E_{NO}	Output noise	All gains = 0dB; BW = 20Hz to 20KHz flat		5	15	µV
E_t	Total tracking error	A_V = 0 to -24dB		0	1	dB
		A_V = -24 to -47dB		0	2	dB
S/N	Signal-to-Noise ratio	All gains 0dB; V_O = $1V_{RMS}$;		106		dB
S_C	Channel separation left/right		80	100		dB
d	Distortion	A_V = 0; V_I = $1V_{RMS}$;		0.01	0.08	%
Bus input						
V_{IL}	Input low voltage				1	V
V_{IH}	Input high voltage		3			V
I_{IN}	Input current	V_{IN} = 0.4 V	-5		5	µA
V_O	Output voltage SDA acknowledge	I_O = 1.6 mA		0.4	0.8	V

Note: 1. The device is functionally good at Vs = 5 V. A step down on Vs to 4 V doesn't reset the device.

2. Bass and treble response: the center frequency and the response quality can be chosen by the external circuitry.

Figure 3. Test circuit



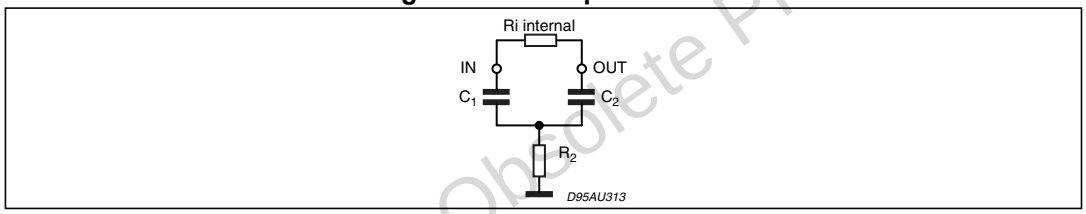
3 Application recommendations

The first and the last stages are volume control blocks. The control range is 0 to -47 dB (mute) for the first one and 0 to -79 dB (mute) for the last one. Both of them have 1 dB step resolution. The very high resolution allows the implementation of systems free from any noisy acoustical effect. The TDA7449 audio processor provides dual-band tone control. Typical responses are shown in *Figure 5* through *9*.

3.1 Bass stage

The bass cell has an internal resistor Ri = 25 kΩ typical. Several filter types can be implemented, connecting external components to the bass IN and OUT pins. *Figure 4* refers to a basic T-type bandpass filter. The filter component values R1 internal F_C, the gain A_V at max. boost and the filter Q factor are calculated as given below.

Figure 4. T bandpass filter



$$F_C = \frac{1}{2 \cdot \pi \cdot \sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}$$

$$A_V = \frac{R2C2 + R2C1 + RiC1}{R2C1 + R2C2}$$

$$Q = \frac{\sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}{R2C1 + R2C2}$$

Once the F_C, A_V, and Ri internal values are fixed, the external component values will be:

$$C1 = \frac{A_V - 1}{2 \cdot \pi \cdot Fc \cdot Ri \cdot Q} \qquad C2 = \frac{Q^2 \cdot C1}{A_V - 1 - Q^2}$$

$$R2 = \frac{A_V - 1 - Q^2}{2 \cdot \pi \cdot C1 \cdot Fc \cdot (A_V - 1) \cdot Q}$$

3.2 Treble stage

The treble stage is a high-pass filter whose time constant is fixed by an internal resistor (25 kΩ typical) and an external capacitor connected between the treble pins and ground.

3.3 CREF

The recommended 10 µF reference capacitor (CREF) value can be reduced to 4.7 µF if the application requires faster power ON.

Figure 5. THD vs. frequency

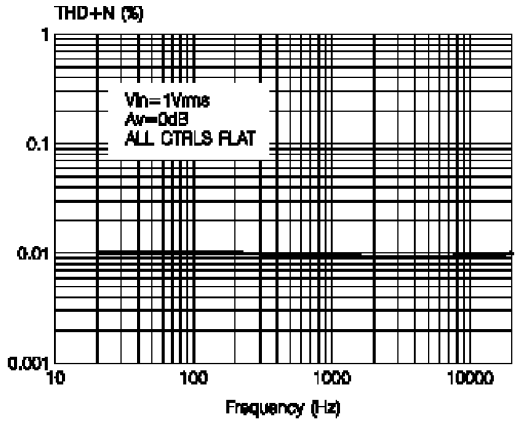


Figure 6. Bass response

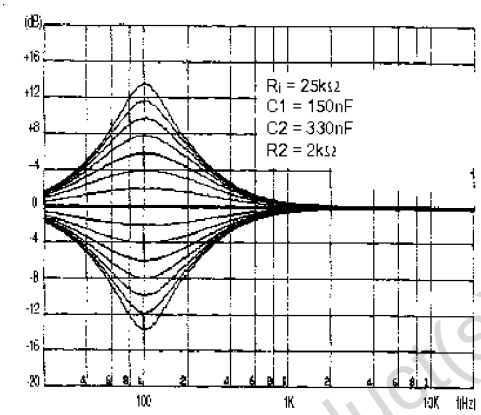


Figure 7. THD vs. R_{LOAD}

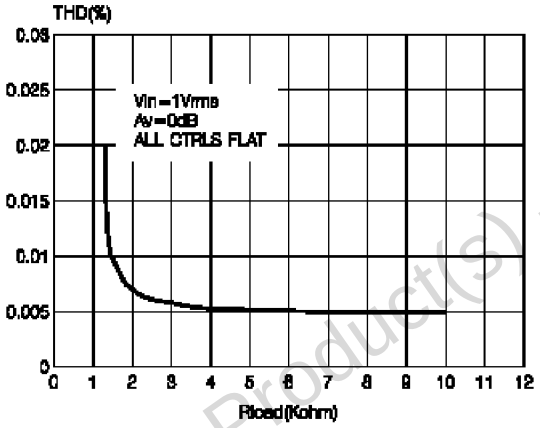


Figure 8. Treble response

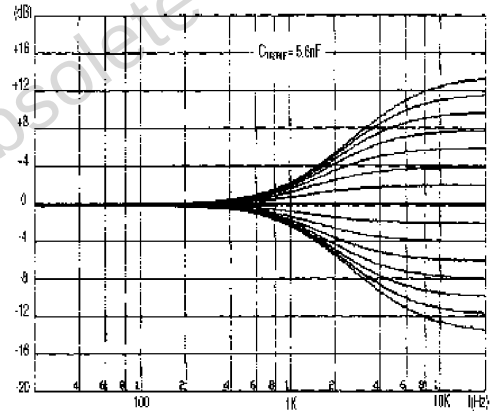
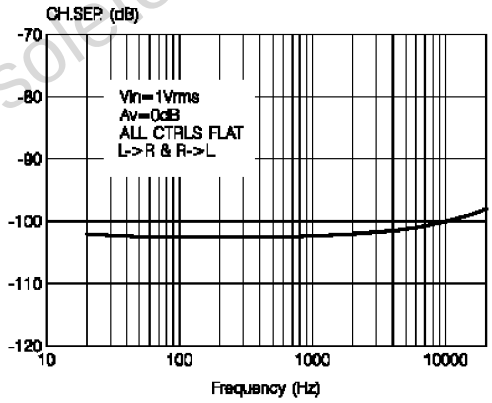


Figure 9. Channel separation vs. frequency



4 I²C bus interface

Data transmission from the microprocessor to the TDA7449 and vice versa takes place through the 2-wire I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to the positive supply voltage must be connected).

4.1 Data validity

As shown in *Figure 10*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

4.2 Start and stop conditions

As shown in *Figure 11*, a start condition is a HIGH-to-LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW-to-HIGH transition of the SDA line while SCL is HIGH.

4.3 Byte format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

4.4 Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 12*). The peripheral (audio processor) that acknowledges has to pull down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

4.5 Transmission without acknowledge

Instead of detecting the acknowledge from the audio processor, the µP can use a simpler transmission which is to simply wait one clock pulse without checking the slave acknowledge and send the new data.

This is of course a riskier approach.

Figure 10. Data validity on the I²C bus

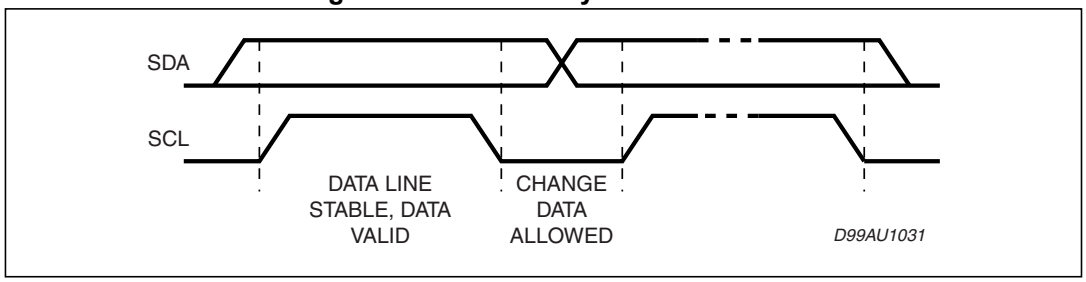


Figure 11. Timing diagram of I²C bus

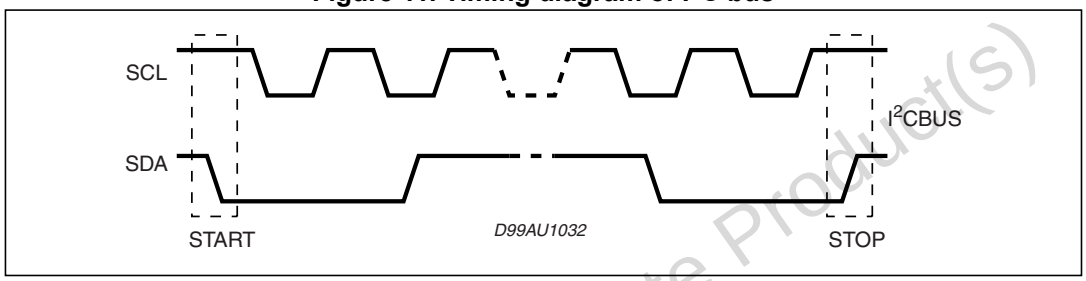
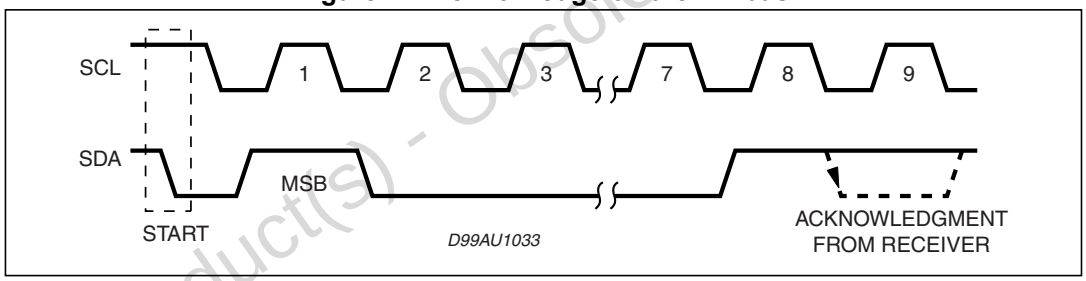


Figure 12. Acknowledge on the I²C bus



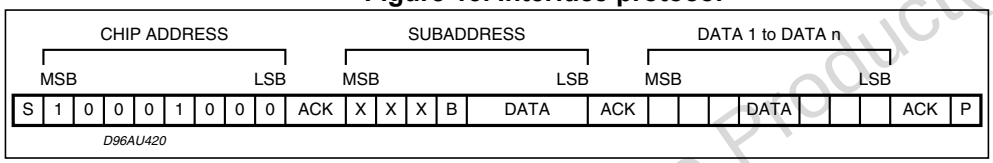
5 Software specifications

5.1 Interface protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7449 address
- A subaddress byte
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

Figure 13. Interface protocol



ACK = Acknowledge

S = Start

P = Stop

A = Address

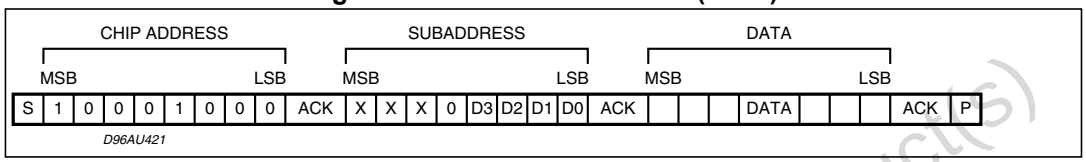
B = Auto-increment

6 Examples

6.1 No incremental bus

The TDA7449 receives a start condition, the correct chip address, a subaddress with B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.

Figure 14. No incremental bus (B = 0)



6.2 Incremental bus

The TDA7449 receives a start condition, the correct chip address, a subaddress with B = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored.

DATA 1 concern the subaddress sent, and DATA 2 concerns the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.

Figure 15. Incremental bus (B=1)

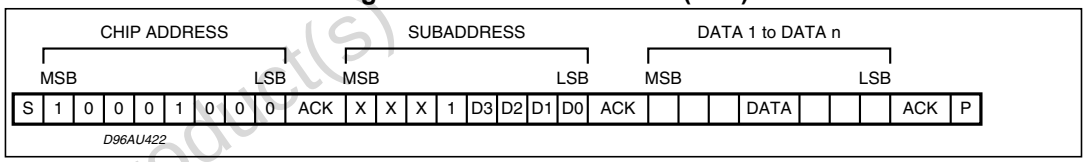


Table 6. Power-on reset condition

Input selection	IN2
Input gain	28 dB
Volume	Mute
Bass	0 dB
Treble	2 dB
Speaker	Mute

7 Data bytes

Address = 88 hex (Addr: OPEN)

Table 7. Function selection: first byte (subaddress)

MSB							LSB	Subaddress
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	Input select
X	X	X	B	0	0	0	1	Input gain
X	X	X	B	0	0	1	0	Volume
X	X	X	B	0	0	1	1	Not allowed
X	X	X	B	0	1	0	0	Bass
X	X	X	B	0	1	0	1	Treble
X	X	X	B	0	1	1	0	Speaker attenuate "R"
X	X	X	B	0	1	1	1	Speaker attenuate "L"

B = 1: incremental bus active

B = 0: no incremental bus

X = don’t care

Table 8. Input selection

MSB							LSB	Input multiplexer
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	0	0	Not allowed
X	X	X	X	X	X	0	1	Not allowed
X	X	X	X	X	X	1	0	IN2
X	X	X	X	X	X	1	1	IN1

Table 9. Input gain selection

MSB							LSB	Input gain 2 dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	0 dB
				0	0	0	1	2 dB
				0	0	1	0	4 dB
				0	0	1	1	6 dB
				0	1	0	0	8 dB
				0	1	0	1	10 dB
				0	1	1	0	12 dB
				0	1	1	1	14 dB
				1	0	0	0	16 dB
				1	0	0	1	18 dB
				1	0	1	0	20 dB
				1	0	1	1	22 dB
				1	1	0	0	24 dB
				1	1	0	1	26 dB
				1	1	1	0	28 dB
				1	1	1	1	30 dB

Gain = 0 to 30 dB

Table 10. Volume selection

MSB							LSB	Volume 1 dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	0 dB
					0	0	1	-1 dB
					0	1	0	-2 dB
					0	1	1	-3 dB
					1	0	0	-4 dB
					1	0	1	-5 dB
					1	1	0	-6 dB
					1	1	1	-7 dB
	0	0	0	0				0 dB
	0	0	0	1				-8 dB
	0	0	1	0				-16 dB
	0	0	1	1				-24 dB
	0	1	0	0				-32 dB
	0	1	0	1				-40 dB
	X	1	1	1	X	X	X	Mute

Volume = 0 to 47dB/mute

Table 11. Bass selection

MSB							LSB	Bass 2 dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	-14 dB
				0	0	0	1	-12 dB
				0	0	1	0	-10 dB
				0	0	1	1	-8 dB
				0	1	0	0	-6 dB
				0	1	0	1	-4 dB
				0	1	1	0	-2 dB
				0	1	1	1	0 dB
				1	1	1	1	0 dB
				1	1	1	0	2 dB
				1	1	0	1	4 dB
				1	1	0	0	6 dB
				1	0	1	1	8 dB
				1	0	1	0	10 dB
				1	0	0	1	12 dB
				1	0	0	0	14 dB

Table 12. Treble selection

MSB							LSB	Treble 2 dB steps
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	-14 dB
				0	0	0	1	-12 dB
				0	0	1	0	-10 dB
				0	0	1	1	-8 dB
				0	1	0	0	-6 dB
				0	1	0	1	-4 dB
				0	1	1	0	-2 dB
				0	1	1	1	0 dB
				1	1	1	1	0 dB
				1	1	1	0	2 dB
				1	1	0	1	4 dB
				1	1	0	0	6 dB
				1	0	1	1	8 dB
				1	0	1	0	10 dB
				1	0	0	1	12 dB
				1	0	0	0	14 dB

Table 13. Speaker attenuation selection

MSB							LSB	Speaker attenuation 1 dB
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	0 dB
					0	0	1	-1 dB
					0	1	0	-2 dB
					0	1	1	-3 dB
					1	0	0	-4 dB
					1	0	1	-5 dB
					1	1	0	-6 dB
					1	1	1	-7 dB
	0	0	0	0				0 dB
	0	0	0	1				-8 dB
	0	0	1	0				-16 dB
	0	0	1	1				-24 dB
	0	1	0	0				-32 dB
	0	1	0	1				-40 dB
	0	1	1	0				-48 dB
	0	1	1	1				-56 dB
	1	0	0	0				-64 dB
	1	0	0	1				-72 dB
	1	1	1	1	X	X	X	Mute

Speaker attenuation = 0 to -79dB/mute

Figure 16. Pin 1

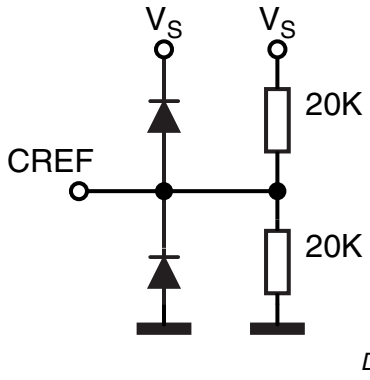


Figure 17. Pins 10, 11

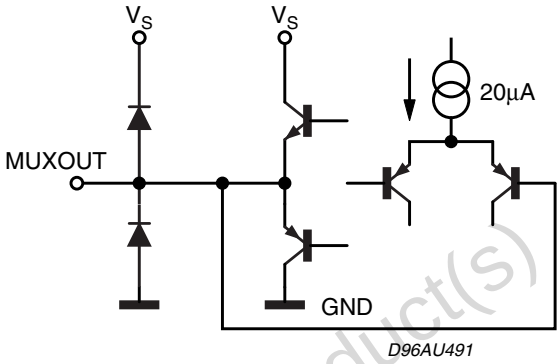


Figure 18. Pins 4, 5

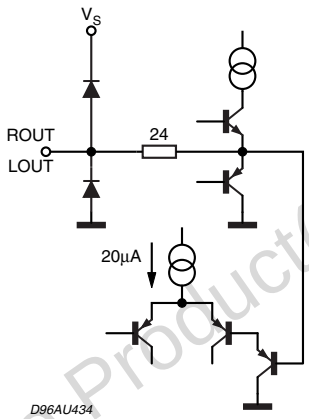


Figure 19. Pins 12, 15

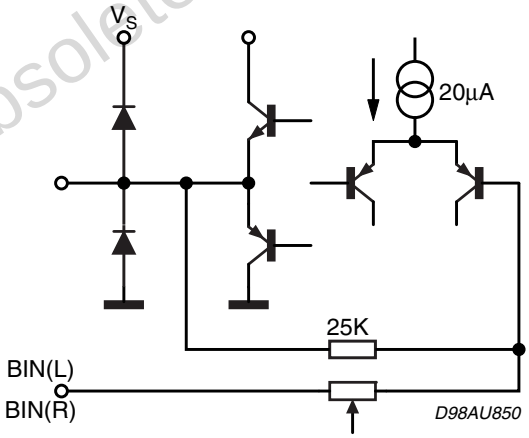


Figure 20. Pins 6, 7, 8, 9

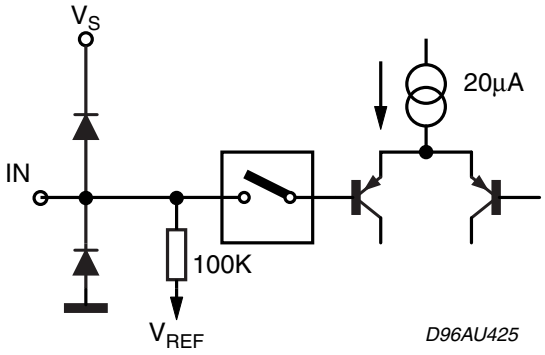


Figure 21. Pins 13, 14

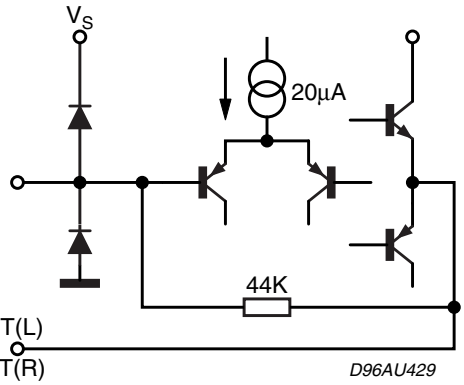


Figure 22. Pins 16, 17

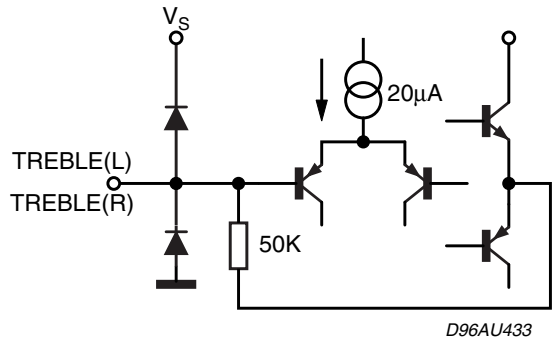


Figure 23. Pin 20

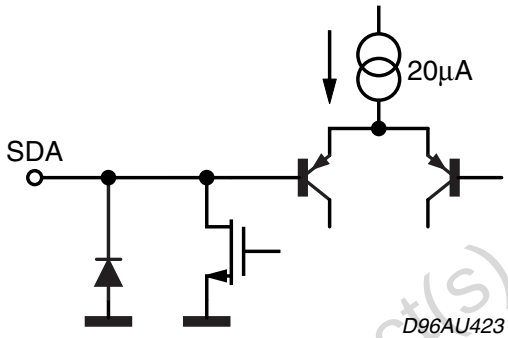
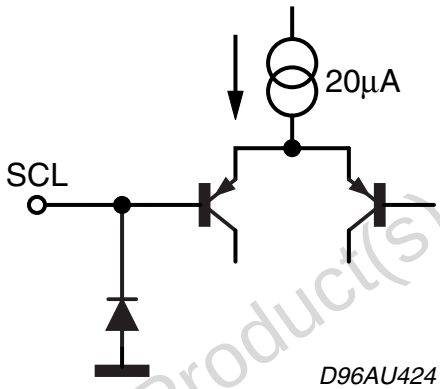


Figure 24. Pin 19



8 Package information

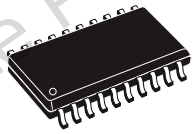
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 25. SO20 mechanical data & package dimensions

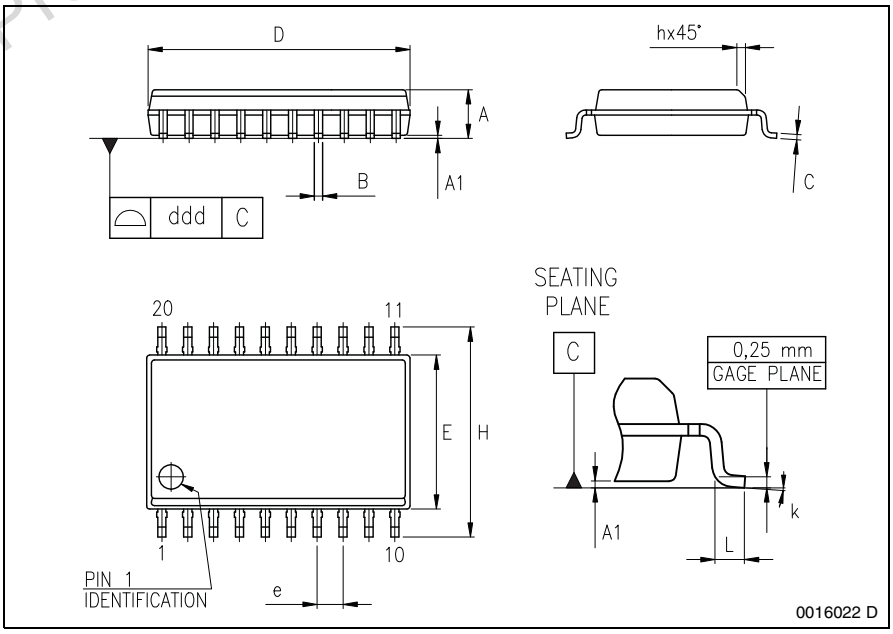
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



9 Revision history

Table 14. Document revision history

Date	Revision	Changes
03-Sep-2014	5	Removed DIP20 package option Updated *Table 1: Device summary* Revised document presentation along with minor textual updates and modification of title

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