50 V Ultra Low Noise FOC Motor Controller

FEATURES AND BENEFITS

- Code-free sensorless field-oriented control (FOC)
- I²C interface for speed control and status readback
- Ultra-quiet low speed operation
- Proprietary non-reverse fast startup
- Soft-On Soft-Off (SOSO) for quiet operation
- Analog / PWM / Clock mode speed control
- Closed-loop speed control
- Configurable current limit
- Windmill startup operation
- Lock detection
- Short-circuit protection (OCP)
- Brake and direction inputs
- Adjustable gate drive

APPLICATIONS

- Ceiling fans
- Pedestal fans
- Bathroom exhaust fans
- Home appliance fans and pumps

DESCRIPTION

The A89301 is a 3-phase, sensorless, brushless DC (BLDC) motor driver (gate driver) which can operate from 5.5 to 50 V.

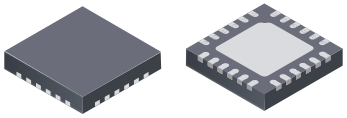
A field-oriented control (FOC) algorithm is fully integrated to achieve the best efficiency and acoustic noise performance. The device optimizes the motor startup performance in a stationary condition, a windmill condition, and even in a reverse windmill condition.

Motor speed is controlled through analog, PWM, or CLOCK input. Closed-loop speed control is optional, and RPM-to-clock frequency ratio is programmable.

A simple I²C interface is provided for setting motor-rated voltage, rated current, rated speed, resistance, and startup profiles. The I²C interface is also used for on/off control, speed control, and speed readback.

The A89301 is available in a 24-contact 4 mm × 4 mm QFN with exposed thermal pad (suffix ES). The package is lead (Pb) free, with 100% matte-tin leadframe plating.

PACKAGE



Not to scale

24-contact QFN
with exposed thermal pad
4 mm × 4 mm × 0.75 mm
(ES package)

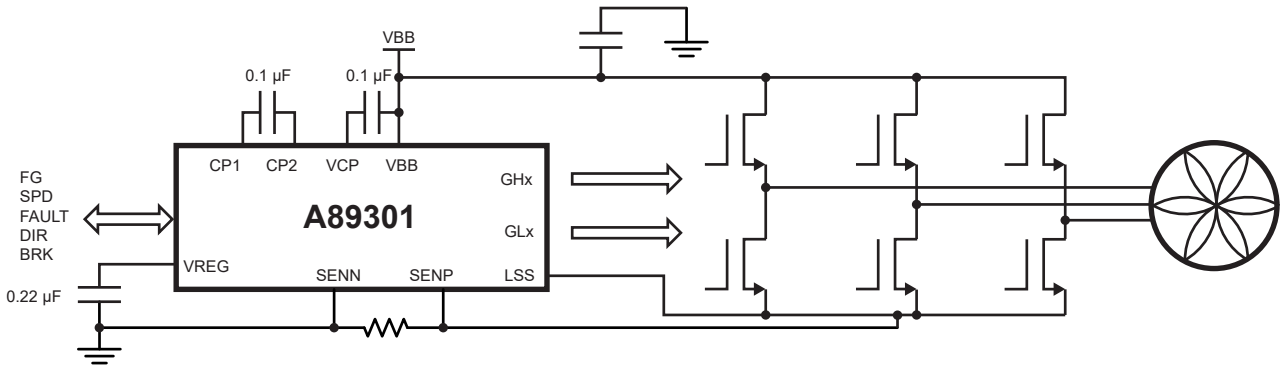


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Ambient Temperature Range (T_A) (°C)	Packaging	Packing
A89301GESSR	–40 to 105	24-contact QFN with exposed thermal pad	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		50	V
Logic Input Voltage Range	V_{IN}	SPD, BRAKE, DIR	–0.3 to 6	V
Logic Output	V_O	FG, FAULT (I < 5 mA)	6	V
LSS	V_{LSS}	DC	±500	mV
		t_W < 500 ns	±4	V
VREG	V_{REG}		0 to 4	V
SENN, SENP	V_{SENN}, V_{SENP}	DC	±500	mV
		t_W < 500 ns	±4	V
Output Voltage	V_{OUT}	SA, SB, SC	–2 to V_{BB}+2	V
		SA, SB, SC, t_w < 50 ns	–4 to V_{BB}+4	V
GHx	V_{GHx}		V_{Sx}–0.3 to V_{CP}+0.3	V
GLx	V_{GLx}		V_{LSS}–0.3 to 8.5	V
VCP	V_{CP}		V_{BB}–0.3 to V_{BB}+8	V
CP1	V_{CP1}		–0.3 to V_{BB}+0.3	V
CP2	V_{CP2}		V_{BB}–0.3 to V_{CP}+0.3	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	24-contact QFN (package ES), on 2-sided PCB 1-in.^{2} copper	45	°C/W

*Additional thermal information available on the Allegro website.

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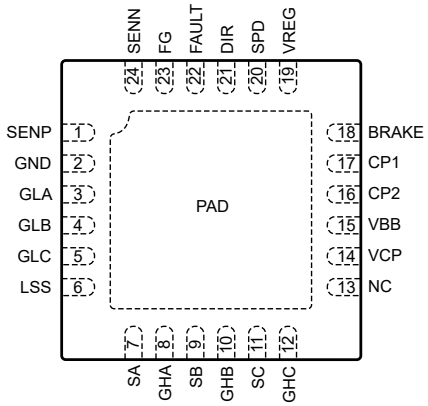
PINOUT DIAGRAM AND TERMINAL LIST



ES Package Pinouts

Terminal List Table

Terminal Number	Name	Function
16	CP2	Charge pump
17	CP1	Charge pump
18	BRAKE	Logic input
19	VREG	2.8 V regulator voltage
20	SPD	PWM or clock mode speed control
21	DIR	Direction control
22	FAULT	Fault indicator output
23	FG	Motor speed output
24	SENN	Current sense negative terminal
1	SENP	Current sense positive terminal
2	GND	Ground
3	GLA	Low-side gate drive output
4	GLB	Low-side gate drive output
5	GLC	Low-side gate drive output
6	LSS	Low-side source
7	SA	Motor output
8	GHA	High-side gate drive output
9	SB	Motor output
10	GHB	High-side gate drive output
11	SC	Motor output
12	GHC	High-side gate drive output
13	NC	No connect
14	VCP	Charge pump
15	VBB	Power supply
PAD	PAD	Exposed pad for enhanced thermal dissipation

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FUNCTIONAL BLOCK DIAGRAM

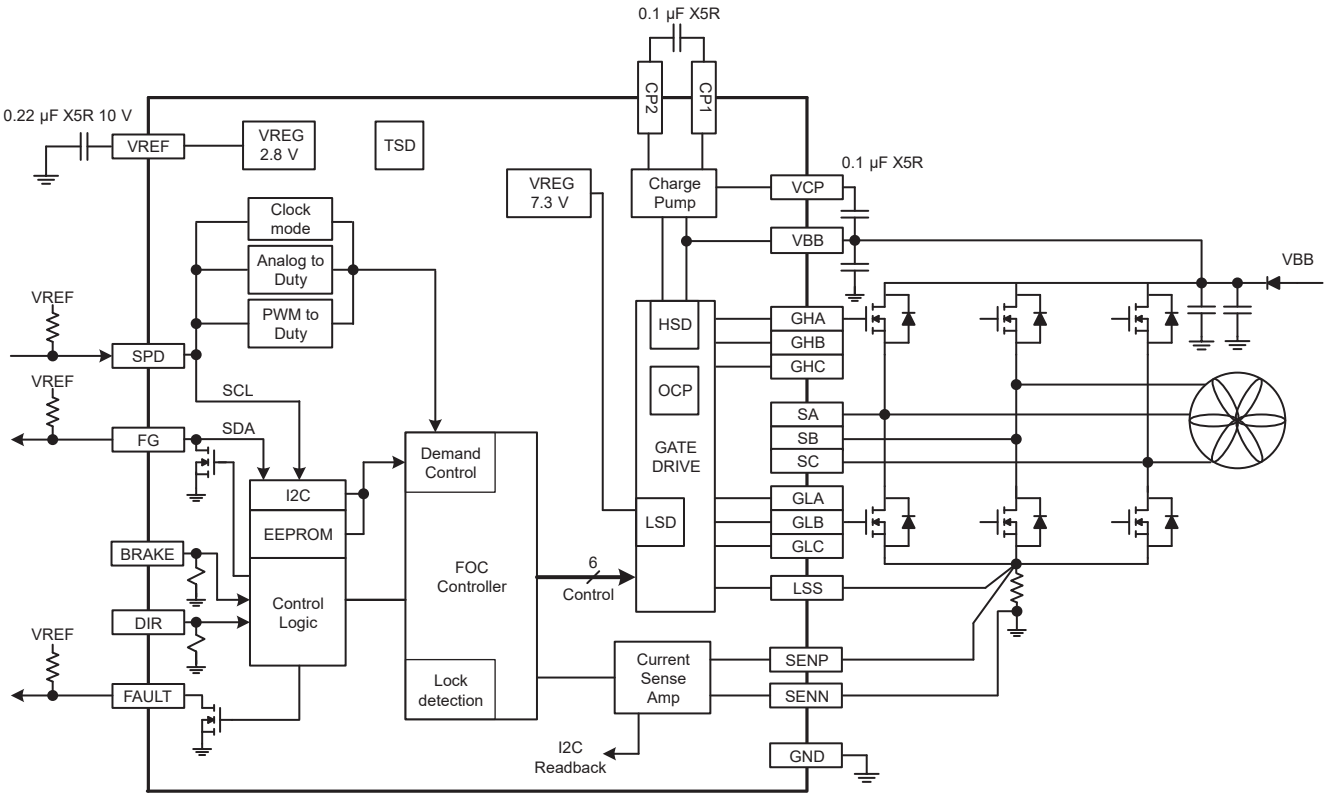

Figure 2: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS [1]: Valid over operating ambient temperature range and operating voltage range, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Supply Voltage Range	V_{BB}	Driving	5.5	–	48	V
		Operating	5.5	–	50	V
VBB Supply Current	I_{BB}	I_{VREG} = 0 mA	–	8	12	mA
		Standby mode	–	10	20	µA
Reference Voltage	V_{REG}	I_{OUT} = 10 mA	2.7	2.86	2.95	V
GATE DRIVE						
High Side Gate Drive Output	V_{GH}	V_{BB} = 8 V	6.5	6.8	–	V
		V_{BB} = 24 V	6.5	6.8	–	V
Low Side Gate Drive Output	V_{GL}	V_{BB} = 8 V	6.5	7.3	–	V
		V_{BB} = 24 V	6.5	7.3	–	V
Gate Drive Source Current	I_{SO}	V_{BB} = 8 V; level 0	–	15	–	mA
		V_{BB} = 8 V; level 1	–	30	–	mA
		V_{BB} = 8 V; level 2	–	55	–	mA
Gate Drive Sink Current	I_{SI}	V_{BB} = 8 V; level 0	–	30	–	mA
		V_{BB} = 8 V; level 1	–	60	–	mA
		V_{BB} = 8 V; level 2	–	105	–	mA
VDS SENSING FOR OCP						
VDS Comparator Threshold	V_{DS_THR}	level 0	–	1	–	V
		level 1	–	2	–	V
MOTOR DRIVE						
PWM Duty On Threshold	PWM_{ON}	Relative to target	–0.5	–	0.5	%
PWM Duty Off Threshold	PWM_{OFF}	Relative to target	–0.5	–	0.5	%
PWM Input Frequency Range	$f_{PWM(MIN)}$	PWM input frequency setting = 0	2.5	–	100	kHz
		PWM input frequency setting = 1	80	–	3200	Hz
Clock Input Frequency Range	f_{CLOCK}	CLOCK mode	1	–	2000	Hz
SPD Standby Threshold (Analog Enter)	$V_{SPD(TH\_ENT)}$		50	100	150	mV
SPD Standby Threshold (Analog Exit)	$V_{SPD(TH\_EXIT)}$		0.4	0.75	1	V
SPD On Threshold	$V_{SPD(ON)}$	ON/OFF setting = 10%	210	250	290	mV
SPD Max	$V_{SPD(MAX)}$		–	2.5	–	V
SPD ADC Resolution	$V_{SPDADC(RES)}$		–	9.78	–	mV
SPD ADC Accuracy	$V_{SPDADC(ACC)}$	V_{SPD} = 0.2 to 2.5 V	–40	–	40	mV
Speed Closed Loop Accuracy	$f_{SPD(ACC)}$	PWM mode or Analog mode	–5	–	5	%
		Clock mode	–0.1	–	0.1	rpm
Dead Time	t_{DT}	Code = 9	–	400	–	ns
Motor PWM Frequency	f_{PWM}	T_A = 25°C	23.3	24.4	25.3	kHz

Continued on next page...

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid over operating ambient temperature range and operating voltage range, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
VBB UVLO	$V_{BB(UVLO)}$	V_{BB} rising	–	4.75	4.95	V
VBB UVLO Hysteresis	$V_{BB(HYS)}$		200	300	450	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C
LOGIC, IO, I²C						
Input Current	I_{IN}	SPD, FG; V_{IN} = 0 to 5.5 V	–5	1	5	µA
		BRK, DIR; V_{IN} = 5 V	–	50	–	µA
Logic Input, Low Level	V_{IL}		0	–	0.8	V
Logic Input, High Level	V_{IH}		2	–	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
FG Output Leakage	I_{FG}	V = 5.5 V	–	–	1	µA

[1] Specified limits are tested at 25°C and 125°C and statistically assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A89301 is a three-phase BLDC controller with integrated gate driver. It operates from 5.5 to 50 V and targets pedestal fan, ceiling fan, and ventilation fan applications.

The integrated field-oriented control (FOC) algorithm achieves the best efficiency and dynamic response and minimizes acoustic noise. Allegro's proprietary non-reverse startup algorithm improves startup performance. The motor will start up towards the target direction after power-up without reverse shaking or vibration. The Soft-On Soft-Off (SOSO) feature gradually increases the current to the motor at "on" command (windmill condition), and gradually reduces the current from the motor at the "off" command, further reducing the acoustic noise and operating the motor smoothly.

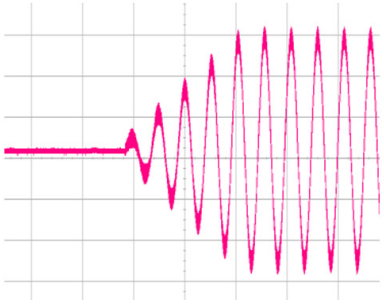

Figure 3: Current Waveform of Soft-On

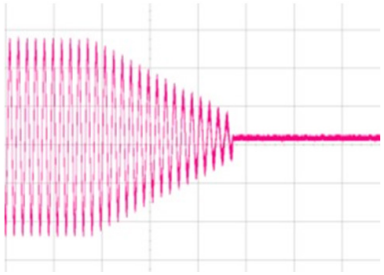

Figure 4: Current Waveform of Soft-Off

Speed Control

Speed demand is provided via the SPD pin. Three speed control modes are selectable through the EEPROM. The A89301 also features a closed-loop speed function, which can be enabled or disabled via the EEPROM.

PWM Mode: The motor speed is controlled by the PWM duty cycle on the SPD pin, and higher duty cycle represents higher speed demand. If closed-loop speed is disabled, the output voltage amplitude will be proportional to the PWM duty cycle. If closed-loop speed is enabled, the motor speed is proportional to the PWM duty cycle, and 100% duty represents the rated speed of the motor, which can be programmed in the EEPROM.

$$close\_loop\_speed = rated\_speed \times duty\_input$$

The SPD PWM frequency range is 80 Hz to 100 kHz. If it is higher than 2.8 kHz, set PWMfreq = 0; if it is lower than 2.8 kHz, set PWMfreq = 1.

Analog Mode: The motor speed is controlled by the analog voltage on the SPD pin, with higher voltage representing higher speed demand. If closed-loop speed is disabled, the output voltage amplitude will be proportional to the analog voltage input. If closed-loop speed is enabled, the motor speed is as follows:

$$closed\_loop\_speed = rated\_speed \times analog\_input / SPD_{MAX}$$

CLOCK Mode: In the clock speed control mode, the closed-loop speed is always enabled. Higher frequency on the SPD pin will drive a higher motor speed as follows:

$$close\_loop\_speed\ (rpm) = clock\_input \times speed\_ctrl\_ratio,$$

where the speed_ctrl_ratio can be programmed in the EEPROM.

For example, if the ratio is 4 and the clock input frequency is 60 Hz, then the motor will operate at 240 rpm. Note the number of motor pole pairs must be set properly in the programming application for the rated speed (rpm) setting to be accurate.

If the clock frequency commands a speed that is higher than twice the rated speed, the A89301 treats it as a clock input error and stops the motor.

CLOCK mode can achieve the best speed closed-loop accuracy.

For all three speed control modes with closed-loop speed enabled, if the demand speed is higher than the maximum speed, the system can run at a certain supply voltage and load condition, and the A89301 will just provide the maximum output voltage (if current limit is not triggered) or the maximum output current (if current limit is triggered).

The SPD pin is also used as SCL in the I^2C mode.

Speed control can also be achieved through I^2C command. Refer to

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register table for more details. While in Analog mode, PWM mode, or CLOCK mode, sending I²C command may cause motor speed change, unexpected startup attempts, or operation failure. Changing from I²C mode to CLOCK (Analog, PWM) mode requires either power cycle, or enter and then exit from standby mode.

Motor Stop and Standby Mode

If the speed demand is less than the programmed threshold, the motor will stop.

On/Off Setting	On Threshold	Off Threshold
6%	7.8%	5.9%
10%	11.7%	9.8%
15%	14.9%	12.9%
20%	21.5%	19.6%

For example, consider 10% is set as the threshold. If PWM duty is less than 9.8% (in PWM mode), or the analog voltage is less than 250 mV (in Analog mode), or the CLOCK input frequency is less than 9.8% of the "rated_speed" (in CLOCK mode), the IC will stop the motor and enter the "idle" mode.

In order to enter standby, two conditions must be met: 1) the motor must be stationary (this condition can be ignored by setting the EEPROM), and 2) PWM or CLOCK signal must remains logic low (in PWM and CLOCK mode) or the analog voltage remains less than $V_{SPD(TH\_ENT)}$ (in Analog mode) for longer than one second.

A rising edge on PWM or CLOCK will wake the IC in PWM and CLOCK mode, and in Analog mode, the SPD voltage must be higher than $V_{SPD(TH\_EXIT)}$ to wake up the IC.

Standby Mode will turn off all circuitry including the charge pump and VREG.

After powering on, the device will always be in the active mode before entering standby mode.

The standby mode can be disabled in the EEPROM.

Direction Input: Logic input to control motor direction. For logic high, the motor phases are ordered A→B→C. For logic low, the motor phases are ordered A→C→B. The A89301 supports changing the direction input while the motor is running. The direction can also be controlled through register.

BRAKE: Active-high signal turns on all low sides for braking function. The Brake function overrides speed control input. Care should be taken to avoid stress on the MOSFET when braking while the motor is running. With braking, the current will be limited only by V_{BEMF}/R_{MOTOR}. The A89301 includes an optional feature which holds off braking until the motor speed drops to a low enough (configurable) level so that the braking current will not damage the MOSFET.

FAULT: Open-drain output provides motor operation fault status. Default is high when there is no fault.

Recommended maximum sink current is 10 mA.

An LED and a serial resistor is recommended between the FAULT and VREG pins. The LED indicates fault information.

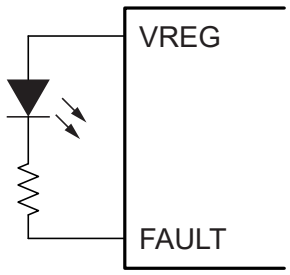

Figure 5: A89301 with LED and Serial Resistor

Fault Type	FAULT Pin	LED Pattern
Lock detected	low	constant on
OCP	0.67 seconds high 0.67 seconds low	slow flashing
Thermal Shutdown	0.67 seconds low 0.17 seconds high 0.08 seconds low 0.17 seconds high 0.08 seconds low 0.17 seconds high	long-short-short flashing
System Error	0.08 seconds low 0.08 seconds high 0.08 seconds low 1.09 seconds high	double short flashing
OVP	0.17 seconds high 0.17 seconds low	fast flashing
Input demand below threshold	0.25 seconds high 0.08 seconds low 0.34 seconds high 0.67 seconds low	long-short flashing

FG: Open-drain output provides motor speed information to the system. The open-drain output can be pulled up to VREG or an external 3.3 or 5 V supply.

The FG pin is also used as SDA in I²C mode. The first I²C command can pass only when the FG is high (open drain off). After the first I²C command, the FG pin is no longer used for speed

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information, and the FG pin is dedicated as a data pin for the I²C interface.

FG is default high after power-on and exit from standby mode, and stays high for at least 9.8 ms. To ensure successful I²C communication, it is recommended to have the first I²C demand within 9.8 ms after power up or exit from standby mode.

FG function can be disabled in the EEPROM; then the FG pin will be dedicated as SDA.

If observing FG signal is required in I²C mode, the FG signal can be reasigned to the FAULT pin by sending I²C command 0x00A0 to address 165 (Decimal).

System Error: A system error occurs when V_{BB}, the charge pump voltage, or the internal regulator which supplies the low-side gate drivers falls below the respective undervoltage threshold. The motor outputs are disabled upon a system error and will remain off until the voltage that caused the error rises above the respective UVLO threshold plus hysteresis.

OVP: An OVP event occurs when V_{BB} exceeds 47 V typical. OVP is only an indication and the outputs are not disabled. The indication is removed when V_{BB} falls below the threshold.

VREG: Voltage reference (2.8 V) to power internal digital logic and analog circuitry. VREG can be used to power external circuitry with up to 10 mA bias current, if desired. A ceramic capacitor with 0.22 µF or greater is required on the pin to stabilize the supply.

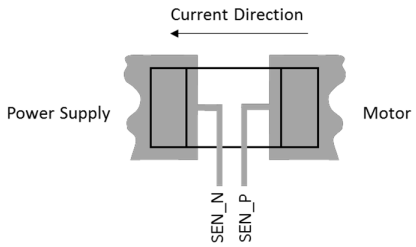
When VREG is loaded externally, the power consumption of the internal LDO is calculated by the equation:

$$P_{LDO} = (I_{LOAD} + I_{INTERNAL}) \times (V_{BB} - V_{REG}).$$

Ensure that the system has good power dissipation and the temperature is within the operating temperature range. The A89301 thermal shutdown function does not protect the LDO.

Bus Current Sensing: A single shunt-resistor connection between SENN and SENP is used to measure the bus current for the FOC algorithm and current limit. The resistor value is approximately tens of a milliohm, depends on the rated current of the system. The integrated shunt-resistor amplifier has a gain of 14.5 and the output range is 0 to 1 V. The voltage difference between SENN and SENP should be less than 65 mV to prevent the signal saturation. For example, if the rated current is 4 A, it is recommend to use a 15 mΩ sensing resistor, so that 4 A × 15 mΩ is between 55 and 65 mV.

Use Kelvin sensing connection for the shunt resistor.



Lock Detect: A logic circuit monitors the motor position to determine if motor is running as expected. If a fault is detected, the motor drive will be disabled for the configurable t_{LOCK} time before an auto-restart is attempted. For additional information, refer to the application note.

Current Control: The motor's rated current at rated speed and normal load must be programmed to the EEPROM for proper operation. The A89301 will limit the motor current (phase current peak value) to 1.3 times the programmed rated current during acceleration or increasing load, which protects the IC and the motor. The current profile during startup can also be programmed.

Overcurrent Protection (short protection): The V_{DS} voltages across each power MOSFET are monitored by the A89301. If a V_{DS} is higher than the threshold when that MOSFET enabled, an OCP fault is triggered and the IC will stop driving immediately.

The VDS comparator threshold can be configured in the EEPROM.

Dead-Time Configuration: In order to avoid shoot-through current in the H-bridge, dead-time is implemented that delays the high-side from turning on after the low-side turns off, and delays the low-side from turning on after the high-side turns off. The dead-time is configurable in the EEPROM with 16 options from 40 to 640 ns.

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Direct Phase Angle Control: The A89301 implements phase angle control based on the user-programmed inductance, together with motor phase current and motor speed. The user may want to bypass this calculated phase advance angle and use direct control from the register.

This function is supported in A89301 by enabling the “direct drive angle” bit in the register. Once enabled, the “motor inductance” register will directly set the phase advance angle, with units of degrees.

Gate Drive Slew Control: A89301 gate driver outputs are current source/sink drivers. The gate drive sink current I_{SI} and source current I_{SO} can be configured in EEPROM to adjust the MOSFET slew rate.

Refer to the application note for details.

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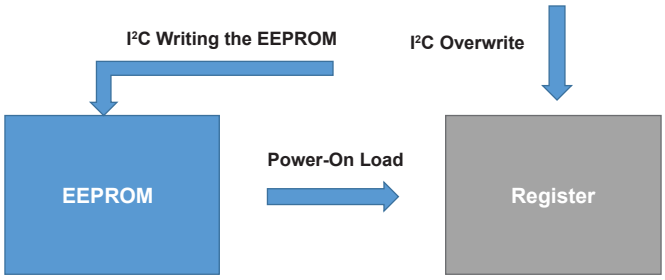
I²C OPERATION AND EEPROM MAP

The I²C interface allows the user to program the register and parameters into EEPROM. The A89301 7-bit slave address is 0x55.

After power-on, the default values in EEPROM will be loaded into the registers, which determines motor system operation. I²C can overwrite those values and change the motor system operation on the fly.

I²C can also be used to program the EEPROM, which is normally done in the production line.



The figures below shows the I²C interface timing.

Read command: Two Step Process

- Start Condition
- 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
- Internal Register Address to be read
- Stop Condition
- Start Condition
- 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 1
- Read 2 data bytes
- Stop Condition

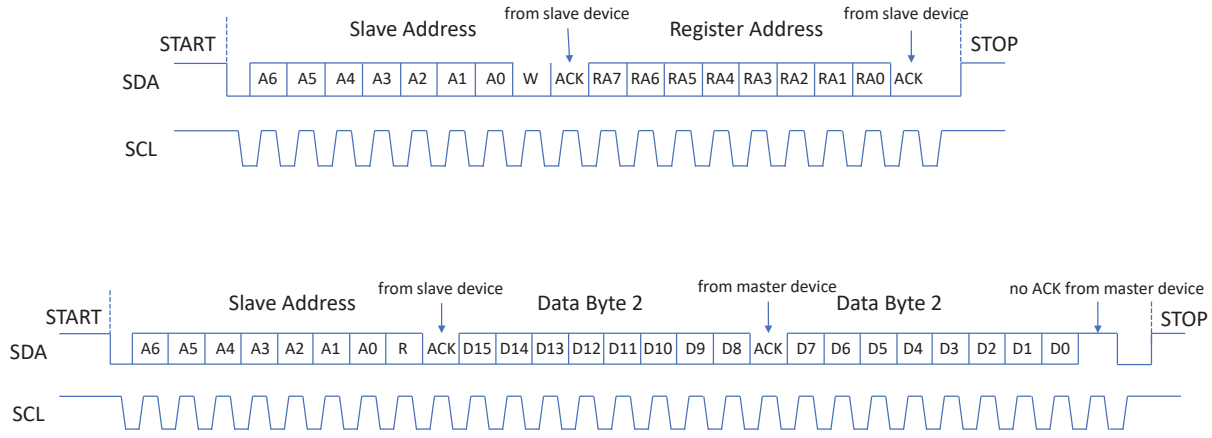


Figure 6: Read Command

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Write command:

Start Condition

- Start Condition
- 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
- Internal Register Address
- 2 data bytes, MSB first
- Stop Condition

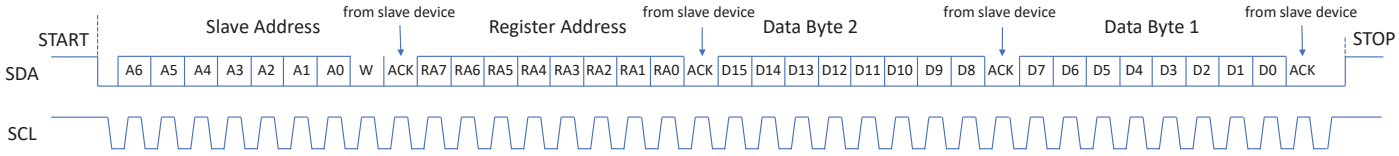

Figure 7: Write Command

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Register and EEPROM Map

Each register bit is associated with one EEPROM bit. The register address is the associated EEPROM bit address plus 64. For example, the rated speed is in EEPROM address 8, bit[10:0]; the associated register address is 72, bit[10:0].

In the following table, the bits shaded in gray should be kept at their default values. Changing these values may cause malfunction or damage to the part. If programming the EEPROM with a custom programmer, it is recommended to use the A89301 application to determine the appropriate settings, save the settings file, and use the file contents to program to the EEPROM. The application's settings file contains one line for each EEPROM address, containing addresses 8 through 22 (15 lines/addresses).

Registers not shown in the table are not for users to access. Changing the value in undocumented registers may cause malfunction or damage to the part.

Table 1: Register and EEPROM Map

Address		A89301 Register Map MSB → LSB			
0		Allegro internal information. No associated register for these EEPROM data			
1					
2					
3					
4					
5					
6		User-flexible code. No associated register for these EEPROM data. Provided to user. For example, tracking number of product, product revision info, etc.			
7					
8 / 72	3:0	Rated_speed [3:0]			
	7:4	Rated_speed [7:4]			
	11:8	speed_close_loop	Rated speed [10:8]		
	15:12	PWMin_range	Direction	Accelerate_range	Clock_PWM
9 / 73	3:0	Acceleration [3:0]			
	7:4	Acceleration [7:4]			
	11:8	Motor_Resistance [3:0]			
	15:12	Motor_Resistance [7:4]			
10 / 74	3:0	Rated Current [3:0]			
	7:4	Rated Current [7:4]			
	11:8	SPD mode	Rated Current [10:8]		
	15:12	Startup_Current [2:0]			
11 / 75	3:0	Open_Drive			
	7:4	Power_Ctl_En	Max_start_curr	Direct_dr_Angle	
	11:8	Startup_mode [1:0]			
	15:12		Extend_lock_mask		Wait_stationary
12 / 76	3:0	PID_P [3:0]			
	7:4	PID_P [7:4]			
	11:8	Motor_Inductance [3:0]			
	15:12	Open_Window		over_Speed_Lock	Motor_Inductance [4]

Continued on next page...

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Table 1: Register and EEPROM Map (continued)

Address		A89301 Register Map			
13 / 77	3:0	PID_I [3:0]			
	7:4	PID_I [7:4]			
	11:8				
	15:12		delay_start		
14 / 78	3:0				
	7:4				FG_pin_dis
	11:8				
	15:12				
15 / 79	3:0	Angle_Error_Lock (startup)			
	7:4	soft_on	soft_off		
	11:8	Deadtime_setting [3:0]			
	15:12	Safe_Brake_thrd [1:0]			
16 / 80	3:0	OCP_reset_mode	OCP_Enable		
	7:4	First_cycle_speed [1:0]		OCP_Masking	
	11:8	Decelerate_buffer [1:0]		Accelerate_buffer [1:0]	
	15:12			BEMF_Lock_filter [1:0]	
17 / 81	8:0	Speed_demand [8:0]			
	9	i2c_speed_mode			
	15:10				
18 / 82	3:0				
	7:4				
	11:8	IPD_Current_Thr [3:0]			
	15:12	drive_gate_slew[1:0]		IPD_Current_Thr [5:4]	
19 / 83	7:0				
	15:8	mosfet_ciss_comp[7:0]			
20 / 84	7:0	Rated_Voltage			
	15:8	Sense_Resistor			
21 / 85	3:0				
	7:4	slight_mv_demand [2:0]			
	11:8			speed_input_off_threshold [1:0]	
	15:12	standby_dis			
22 / 86	3:0	speed_response_tc_and_clock_speed_ratio			
	7:4	Restart_attempt		speed_response_tc_and_clock_speed_ratio	
	11:8	Lock_restart_set	vibration_lock	Soft_off_time	Brake_mode
	15:12	vds_threshold_sel			deadtime_comp

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Table 2: Register and EEPROM Map Notes

Parameter	Address	Notes
Rated_Voltage	20 [7:0]	Rated Voltage (V) = Rated_voltage_register_value / 5
Rated_Speed	8 [10:0]	Rated Speed (Hz) = Rated_speed_register_value × 0.530
Motor_Resistance	9 [15:8]	Motor Resistance (Ω) = Motor_resistance_register_value / [(Rated_voltage_register_value × 4.096) / (Sense_resistor_register_value / 125) / (Rated_voltage_register_value / 10)]
Rated_Current	10 [10:0]	Rated Current (mA) = Rated_current_register_value / (Sense_resistor_register_value / 125)
Startup_Current	10 [15:13]	0: NA. else Startup Current = Rated Current × 1/8 × (startup_current_register_value + 1)
Max_start_curr	11[6]	Refer to the application note.
Acceleration	9 [7:0]	Acceleration (Hz/s) = Acceleration_register_value × k if range = 0 then k = 0.05, else k = 3.2
Accelerate_range	8 [13]	
speed_close_loop	8 [11]	1: closed loop. 0: open loop.
Direction	8 [14]	1: A→B→C. 0: A→C→B.
SPD mode	10 [11]	1: analog 0: digital (PWM or Clock).
Clock_PWM	8 [12]	1: clock mode. 0: PWM mode.
PWMin_range	8 [15]	1: ≤ 2.8 kHz 0: > 2.8 kHz.
speed_response_tc_and_clock_speed_ratio	22 [5:0]	When 'open loop' speed is enabled, this setting has no effect. When 'closed loop' speed is enabled, the setting controls the speed response time constant: Time constant (seconds) = speed_response_tc_and_clock_speed_ratio / 15. When clock mode is enabled, this setting also controls the ratio between input frequency and target motor speed: Ratio (rpm/Hz) = speed_response_tc_and_clock_speed_ratio × 0.25. If used, the programmed value of this setting must be between 1 and 41.
Speed_input_off_threshold	21 [9:8]	00: 10%. 01: 6% 10: 15%. 11: 20%
FG_pin_dis	14[4]	1: FG pin is always high, facilitate the I²C communication.
Startup_mode	11 [11:10]	00: 6 pulse mode. 01: 2 pulse mode. 10: slight-move mode. 11: align & go.
Wait_stationary	11[12]	Refer to the application note.
IPD_current_thrd	18 [13:8]	IPD current threshold (A) = IPD_current_thrd_value × 0.086
Slight_mv_demand	21 [7:5]	Amplitude demand in slight move mode (%) = value × 3.2 + 2.4
PID_P	12 [7:0]	Position observer loop P gain.
PID_I	13 [7:0]	Position observer loop I gain.
Motor_Inductance	12 [12:8]	Refer to the application note.
Direct_dr_Angle	11[5]	1: The 12[12:8] value will directly control the phase advance angle in units of degrees.
Sense_Resistor	20 [15:8]	Sense resistor value (mΩ) = sense_resistor_value / 3.7
Open_drive	11 [3]	Refer to the application note.
Power_Ctrl_En	11 [7]	1: enable the current limit.
Open_window	12 [15]	1: open window for inductance tuning. 0: normal
delay_start	13[13]	1: delayed start. 0: start right after windmill checking.

Continued on next page...

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Table 2: Register and EEPROM Map Notes (continued)

Parameter	Address	Notes
Soft_off	15 [6]	Refer to the functional description.
Soft_on	15 [7]	Refer to the functional description.
Soft_off_time	22[9]	Maximum soft off-time. 1: 4 seconds. 0: 1 second.
First_Cycle_Speed	16 [7:6]	00: 0.55 Hz. 01: 1.1 Hz. 10: 2.2 Hz. 11: 4.4 Hz
Accelerate_buffer	16 [9:8]	Refer to the application note.
Decelerate_buffer	16 [11:10]	Refer to the application note.
Deadtime_setting	15[11:8]	(n + 1) × 40 ns.
deadtime_comp	22[12]	1: enable the deadtime compensation logic.
drive_gate_slew	18[15:14]	Refer to the electronics characterization table.
mosfet_ciss_comp	19[15:8]	Refer to the electronics characterization table. Ciss / gate slew 00 / gate slew 01 / gate slew 10 200 pF / 0x55 / 0x44 / 0x33 400 pF / 0x88 / 0x66 / 0x44 600 pF / 0xBB / 0x77 / 0x55 1000 pF / 0xCC / 0x88 / 0x66 2000 pF / 0xFF / 0xCC / 0x88 3000 pF / 0xFF / 0xFF / 0xBB 4000 pF / 0xFF / 0xFF / 0xEE Refer to the application note for more details.
Standby_mode	21 [15]	0: enable. 1: disable.
Brake_mode	22 [8]	0: brake when safe. 1: 100% uncontrolled
Safe_brake_thrd	15 [15:14]	00: 1× rated current. 01: 2×. 10: 4×. 11: 8×.
OCP_reset_mode	16 [3]	0: upon motor restart. 1: after 5 seconds.
OCP_Enable	16 [2:0]	100: 480 ns filter. 111: OCP disabled.
OCP_masking	16 [5:4]	00: no masking. 01: 320 ns masking. 10: 640 ns masking. 11: 1280 ns masking. Refer to the application note for more details.
vds_threshold_sel	22 [15]	1: 2 V. 0: 1 V. Refer to the application note for more details.
Angle_Error_Lock	15 [3:2]	Lock detect during startup. 00: disabled. 01: 5 degrees. 10: 9 degrees. 11: 13 degrees
BEMF_lock_filter	16 [13:12]	Refer to the application note.
Extend_lock_mask	11 [14]	Refer to the application note.
Vibration_lock	22 [10]	Refer to the application note.
Over_speed_lock	12 [13]	Refer to the application note.
Restart_attempt	22 [7:6]	00: Always. 01: 3 times. 10: 5 times. 11: 10 times.
Lock_restart_set	22 [11]	0: 5 seconds. 1: 10 seconds.
i2c_spd_mode	17 [9]	0: controlled by SPD pin. 1: controlled by register value in 17 [8:0].
i2c_spd_demand	17 [8:0]	0~511 represents 0~100%

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Table 2: Register and EEPROM Map Notes (continued)

Parameter	Address	Notes
READBACK		
Motor speed	120	Motor Speed (Hz) = register_value × 0.530 Hz
Bus current	121	Bus current (mA) = register_value / (Sense_resistor_register_value / 125)
Q-axis current	122	Q-axis current (mA) = register_value / (Sense_resistor_register_value / 125)
V_{BB}	123	V_{BB} (V) = register_value / 5
Temperature	124	Temperature (°C) = register_value – 53
Control demand	125	0~511 represents 0~100%
Control command	126	0~511 represents 0~100%
Operation state	127 [15:12]	

Note: Refer to application note and user interface for additional detail.

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Programming EEPROM

The A89301 contains 24 words of EEPROM, each of 16 bit length. The EEPROM is controlled with the following I²C registers.

EEPROM Control – Register 161: Used to control programming of EEPROM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Set EEPROM voltage required for Writing or Erasing.
1	ER	Sets Mode to Erase.
2	WR	Sets Mode to Write.
3	RD	Sets Mode to Read.
15:4	n/a	Do not use; always set to zero (0) during programming process.

EEPROM Address – Register 162: Used to set the EEPROM address to be altered

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
0:4	eeADDRESS	Used to specify EEPROM address to be changed. There are 20 addresses. Do not change address 0 or 19 as these are factory-controlled.
15:5	n/a	Do not use; always set to zero (0) during programming process.

EEPROM Data_In – Register 163: Used to set the EEPROM new data to be programmed

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the EEPROM address to be erased or written. There are 24 addresses.

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EEPROM Commands

There are three basic commands, Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 10 ms per word.

Each word must be written individually. The following examples are shown in the following format:

I2C_register_address [data] ; comment

Example #1: Write EEPROM address 7 to 261 (hex = 0x0105)

1. Erase the existing data.
   - A. 162 [7] ; set EEPROM address to erase.
   - B. 163 [0] ; set Data_In = 0x0000.
   - C. 161 [3] ; set control to Erase and Voltage High.
   - D. Wait 15 ms ; requires 15 ms High Voltage Pulse to Write.
2. Write the new data.
   - A. 162 [7] ; set EEPROM address to write.
   - B. 163 [261] ; set Data_In = 261.
   - C. 161 [5] ; set control to Write and Set Voltage High.
   - D. Wait 15 ms ; requires 15 ms High Voltage Pulse to Write.

Example #2: Read address 7 to confirm correct data properly programmed.

1. Read the word.
   - A. 7 [N/A for read] ; read register 7; this will be contents of EEPROM.

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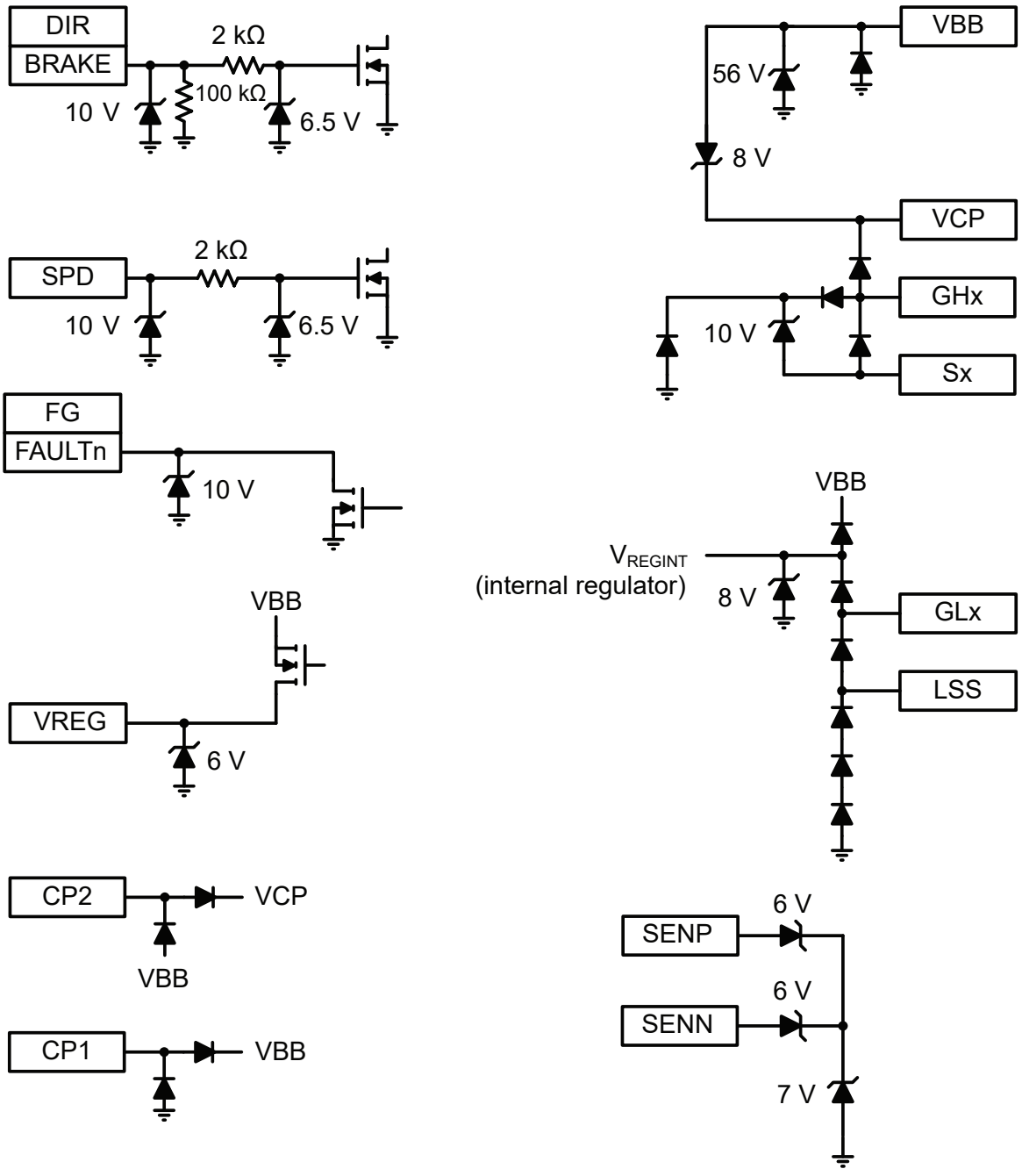
PIN DIAGRAMS



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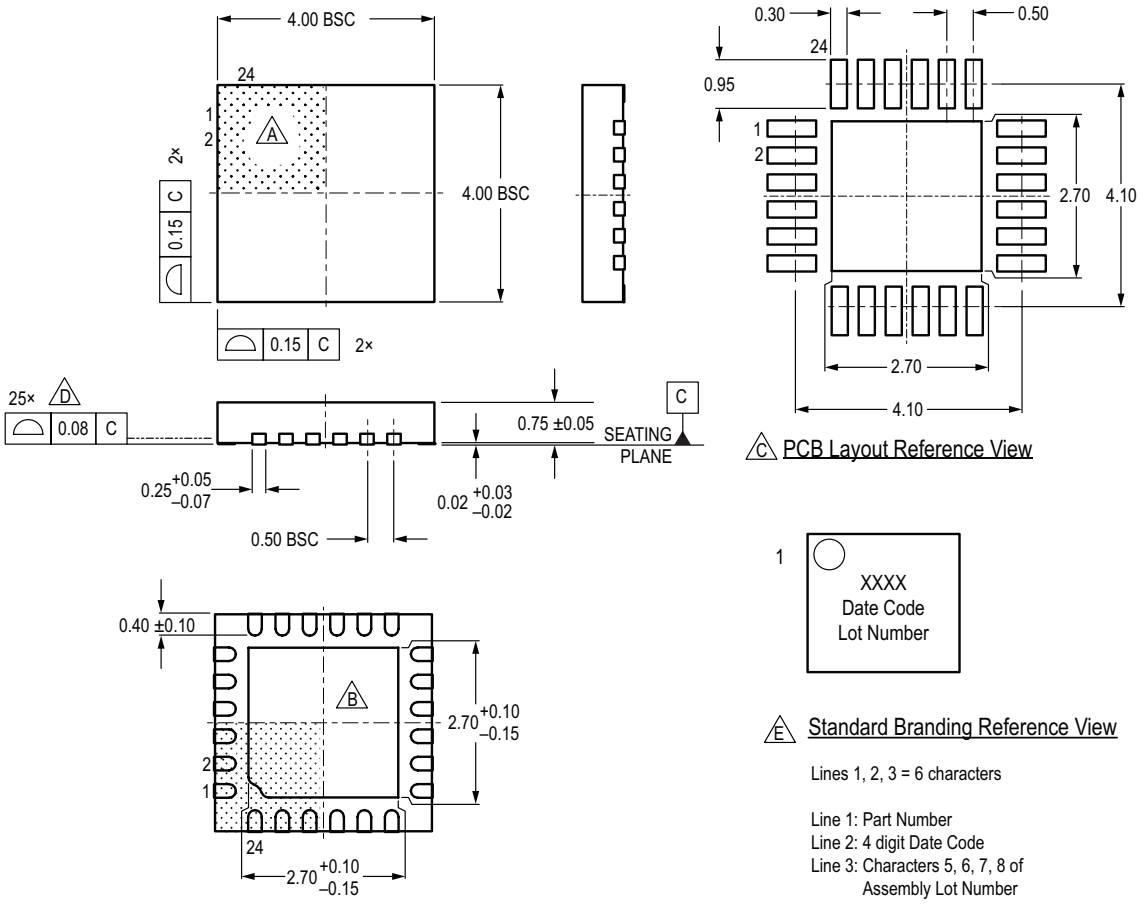
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD.)
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 8: Package ES, 24-Contact QFN with Exposed Pad

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Revision History

Number	Date	Description
–	December 13, 2018	Initial release
1	January 24, 2019	Updated Motor PWM Frequency (page 4); added deadtime_comp to Table 1 (page 11) and Table 2 (page 13); added mosfet_comp to Table 2 (page 13).
2	March 19, 2019	Updated Output Voltage Absolute Maximum Rating (page 2), PWM Mode and Clock Mode (page 6), Motor Stop and Standby Mode (page 7-9), I²C Operation, EEPROM Map (page 10-15), and EEPROM Commands (page 17).
3	June 10, 2019	Minor editorial updates
4	August 10, 2020	Updated table 1, “support_gt_slew[7:0] ” to “mosfet_ciss_comp[7:0] ” (page 13). Updated table 2, “mosfet_comp ” to “mosfet_ciss_comp ” (page 15).
5	March 19, 2021	Added Functional Block Diagram (page 4); updated Register 22[5:0] (pages 14-15), EEPROM Register 163 description (page 18), EEPROM Commands section (page 19)
6	August 9, 2021	Updated Fault Table (page 8) and package drawing (page 21); added System Error and OVP sections (page 9)

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