

Structure            Silicon Monolithic Integrated Circuit

Product            Power Management for Cellular Phone

Type                **BH6038KN**

Function            -A built-in 7-channel CMOS-typed series regulator.  
                       -A built-in Lithium battery charge control circuit.

○Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Range	Unit	Condition
Maximum Supply Voltage	V <sub>MAX</sub>	7.0	V	
Power Dissipatin 1	P <sub>d1</sub>	500            (*1)	mW	
Power Dissipatin 2	P <sub>d2</sub>	700            (*2)	mW	
Operating Temperature Range	T <sub>opr</sub>	-30 ~ +75	°C	
Storage Temperature Range	T <sub>stg</sub>	-55 ~ +125	°C	

(\*1) This value is the allowable loss of a single package. Reduce 5.0mW/°C when Ta=25°C or above.

(\*2) Reduce 7.0mW/°C when Ta=25°C or above.

When mounted on a 70mm×70mm×1.6mm thick glass epoxy PCB.

○Recommend Movement Range (Ta = -30~+80°C)

Parameter	Symbol	Range	Unit	Condition
Battery Voltage	VBAT	3.20~4.50	V	
Adapter Voltage	VADP	4.60~5.90	V	
Operating Temperature range	Topr	-30~+75	°C	

This product is not especially designed to be protected from radioactivity.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

Use-related Cautions

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toy).

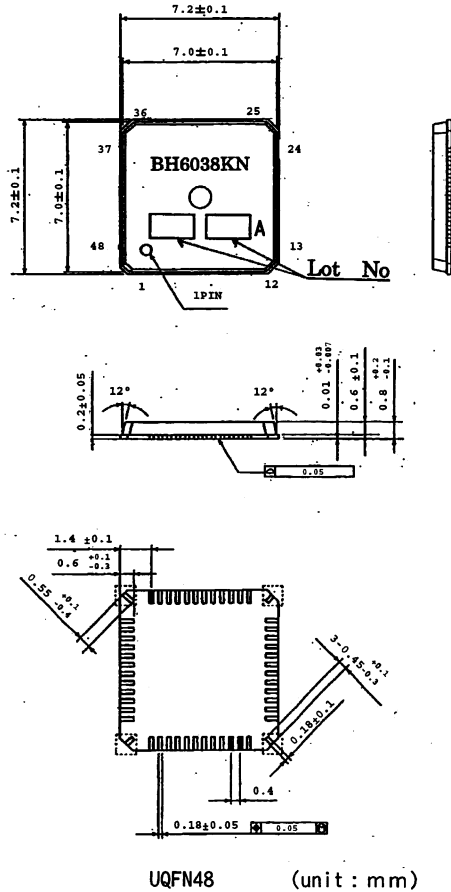
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○Electrical Characteristics

Unless otherwise specified, Ta=+25°C, VBAT=3.6V

Parameter	Symbol	Spec			Unit	Condition	
		MIN	TYP	MAX			
REG1 Output Voltage	VO1	2.79	2.85	2.91	V	Io=50mA	
REG1 Load Stability	ΔVL1	-	10	65	mV	Io=1~75mA	
REG1 Input Voltage Stability	ΔVI1	-	10	60	mV	VBAT=3.3~4.5V, Io=50mA	
REG2 Output Voltage	VO2	1.79	1.85	1.91	V	Io=30mA	
REG2 Load Stability	ΔVL2	-	10	65	mV	Io=1~45mA	
REG2 Input Voltage Stability	ΔVI2	-	10	60	mV	VBAT=3.3~4.5V, Io=30mA	
REG3 Output Voltage	VO3	2.79	2.85	2.91	V	Io=120mA	
REG3d Stability	ΔVL3	-	15	80	mV	Io=1~180mA	
REG3 Input Voltage Stability	ΔVI3	-	10	60	mV	VBAT=3.3~4.5V, Io=120mA	
REG4 Output Voltage	VO4	1.79	1.85	1.91	V	Io=50mA	
REG4d Stability	ΔVL4	-	10	65	mV	Io=1~75mA	
REG4 Input Voltage Stability	ΔVI4	-	10	60	mV	VBAT=3.3~4.5V, Io=50mA	
REG5 Output Voltage	VO5	2.79	2.85	2.91	V	Io=80mA	
REG5d Stability	ΔVL5	-	15	80	mV	Io=1~120mA	
REG5 Input Voltage Stability	ΔVI5	-	10	60	mV	VBAT=3.3~4.5V, Io=80mA	
REG6 Output Voltage	VO6	2.79	2.85	2.91	V	Io=40mA	
REG6d Stability	ΔVL6	-	15	80	mV	Io=1~60mA	
REG6 Input Voltage Stability	ΔVI6	-	10	60	mV	VBAT=3.3~4.5V, Io=40mA	
RFREG Output Voltage	VORF	2.74	2.8	2.86	V	Io=60mA	
Fred Stability	ΔVLRf	-	20	60	mV	Io=1~60mA	
Charge Controller (With 0.33Ω Charge Current Detection Resistor Connected)							
Charge Control Voltage	VCHG	4.17	4.20	4.23	V	Ta=-10~60°C Charge current : 60mA	
Rapidity Charge Current	ICHG	0.9C	1C	1.1C	mA	1C=500mA	
SETR Current	ISETR	80	90	100	mA		
Overload Protection detect current	ILIM	1.8C	2.0C	2.2C	mA		
Convergence detect current	IDET08C	0.7C	0.8C	0.9C	mA		
Forced charge current	ICMCG	17	43	69	mA	VBAT=1.89V	
Forced charge start voltage	VCMCG	1.9	2.0	2.1	V		
Adapter Detection	6.0V detect voltage	VAD60	5.9	6.1	6.3	V	In voltage rise
	Hysteresis voltage	ΔVAD60	20	50	100	mV	
	3.0V detect voltage	VAD30	2.8	3.0	3.2	V	In voltage fall
	Hysteresis voltage	ΔVAD30	20	50	100	mV	
Battery Voltage detection	5.0V detect voltage	VVD50	4.85	5.1	5.35	V	In voltage fall
	Hysteresis voltage	ΔVVD50	50	100	150	mV	
	4.43V detect voltage	VVD43	4.43	4.56	4.69	V	In voltage fall
	Hysteresis voltage	ΔVVD43	20	50	100	mV	
	3.3V detect voltage	VVD33	3.25	3.42	3.59	V	In voltage fall

○Package Diagram

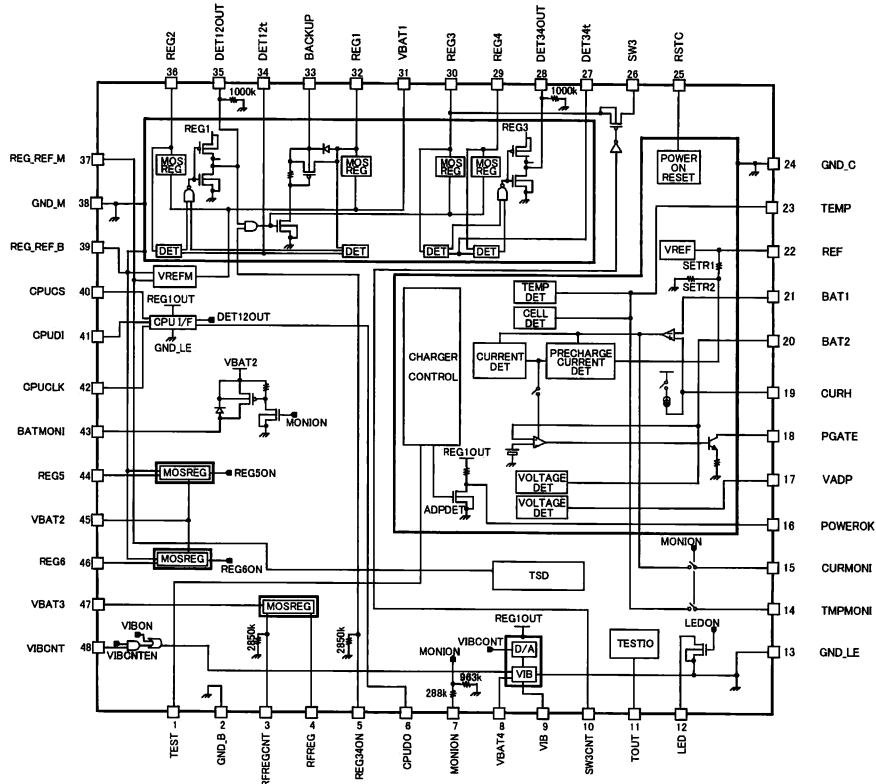


○Terminal table

PIN	BALL Name	PIN	BALL Name
1	TEST	25	RSTC
2	GND_B	26	SW3
3	RFREGCNT	27	DET34t
4	RF_REG	28	DET34OUT
5	REG34ON	29	REG4
6	CPUDO	30	REG3
7	MONION	31	VBAT1
8	VBAT4	32	REG1
9	VIB	33	BACKUP
10	SW3CNT	34	DET12t
11	TOUT	35	DET12OUT
12	LED	36	REG2
13	GND_LE	37	REG_REF_M
14	TMPMONI	38	GND_M
15	CURMONI	39	REG_REF_B
16	POWEROK	40	CPUCS
17	VADP	41	CPUDI
18	PGATE	42	CPUCLK
19	CURH	43	BATMONI
20	BAT2	44	REG5
21	BAT1	45	VBAT2
22	REF	46	REG6
23	TEMP	47	VBAT3
24	GND_C	48	VIBCNT

Note) Indicated parts by broken lines are not required for implementation  
Schematic No.: EX343-5001-1

○Block Diagram



## ○Use-related Cautions

## (1) Absolute maximum ratings

If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

## (2) Recommended operating range

This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

## (3) Reverse connection of power supply connector

There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

## (4) Power supply lines

In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

## (4) GND voltage

Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

## (6) Shorts between pins and misinstallation

When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

## (7) Operation in strong magnetic fields

Be careful when using the LSI in a strong magnetic field, since it may malfunction.

## (8) Inspection in set board

When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

## (9) Input pins

Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

## (10) Ground wiring pattern

When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

## (11) Externally attached capacitors

When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

## (12) Thermal shutdown circuit (TSD)

When junction temperatures become 150°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

## (13) Thermal design

Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

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